EELE 414 – Introduction to VLSI Design
Homework #1

Name: _____
Grade: _____ /10

NOTE: Print this sheet and use as a cover for your homework set. Staple your solutions to the back with your name in the upper right corner of each page. Clearly indicate which problem number you are working. Clearly mark your solution. Show your work for partial credit.

1) VLSI Design Economy (5 pts)

Your company is going to produce a digital IC that performs a dedicated task. The application is not demanding from a performance perspective so all implementations options are available (i.e., ASIC, STD_Cell, Structured ASIC, or FPGA). Your job is to determine the break even time (in months) for each of the different implementations options.

The following information can be used for your analysis:

	Custom ASIC	**STD Cell**	**Structured ASIC**	**FPGA**
Upfront NRE:	$500k	$300k	$100k	$0
# of Design Engineers:	4	3	2	2
Man-Months Per Engineer	18	12	9	9
Your cost for each IC	$1.25	$2.25	$5.25	$25

Monthly Cost Per Engineer	$10,000/month
Predicted Monthly Volume	10,000 pieces/month
Sale Price for IC	$30/chip

a) Calculate the # of months until each of the 4 implementation approaches breaks even. You can assume that all of the upfront cost can be lumped into a single number and that all techniques begin generating revenue in month 1.

b) Produce a plot comparing the monthly income/debt for each of the implementation approaches. Plot the income debt as bar graphs against time (in months). Add a line for the cumulative sum of income/debt. Your lines should intersect the $0 cumulative sum mark at the number of months calculated in part a.

c) Find the number of months after the breakeven point that you have accumulated $1M in profit for each of the 4 techniques.

2) Modern FPGA Cost (5 pts)

a) You are going to go out and find the real cost of modern FPGAs. You are to find out the cost of the most expensive Xilinx Virtex 7 FPGA and the least expensive Xilinx Virtex 6 FPGA. The most expensive will be the largest die, most IO, fastest speed grade, and most bells and whistles. The least expensive will be the smallest die, least IO, slowest speed grade, and least bells and whistles. If volume is a consideration, you can use the most conservative numbers (i.e., the lowest volume for the most expensive parts and the highest volume for the least expensive parts).