EELE 414 – Introduction to VLSI Design
Homework #2 due 10/22/15

Name: _____
Grade: _____ /10

1) MOS Behavior:
(3 Points)

a) For a MOS structure with p-type Silicon, sketch the locations of the charge carriers during *depletion.* You can indicate electrons as $\mathbf{e}^-$ and holes as $\oplus$. Indicate the location of the depletion region and any polarization that occurs in the oxide. Indicate where x_d is located. Assume that V_B=0v and that V_G>0 (small).

b) Now sketch the locations of the charge carriers during *inversion*. Show the depletion region, the inversion layer, and any polarization that occurs in the oxide. Indicate where x_{dm} is located. Assume that V_B=0v and that V_G>0 (large).

c) If we dope the p-type silicon to a carrier concentration of $N_A=10^{16}cm^{-3}$ and a resulting Fermi potential of ϕ_{Fp}=-0.35 V, what is the maximum depletion depth (x_{dm}) during inversion?

2) MOSFET Behavior
(3 Points)

a) For a MOSFET structure with p-type Silicon, sketch the locations of the charge carriers during *depletion.* Indicate the location of the depletion region and any polarization that occurs in the oxide. Assume that $V_B=V_S=V_D$=0v and that V_G>0 (small).

b) Now sketch the locations of the charge carriers during *inversion*. Show the depletion region, the inversion layer, and any polarization that occurs in the oxide. Assume that $V_B=V_S=V_D$=0v and that V_G>0 (large).

c) When we apply a voltage to the Gate, it causes a depletion region beneath it. If $V_S=V_D$=0v, why is there a depletion region around the Source and Drain?

3) Threshold Voltage
(3 Points)

a) Given a MOSFET system with the following parameters:
(2 points)

t_{ox} = 200 Å
ϕ_{GC} = -0.245 V (Built in potential of the Gate-to-Channel MOS system)
$N_A = 2 \cdot 10^{15}$ cm^{-3}
$Q_{ox} = q \cdot 2 \cdot 10^{11}$ C/cm^2

Find the threshold voltage V_{T0} under zero substrate bias at room temperature (T=300 k). Note that $\varepsilon_{ox} = 3.97 \cdot \varepsilon_0$ and $\varepsilon_{Si} = 11.7 \cdot \varepsilon_0$.

b) Now assume that there is a substrate bias of V_{SB} = 0.5V and find the new threshold voltage (V_T). You are given that γ=0.39 $V^{½}$. Note: you will need some of your answer from part a (V_{T0} & ϕ_F). Hint, your answer from part (a) should have been between $0.2 < V_{T0} < 0.4$. If it isn't, use V_{T0}=0.3v for this part.
(1 point)

4) MOSFET Modes of Operation
(1 Point)

What regions are the following NMOS transistors operating in if V_T=1 v?