

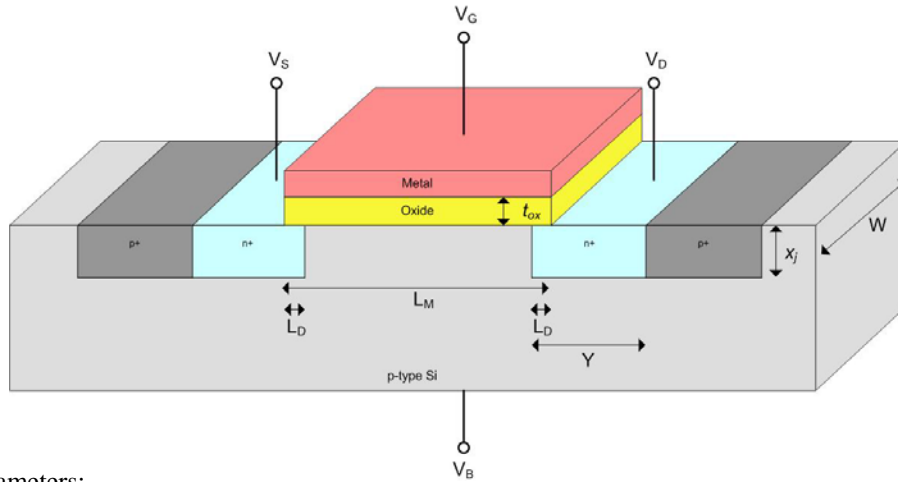
EELE 414 – Introduction to VLSI Design
Homework #4 (show work for full credit)

Name: _____

Grade: _____ /10

1) MOSFET Capacitance Calculations
 (5 Points)

Given the following N-Channel, enhancement-type MOSFET:



with parameters:

N_A	$= 10^{15}$	cm^{-3}	(Substrate Doping)
N_D	$= 10^{19}$	cm^{-3}	(Source/Drain Doping)
N_{Asw}	$= 10^{18}$	cm^{-3}	(Sidewall p+ Doping)
L_M	$= 0.25$	μm	(Drawn Channel Length)
L_D	$= 0.0025$	μm	(Gate Overlap)
W	$= 2.5$	μm	(Channel Width)
Y	$= 1$	μm	(Junction Length)
x_j	$= 0.25$	μm	(Junction Depth)
t_{ox}	$= 5.6$	nm	(Gate Oxide Thickness)
C_{ox}	$= 0.627$	$\mu\text{F}/\text{m}^2$	(Unit Gate Oxide Capacitance) notice the units!!!

This MOSFET has diffusion regions (i.e., the Source and Drain) that are surrounded by “channel-stop-implants” with p+ doping to isolate it from its neighboring MOSFETs. This MOSFET has a $V_S=0\text{v}$ and a V_D that changes from 0 to 2.5v.

Find the capacitances: C_{gs} , C_{gd} , C_{gb} , C_{sb} , and C_{db} :
 (points 1pt, 1pt, 1pt, 1pt, 1pt)

Tips:

- For the Oxide related capacitances (C_{gs} , C_{gd} , C_{gb}), find the capacitance values that represent a worst case. You can assume the NMOS is in the linear region for the oxide calculations. Remember the *effective Gate Length*.
- Example 3.8 in the textbook walks through finding the junction capacitance C_{db} when changing from 0.5v to 5v. You can use this as a reference to find the junction capacitance during a changing voltage.
- For C_{sb} , there is no voltage change across the p/n junction.

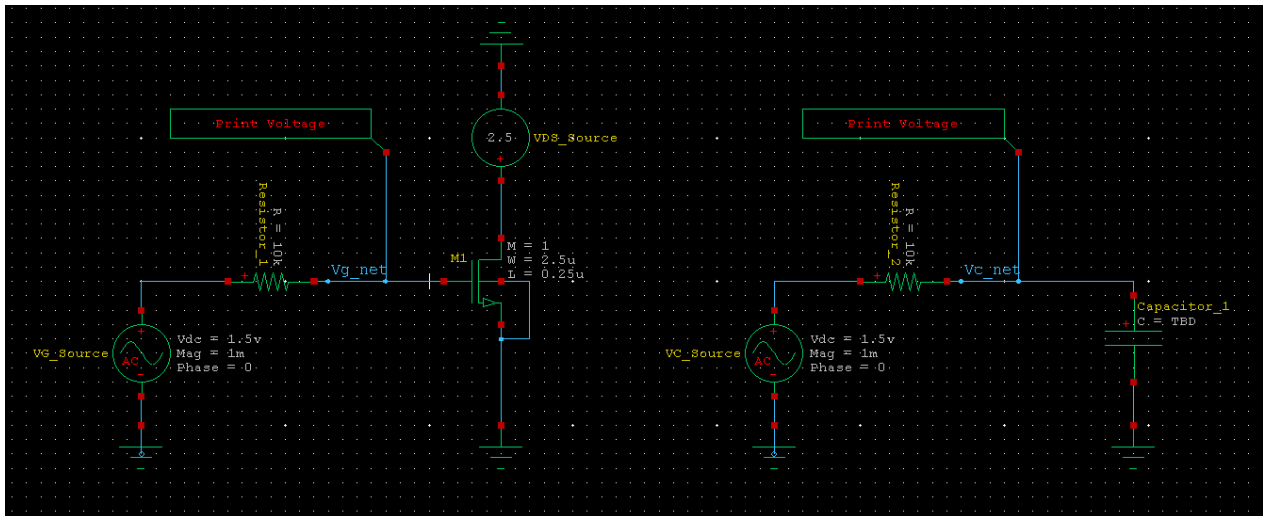
2) MOSFET Capacitance using SPICE (LEVEL 1)
(3 points)

One way you can find the capacitance of a device is performing an AC simulation using SPICE. If you drive a small AC signal through a resistor into the gate of the device, you will observe a frequency response that looks similar to an RC low-pass filter. The capacitance that makes the response at the gate roll off is due to the input capacitance of the device. If you include an ideal RC circuit in your simulation with the same resistor value, you can alter the ideal capacitor to try to match the two responses (device vs. ideal). Whatever the capacitance value you find in the ideal RC circuit that causes the responses to match is the actual capacitance of the input of the device.

The capacitance of the device is modeled at different levels. In the Generic 0.25um kit on the course website, there is a Level 1 model that does not contain any parasitic parameters. This level will only model the Cox of the device. This means input capacitance will change with W/L, but will NOT change as you put the device into different regions of operation (Cut-off, Linear, Saturation).

A Level 2 model is provided in the Generic 0.25um kit that **does** include the parasitic parameters of the device and will show a change in input capacitance as you put the device into different modes of operation.

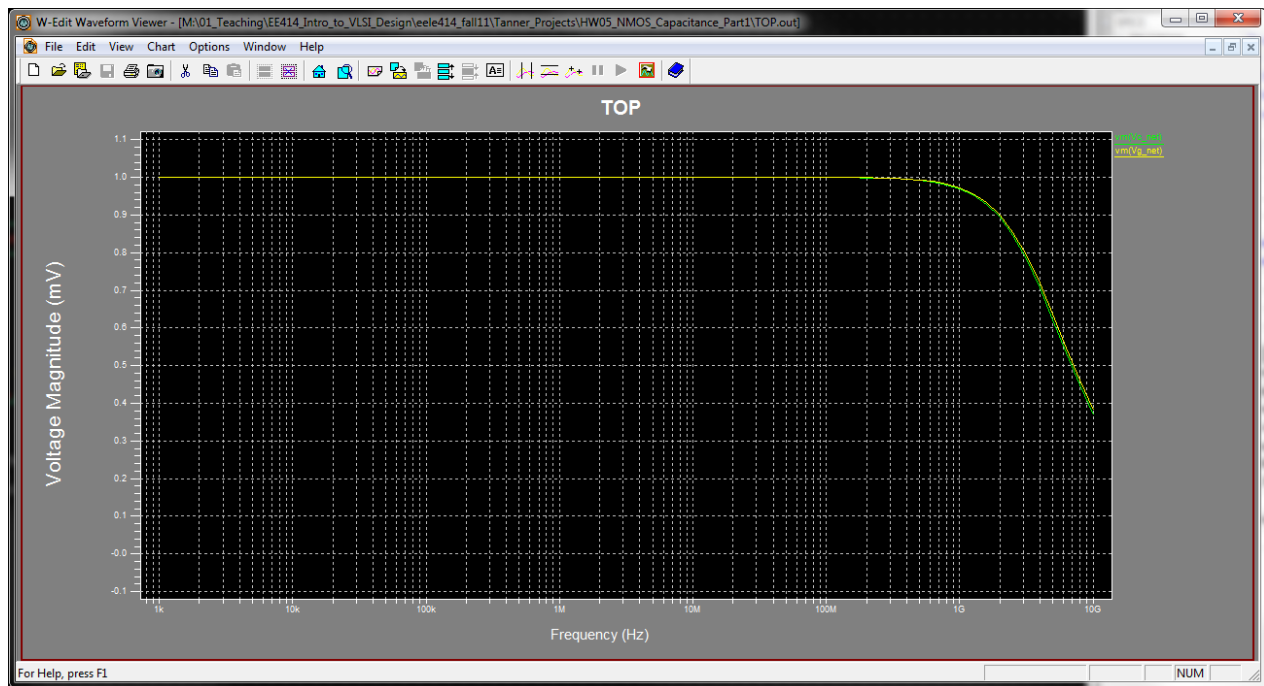
- a) Use SPICE and the technique described above to determine the input capacitance of an NMOS transistor from the Generic 0.25um process with $L_n=0.25\mu\text{m}$ & $W_n=2.5\mu\text{m}$. Use the **Level 1** models. Use a resistor value 10k in order to bring the pole of the response down to a reasonable level. Your schematic should look like the following.



Things to note:

- When you put down a voltage source and configure it as “AC”, you can specify both a DC offset and an AC signal (Mag & Phase). You can use the DC component as how you turn on/off the device ($V_G > V_t$). You want to put a very small AC signal on top of the DC signal so that it isn't large enough to effect the mode of operation of the device. 1mV is small enough for this problem.
- Use a 10k resistor in order to bring the pole down below 10GHz.
- Run the AC simulation from 1k to 10G with a dec scale and 10 steps per decade
- You want to observe on the device side of the resistor since if you observe at the output of the ideal voltage source, you will simply see the ideal output.

- You should get a frequency response like the following once you dial in the correct value of the capacitor. Hint, it is not very large (i.e., fF).



To receive full credit, turn in the following:

- the value of capacitance you found
- a plot of your schematic
- a plot of your frequency response

3) MOSFET Capacitance using SPICE (LEVEL 2)
(2 points)

Now use the same simulation technique to find the input capacitance of this NMOS when using the **Level 2** models when it is in the **linear region**. You will need to change the spice library file to the Level 2 file that is found in the Generic 0.25um kit. You will also need to provide a VGS and VDS voltage that puts the device in the linear region.

To receive full credit, turn in:

- the value of the capacitance you found
- a print out of the SPICE Netlist of your top level circuit.