## To the EELE414 class,

Here are the changes I used to get Tanner to function.

- 1. The Generic\_025\_SPICE\_Models\_Level1.lib library file has some brackets, and a ".end" statement that confused the new version of Tanner. Use the new library attached dated 10/02/12.
- 2. Be sure <u>not</u> to change the M=1 variable to M1 (maybe only I did this!) this must be an integer and is used for multi-fingered gate structures. Change the <u>name</u> from NMOS\_1 to M1. When the NMOS\_1 Device and the has been correctly updated:



Clicking on the "eye" symbol on the properties window will show only the visible parameters of the selected schematic symbol making it easier to see.

3. The "Print Device Terminal" block should look like:

			DXIN N N N O	
			a Device MML a Tempal D	
rint Device Terminal				
irrent:D of MM1				

4. The rest of the "Guide to Tanner for VLSI" seems to be correct.

## 5. The "TOP.sp" compiled file from S-Edit may be opened in T-Spice and looks like:

- \* SPICE export by: S-Edit 15.22
- \* Export time: Tue Oct 02 14:17:23 2012
- \* Design: HW03\_NMOS\_IV\_Part1
- \* Cell: top
- \* Interface: view0
- \* View: view0
- \* View type: connectivity
- \* Export as: top-level cell
- \* Export mode: hierarchical
- \* Exclude empty cells: yes
- \* Exclude .model: no
- \* Exclude .end: no
- \* Exclude simulator commands: no
- \* Expand paths: yes
- \* Wrap lines: no
- \* Root path: C:\Documents and Settings\andyo\My Documents\Tanner EDA\Tanner Tools
- v15.2\EELE414\_VLSI\_Fall2012Tanner\_Projects\HW03\_NMOS\_IV\_Part1
- \* Exclude global pins: no
- \* Exclude instance locations: yes
- \* Control property name: SPICE

\*\*\*\*\*\*\*\*\* Simulation Settings - General Section \*\*\*\*\*\*\*\*
.probe
.option probev
.option probei
.lib "C:\Documents and Settings\andyo\My Documents\Tanner EDA\Tanner Tools
v15.2\EELE414\_VLSI\_Fall2012Tanner\_Projects\Tanner\_Libraries\Generic\_025\_Kit\Generic\_025\_SPICE\_Models\_
Level1.lib"
\*\*\*\*\*\*\*\*\* Simulation Settings - Parameters \*\*\*\*\*\*\*\*

.param VDS\_param = 2.5 .param VGS\_param = 1

```
*------ Devices With SPICE.ORDER > 0.0 ------
***** Top Level *****
MM1 N_1 N_2 Gnd Gnd NMOS W=2.5u L=250n M=1 AS=2.25p PS=6.8u AD=2.25p PD=6.8u
VVDS_source N_1 Gnd DC VDS_param
VVGS_Source N_2 Gnd DC VGS_param
.PRINT DC ID(MM1)
```

\*\*\*\*\*\*\*\*\* Simulation Settings - Analysis Section \*\*\*\*\*\*\*\*\* .dc lin VDS\_param 0 2.5 100m lin VGS\_param 1 1.5 250m

\*\*\*\*\*\*\*\* Simulation Settings - Additional SPICE Commands \*\*\*\*\*\*\*\*

.end

Syntax for the libraries and p-spice net lists are in the tspice.pdf manual in the document folder of the Tanner Directory on the C: drive.

Corrected listing for Generic\_025\_SPICE\_Models\_Level1.lib:

\* Generic 0.25um Process \*\*\*\*\*\* .MODEL NMOS NMOS +LEVEL = 1\* Electrical Properties +KP = 178e-6+VTO = 0.3703728+GAMMA = 0.029+PHI = 0.279+LAMBDA = 0.05\* Physical Parameters, these are overriden by the electrical parameters but are included for refernce +UO = 284.0529492+TOX = 5.6E-9 +NSUB = 1e15 \*+LD = 0.0025e-6 \* Not going to use this for now, it effects KP & COX & results in ~2-3% difference in IDS .MODEL PMOS PMOS +LEVEL = 1\* Electrical Properties +KP = 62.7e-6+VTO = -0.4935548+GAMMA = 0.029+PHI = 0.279+LAMBDA = 0.05\* Physical Parameters, these are overriden by the electrical parameters but are included for refernce +UO = 100+TOX = 5.6E-9 +NSUB = 1e15\*+LD = 0.0025e-6 \* Not going to use this for now, it effects KP & COX & results in ~2-3% difference in IDS

\*.END