

EELE 414 – Introduction to VLSI Design
3 Credits, Fall Semester, 2014
Department of Electrical & Computer Engineering
Montana State University
Bozeman, MT

Description: This course introduces students to the fundamentals concepts of CMOS VLSI circuit design. This course will cover CMOS device characteristics and timing. CMOS fabrication will be covered including process steps, metal, active, and poly layers, and design rules. CAD tools will be introduced for use in design, simulation, and layout of integrated circuits. Design analysis techniques will be presented for the static and dynamic evaluation of CMOS circuits. Memory elements including flip-flops, SRAM, and DRAM will also be presented.

Outcomes: At the end of this course the student should be able to:

- 1) Design and analyze a MOSFET circuit
- 2) Create an integrated circuit layout from a schematic
- 3) Create a schematic from an integrated circuit layout
- 4) Describe the fabrication process of a CMOS circuit
- 5) Design a complex CMOS gate from a truth table
- 6) Verify performance of a CMOS gate using hand calculations and SPICE simulations
- 7) Use a CAD tool to generate the layout of a CMOS circuit
- 8) Understand the impact of layout on the performance of a CMOS circuit

Instructor: Andy V. Olson
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Time & Location: TR, 11:00am – 12:15pm,
632 Robert Hall

Required Text: *“CMOS Digital Integrated Circuits” 3rd Edition.*
Sung-Mo Kang and Yusuf Leblebici, McGraw Hill, 2003.

Website: [class website](#)

The website will be the main source of information for the course. All handouts, homework, and announcements will be posted. It is the student’s responsibility to download and print the necessary documents needed in the course.

Office Hours: Check my website for the most recent schedule (www.coe.montana.edu/ee/andyo)
Also available through email appointment

Requisites: Pre-requisite(s): EE262, EE317

<u>Distribution</u>	<u>Letter Assignment</u>
Homework - 40%	90% - 100% = A
Exam #1 - 20%	80% - 89% = B
Exam #2 - 20%	70% - 79% = C
Exam #3 - 20%	60% - 69% = D
	0% - 59% = F

Notes:

- Instructor reserves the right to apply a grading curve and to assign +/-’s to grades as appropriate.
- Homework is due at the beginning of class. Late Assignments can be turned in up to one week after the due date to receive up to 50% credit. Assignments over one week late will not receive credit.
- No make up exams will be given. Make plans to attend the scheduled exams.

**General
Outline :**

- 1) CMOS transistor characteristics
- 2) CMOS fabrication process
- 3) SPICE modeling and simulation
- 4) Layout
- 5) CMOS static behavior
- 6) CMOS dynamic behavior
- 8) CMOS combinational logic circuits
- 9) CMOS sequential logic circuits
- 10) CMOS Memory (SRAM, DRAM)

**Academic
Policies**

This course will follow the policies outlined in the *Conduct Guidelines and Grievance Procedures for Students*” (http://www2.montana.edu/policy/student_conduct/) and the *MSU Policy and Procedures Manual* (<http://www2.montana.edu/policy/>). Please consult these documents on policies regarding academic honesty, student and instructor rights, and general standards of conduct.