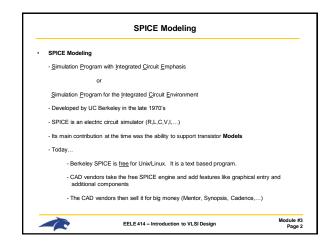
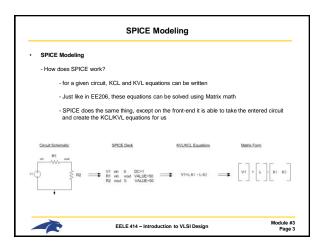
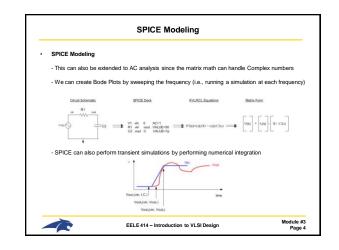
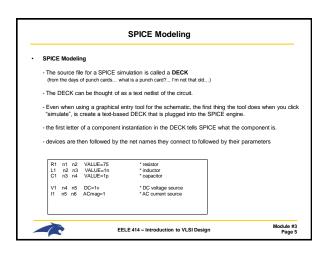
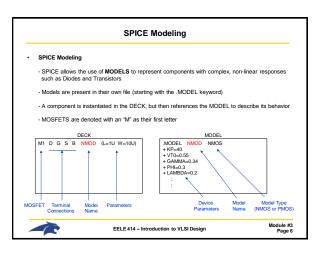
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Module #3 – SPICE Modeling	
Agenda I. SPICE Modeling	
Announcements	
1. Read Chapter 4	
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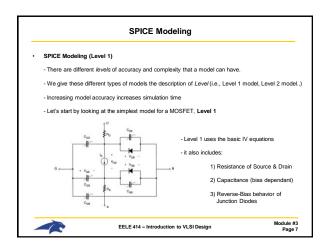


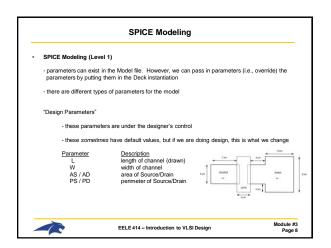


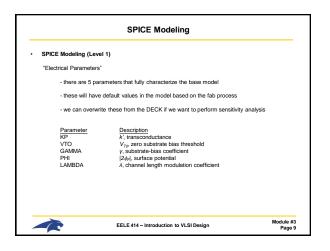


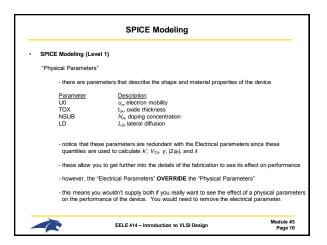












SPICE Modeling			
SPICE Modeling (Level 1)			
"Parasitic Parameters"			
- these are the ca	pacitances and resistances of the material		
Parameter	Description		
CJ	C _{J0} , zero-bias bulk capacitance per area		
CJSW	C_{JOSWP} zero-bias sidewall capacitance per area		
- there parameter	s scale with the size of the device provided by W,L,AS,	AD,PS, and PD.	
	more parameters in table 4.1 in the textbook, take a loo to properly predict the behavior of a transistor.	k and you'll see why	
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SPICE Modeling		
SPICE Modeling (Level 2)		
- Level 2 adds the following behavior to the Level 1 model		
 Variation of the bulk depletion charge dependence on the channel voltage (we assumed i was constant in Level 1). 		
2) Variation of electron mobility (u_n) with the applied E-field		
3) Variation of effective Channel Length in Saturation model		
4) Carrier Velocity Saturation		
5) Subthreshold Conduction		
 we also have the ability to indicate which level we want to use. For example, you can have a Level 2 model, but in the instantiation you say: 		
M1 D G S B NMOD (Level=1 L=1U W=10U)		
this will tell the simulator to ignore all the parameters associated with Level 2 or higher accuracy.		
- we can also put the "Level=1" as the first parameters in the model		
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SPICE Modeling

SPICE Modeling (Level 3)

- Level 3 was developed to specifically address small geometry effects.

- instead of trying to come up with an expression for each and every *bump and wiggle* on the IV curve, Level 3 instead moves toward a more empirical approach.

- curve-fitting parameters are added to the IV equations from Level 1 and Level 2.

- these parameters are dialed-in based on measurement data from a test run of transistors.



