Digital Design: An Embedded Systems Approach Using VHDL

Chapter 6
Implementation Fabrics

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Integrated Circuits

- Early digital circuits
  - Relays, vacuum tubes, discrete transistors
**ENIAC**

- **ENIAC** - Electronic Numerical Integrator And Computer

- Completed machine was unveiled on February 14, **1946** at the University of Pennsylvania

- Cost almost $500,000 (nearly $6 m in 2008, adjusted for inflation).

- ENIAC was designed to calculate artillery firing tables for the United States Army's Ballistic Research Laboratory, but its first use was in calculations for the hydrogen bomb.
ENIAC

- 17,468 vacuum tubes
- 7,200 crystal diodes
- 1,500 relays
- 70,000 resistors
- 10,000 capacitors
- 5 million hand-soldered joints.
- Weighed 30 tons.
- Measured roughly 8.5 by 3 by 80 feet
- Took up 680 square feet
- Consumed 150 kW of power
The basic machine cycle was 200 microseconds (20 cycles of the 100 kHz clock in the cycling unit), or 5,000 cycles per second for operations on the 10-digit numbers.

In one of these cycles, ENIAC could write a number to a register, read a number from a register, or add/subtract two numbers.

A 10- by 10-digit multiplication took 14 cycles, or 2800 microseconds—a rate of 357 per second.

Division or square root took up to 143 cycles, or 28,600 microseconds—a rate of 35 per second.
• Several tubes burned out almost every day, leaving it nonfunctional about half the time.

• Most of these failures, however, occurred during the warm-up and cool-down periods, when the tube heaters and cathodes were under the most thermal stress.

• By the simple (if expensive) expedient of never turning the machine off, the engineers reduced ENIAC's tube failures to the more acceptable rate of one tube every two days.

• "We had a tube fail about every two days and we could locate the problem within 15 minutes."

• In 1954, the longest continuous period of operation without a failure was 116 hours (close to five days).
Integrated Circuits

- Integrated circuits (ICs, or “chips”)
  - Manufacture of multiple transistors and connections on surface of silicon wafer
  - Invented in 1958: Jack Kilby at Texas Instruments (TI)
  - Rapid growth since then, and ongoing
The first working integrated circuit was created by Jack Kilby in 1958. It contains a single transistor and supporting components on a slice of germanium and measures 1/16 by 7/16 inches (1.6 x 11.1 mm).
IC Manufacture: Wafers

- Start with ingot of pure silicon
- Saw into wafers & polish
  - Early wafers: 50mm
  - Now 300mm
IC manufacture: Processing

- Chemical processing steps based on photolithography
  - Ion implantation
  - Etching a deposited film
    - SiO$_2$, polysilicon, metal

Virtex-6 FPGAs are fabricated on a 40nm, triple-oxide, 12-metal layer process
IC Manufacture: Test & Packaging

- Defects cause some ICs to fail
  - Test to identify which ICs don’t work
  - Discard them when wafer is broken into chips
    - Their cost is amortized over working chips
  - Yield depends (in part) on IC area
    - Constrain area to reduce final IC cost

- Working chips are packaged and tested further
Exponential Trends

- Circuit size and complexity depends on minimum feature size
  - Which depends on manufacturing process
    - Mask resolution, wavelength of light
- Process nodes (ITRS Roadmap)
  - Smaller feature size $\Rightarrow$ denser, faster
SSI and MSI

- In 1964, TI introduced 5400/7400 family of TTL ICs
  - Other manufacturers followed, making 7400 family a de facto standard
- Small-scale integrated (SSI)
  - 7400: 4 × NAND gate 7427: 4 × NOR gate
  - 7474: 2 × D flip-flop ...
- Medium-scale integrated (MSI)
  - 7490: 4-bit counter 7494: 4-bit shift reg
  - ...

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Other Logic Families

- Variations on electrical characteristics
  - 74L... : low power
  - 74S... : Schottky diodes ⇒ fast switching
  - 74LS... : compromise between speed and power
  - 74ALS... : advances low-power Schottky
  - 74F... : fast

- CMOS families
  - 4000 family: very low power, 3–15V
  - 74HC..., 74AHC... : TTL compatible
Large Scale Integration

- 1970s: LSI (thousands of transistors)
  - Small microprocessors became feasible
  - Custom LSI chips for high-volume applications
- SSI/MSI mainly used for glue logic
- Later additions to 74xx... families oriented toward glue-logic and interfacing
  - E.g., multibit tristate drivers, registers
  - Other functions supplanted by PLDs
MSI Example: Counter/Display

- **74LS390**: dual decade counter

![74LS390 Diagram]

- **74LS47**: 7-segment decoder

![74LS47 Diagram]
MSI Example: Counter/Display
VLSI and ASICs

- **1980s: Very Large Scale Integration**
  - Then ULSI, then what?
  - VLSI now just means IC design

- **Application-specific ICs (ASICs)**
  - Enabled by CAD tools, foundry services
  - Often designed for a range of related products in a market segment
    - Application-specific standard products (ASSPs)
    - E.g., cell phone ICs
ASIC Economics

- ASIC has lower unit cost than an FPGA
  - But more design/verification effort
  - Higher non-recurring engineering (NRE) cost
    - Amortized over production run
  - ASICs make sense for high volumes
- Full custom
  - Design each transistor and wire
  - High NRE, but best performance & least area
- Standard cell
  - Use basic components from a foundry’s library
Programmable Logic Devices (PLDs)

- PLDs can be programmed after manufacture to vary their function
  - C.f. fixed-function SSI/MSI ICs and ASICs
- Higher unit cost than ASIC
  - But lower NRE
  - Ideal for low to medium product volumes
Programmable Array Logic (PALs)

- Introduced by Monolithic Memories Inc in 1970s
  - First widely-used PLDs
  - Programmed by blowing fusible links in the circuit
    - Use a special programming instrument
- PAL16L8
  - 16 inputs, 8 active-low outputs
- PAL16R8
  - 16 inputs, 8 registered outputs
Feedback path is useful for implementing FSMs
Designing with PALs

- Useful even for simple circuits
  - Single package solution lowers cost
- Describe function using Boolean equations
  - In HDL, or simple language such as ABEL
  - Synthesize to fuse map file used by programming instrument
- If design doesn’t fit
  - Partition into multiple PALs or use a more complex PLD
Generic Array Logic (GALs)

- Programmable Output Logic Macrocells (OLMCs)
  - Use EEPROM technology
  - E.g., GAL22V10
Complex PLDs (CPLDs)

- Cramming multiple PALs into an IC
  - Programmable interconnection network
  - Use flash RAM technology to store configuration
FPGAs

- **Field Programmable Gate Arrays**
  - Smaller logic blocks, embedded SRAM
  - Thousands or millions of equivalent gates

Programmable interconnect
Logic Block Example

- Xilinx FPGA Logic Blocks
  - Lookup Tables (LUTs) plus flip-flops
  - E.g., Spartan-II

- Too complex to program LBs manually
  - Let synthesis tools map HDL code to LBs and program the interconnect
I/O Blocks

- Typically allow for registered or combinational input/output, plus tristates
  - Programmable logic levels, slew rate, input threshold, ...

![Diagram of I/O Blocks]
Platform FPGAs

- Include embedded cores for special applications
  - Processor cores
  - Signal processing arithmetic cores
  - Network interface cores
- Embedded software can run from SRAM in the FPGA
  - Single-chip solution, reduces cost
  - Avoids high NRE of ASIC
Structured ASICs

- Array of very simple logic elements
  - Not programmable, no programmable interconnect
- Customized by designing top metal interconnection layer(s)
  - Lower NRE than full ASIC design
  - Performance close to full ASIC
- May become popular for mid-volume applications

FPGA Vendors allow “hard copy” versions of their FPGAs
IC Packages

- ICs are encapsulated in protective packages
  - External pins for connected to circuit board
  - Bond-wires or flip-chip connections
Printed Circuit Boards (PCBs)

- Layers of conducting wires (copper) between insulating material (fiberglass)
  - Manufactured using photolithography and etching
- Wires interconnect ICs and other components
  - External connections to other system components
Through-Hole PCBs

- IC package pins pass through drilled holes
  - Soldered to PCB wires that join the hole
Surface Mount PCB

- IC package pins soldered to wires on PCB surface
- Packages and PCB features are generally smaller than through-hole
Multichip Modules (MCMs)

- Several ICs on a ceramic carrier
  - Can also include thin-film passives and discrete components
  - External connections for PCB mounting

- Ideal for high-density applications
  - E.g., cell phones
Signal Integrity

- Signals propagate over bond wires, package pins, PCB traces
  - Various effects cause distortion and noise
  - Signal integrity: minimizing these effects
- Propagation delay in PCB trace
  - $\approx \frac{1}{2}c \Rightarrow \approx 150\text{mm/\text{ns}}$ ($\approx 5.9\text{ in/\text{ns}} : c=>\approx 1\text{ft/\text{ns}} : 0.98\text{ ft/\text{ns}}$)
- If two traces differ in length
  - Skew at arrival point can be significant
  - Careful PCB design needed
Ground Bounce

- Transient current flows when an output switches logic level
  - Parasitic inductance causes voltage shift on power supply & ground signals
  - Spikes on other drivers
  - Threshold shift on receivers
Minimizing Bounce

- Bypass capacitors between ground and +V
  - 0.01µF – 0.1µF, close to package pins
- Separate PCB planes for ground and +V
- Limit output slew rate
  - Trade off against propagation delay
Transmission Line Effects

- Occur when rise time is comparable to path delay
  - Reflections interfere with transitions, resulting in under/overshoot and ringing
  - Can cause false/multiple switching
  - Use PCB layout techniques to minimize effects
Electromagnetic Interference

- Transitions cause electromagnetic fields
  - Energy radiated from PCB traces
  - Induces noise in other systems
  - Subject to regulation

- Crosstalk
  - Radiation to other traces in the system
    - Particularly adjacent parallel traces
  - PCB layout and slew-rate limiting can minimize both
Differential Signaling

- Reduces susceptibility to noise
- Transmit a signal \( (S_P) \) and negation \( (S_N) \)
  - At receiver, sense difference between them
  - \( S_P - S_N \)
- Noise induced on both \( S_P \) and \( S_N \)
  - \( (S_P + V_{\text{Noise}}) - (S_N + V_{\text{Noise}}) = S_P - S_N \)
Summary

- Exponential improvements in IC manufacturing
- SSI and MSI TTL logic families
- ASICs: full-custom and standard cell
- PALs, CPLDs, FPGAs, platform FPGAs
- IC packages for PCB assembly
  - Through-hole and surface mount
- Signal integrity