EELE 461 / EELE561 - Digital System Design
3 Credits, Spring Semester, 2012
Department of Electrical & Computer Engineering
Montana State University
Bozeman, MT

Description: This course introduces students to the physical phenomena that lead to signal degradation when generating and transmitting digital signals. The broadband response of transmission lines will be presented in addition to lumped versus distributed analysis. Emphasis is placed on the physical structures that are used to construct modern digital systems (on-chip Rx/Tx circuitry, on-chip interconnect, IC packaging, PCB's, connectors, and cables). The fabrication process for each component of the digital system will be presented in addition to the tradeoffs between mechanical reliability, cost, and electrical performance. Modern analysis tools will be used to explore these topics including SPICE circuit simulators, EM field solvers, and PCB design/layout software. Modern test equipment will also be presented including Time Domain Reflectrometry (TDR), Vector Network Analysis (VNA), and Jitter Characterization using Real-Time Digital Oscilloscopes.

Outcomes: At the end of this course the student should be able to:

1) Design and analyze a digital chip-to-chip link.
2) Analyze the transmission line behavior when stimulated with a digital signal.
3) Analyze the cross-talk between signal lines in a digital system.
4) Describe the construction of a Printed Circuit Board.
5) Use modern CAD tools to create PCB schematics and layout.
6) Describe the construction of an Integrated Circuit package.
7) Use modern CAD tools to extract the electrical parameters of an interconnect structure.
8) Use modern CAD tools simulate the performance of a digital link.
9) Use a TDR oscilloscope to measure impedance discontinuities in a transmission line.

Instructor:
Dr. Brock J. LaMeres
533 Cobleigh Hall
Department of Electrical & Computer Engineering, MSU
406-994-5987
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Time & Location: MWF, 9:00am – 9:50am,
110 EPS

Required Text: *"Signal& Power Integrity - Simplified"*
Eric Bogatin
Prentice Hall PTR, 2nd edition, 2009.

Website: www.coe.montana.edu/ee/lameres/courses/eele461_spring12

The website will be the main source of information for the course. All handouts, homework, and announcements will be posted. It is the student's responsibility to download and print the necessary documents needed in the course.

Office Hours: Check instructor website for most recent schedule.

Requisites: Pre-requisite(s): EE308, EE334, EE371

Grading:

Distribution	
Homework	- 25%
Exam #1	- 25%
Exam #2	- 25%
Final Project	- 25%

Letter Assignment	
90% - 100%	= A
80% - 89%	= B
70% - 79%	= C
60% - 69%	= D
0% - 59%	= F

Notes:
- Instructor reserves the right to apply a grading curve and to assign +/-'s to grades as appropriate.
- Homework is due at the beginning of class. Late Assignments can be turned in up to one week after the due date to receive up to 50% credit. Assignments over one week late will not receive credit.
- No make up exams will be given. Make plans to attend the scheduled exams.

Labs: We will periodically meet in Cobleigh Hall 601to have a lab instead of a lecture. The purpose of the lab is to familiarize the students with modern CAD tools (simulation, PCB layout, etc...). During each lab, we will walk through how to use a CAD tool. The students will be given a short assignment that they will have to complete using the CAD tool. Most laboratory assignments can be completed during the lab period.

Project: During the first half of the semester, weekly homework assignments will be given. During the second half of the semester, a design project will be assigned. The project will incorporate all of the signal integrity theory that we have learned in class.

EE 561: This is a 400/500 level co-convened course. EE561 students will do all of the same homework problems that EE461 students do in addition to a weekly research assignment. The research assignment will be listed on the homework assignment. EE561 students will also have a research component to their design project. Both EE461 and EE561 will take the same two exams.

General Outline:

1) Digital System Signaling Overview, Logic Levels, Analog Behavior of digital signals.
2) Rx/Tx On-Chip Circuitry Design and Fabrication
3) On-Chip Interconnect Design and Fabrication
4) IC Package Design and Fabrication, Inductance, Ground Bounce
5) PCB Design and Fabrication
6) Design Tools, PADs PCB Design/Layout
7) Electromagnetism, Lumped vs. Distributed Systems, Reflections, Fourier Series of Digital Pulse
8) Simulation Tools: ADS SPICE Simulator
9) Impedance, Termination Schemes, X-talk, ISI, Even and Odd Mode Impedance
10) Return Current, Ground Bounce, Simultaneous Switching Noise (SSN)
11) Power Distribution, Decoupling, Noise Analysis, Jitter, Eye Diagrams, Random vs. Deterministic
12) Simulation Tools, ADS 2D/3D Field Solver
13) Bus Architectures, Synchronous, Source-Synchronous, Embedded Clock
14) Advanced Signaling, Pre/Post Emphasis, Differential vs. Signal End, Cost Trade-offs
15) Test Equipment, Time Domain Reflectrometry, Vector Network Analysis, Jitter

Academic Policies: This course will follow the policies outlined in the *Conduct Guidelines and Grievance Procedures for Students" (http://www2.montana.edu/policy/student_conduct/)* and the *MSU Policy and Procedures Manual* (http://www2.montana.edu/policy/) . Please consult these documents on policies regarding academic honesty, student and instructor rights, and general standards of conduct.