Brock J. LaMeres
Agilent Technologies

“RF Effects in PCB Design”

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Topics:

1) Printed Circuit Board Via
2) Bandwidth Estimation
3) Effect of Via on Bandwidth
PCB Bandwidth Estimation
(Background)

- The overall risetime of a system is the RMS average of all risetimes in the system:

\[ t_{\text{system}} = \sqrt{t_1^2 + t_2^2 + t_3^2} \]

Risetime to Bandwidth Conversion
(Risetime BW Product)

\[ t_{\text{RISE}} \times BW = 0.35 \]
PCB Bandwidth Estimation
(Background)

- The MAXIMUM Toggle rate of a digital system is:

\[ f_{\text{max}} = \frac{0.35}{t_{\text{RISE}}} \]

Time Constant to Risetime Conversion

\[ t_{\text{RISE}} = 2.2 \times \text{Tau} \]

(Tau = RC or ZC)
Parallel Termination Example

$t_{\text{driver}} = 400 \ \text{ps}$

$Z_0 = R_L = 50 \ \Omega$

$C_L = 6 \ \text{pF}$

$\tau_{\text{load}} = \left( \frac{50}{50} \right) \times 6 \ \text{pF} = 150 \ \text{ps}$

$\text{trise(} \text{load}) = 2.2 \times (150 \ \text{p}) = 330 \ \text{ps}$

$t_{\text{system}} = \sqrt{(400 \ \text{p})^2 + (330 \ \text{p})^2} = 519 \ \text{ps}$

$f_{\text{max}} = \frac{0.35}{519 \ \text{p}} = 674 \ \text{MHz}$
Series Termination Example

$t_{\text{driver}} = 400$ ps
$Z_0=R_L=50$ Ω
$C_L=6$ pF

$\tau_{\text{load}} = (50)\times 6p = 300$ ps
$\text{trise(\text{load})} = 2.2\times (300p) = 660$ ps
$t_{\text{system}} = \sqrt{(400p)^2 + (660p)^2} = 772$ ps
$f_{\text{max}} = \frac{0.35}{772p} = 454$ MHz
PCB Bandwidth Estimation  
(Series vs. Parallel Termination)

Addition of a Via

\[ t_{driver} = 400 \text{ ps} \]
\[ Z_0=R_L=50 \ \Omega \]
\[ C_L=6 \ \text{pF} \]
\[ C_{via} = 1\ \text{pF} \]

\[ \tau_{(load)} = (50)*6p = 300 \text{ ps} \]
\[ t_{rise}(load) = 2.2*(300p) = 660 \text{ ps} \]

\[ \tau_{(via)} = (50)*1p = 50 \text{ ps} \]
\[ t_{rise}(via) = 2.2*(50p) = 110 \text{ ps} \]

\[ t_{system} = \sqrt{(400p)^2 + (660p)^2 + (110p)^2} = 780 \text{ ps} \]

\[ f_{max} = \frac{0.35}{780p} = 448 \text{ MHz} \]

- a loss of 7MHz due to the via
PCB Bandwidth Estimation  
(Compensation)

1) An inductor can be used in series with a capacitive load to raise the load impedance.

2) The ground plane clearance can be backed off around a via to make it look less capacitive.
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Comments or Question?