Compensation for Simultaneous Switching Noise in VLSI Packaging

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Problem Statement

• Package Interconnect Limits VLSI System Performance

• The three main components of this are:

  1) Cost
  2) Power Delivery
  3) Signal Path Reflections
Agenda

• Current Problems
• Current Solutions
• Proposed Solutions
• Case Study of Proposed Solutions
Why is packaging limiting performance?

Transistor Technology is Outpacing Package Technology
Problem #1 - Cost

1) Cost
- IC core technology is increasing faster than package technology.
- Simply adding I/O on the package to keep up with core speeds is too expensive.

Example:
- 64-bit data bus
  - on chip = (4GHz)*(64)
  = 256 Gb/s
- I/O needed = (256G)/(400M)
  = 640
- 4:1:1 Pwr/Gnd
  = 640+160+160
  = 960
  (just for the data bus)
Problem #1 - Cost

1) Cost cont...

- Aggressive Package Design will increase the data rates of the package
- But it is too expensive for mainstream designs
- 95% of VLSI design-starts are wire-bond

QFP – Wire Bond : $0.22 / pin

BGA – Wire Bond : $0.34 / pin (Dominant)

BGA – Flip-Chip : $0.63 / pin
Problem #1 - Cost

1) Cost cont...

- The Desired Solution:

  A) Make Existing Package Technology Go Faster

  B) Postpone Advanced Packaging Leap as long as possible

“Today’s Package of Choice”

Level 1: Wire Bond

Level 2: BGA
Problem #2 – Power Delivery

2) Power Delivery
- Modern IC’s require large amounts of instantaneous current ($P_4 = 80\text{Amps}$)
- The package interconnect has inductance that causes voltage noise.
- The wire bond is the largest source of inductance.

Wire Bond Inductance (~2.8nH)
Solder Ball Inductance (~0.2nH)
Problem #2 – Power Delivery

2) Power Delivery cont…

- The voltage noise causes ground bounce and power supply droop.
- These effects cause unwanted switching and slow performance.
- The problem is amplified when many signals switch at the same time.
- This is called **Simultaneous Switching Noise (SSN)**

\[ V_{\text{Noise}} = L \left( \frac{di}{dt} \right) \]
Problem #2 – Power Delivery

2) Power Delivery cont…

- The Desired Solution:

  A) Use Existing Package Technology to Deliver Power

  B) Postpone Advanced Packaging Leap as long as possible
Problem #3 – Reflections

3) Signal Path Reflections

- Typical Motherboards and Packages use 50Ω transmission lines.
- The package interconnect has excess inductance that looks >50Ω’s.
- This causes reflections due to impedance mismatch.
Problem #3 – Reflections

3) Signal Path Reflections cont...
- Reflections cause unwanted switching
- Reflections slow down rise times

\[
\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}
\]

The Reflection due to the Wire-Bond:

\[Z_L = \text{Wire Bond Impedance}\]
\[Z_0 = 50\Omega\]
Problem #3 – Reflections

3) Signal Path Reflections cont…

- The Desired Solution:

A) Use Existing Package Technology to Transmit Signals

B) Postpone Advanced Packaging Leap as long as possible
Problem

Why is packaging an electrical issue now?

**Cost**

Historically, the transistor delay has dominated performance, not packaging. Inexpensive packaging has met the electrical performance needs.

**Power Delivery**

As transistors shrink, more can be put on an IC and they can run faster. This means today more power is being consumed in less time.

**Impedance Matching**

Today’s rise times are fast enough so that Packages must be treated as transmission lines. Until recently, we didn’t care about impedance.
Current Solution #1 - Cost

Continue to use Wire-Bonding

1) Use Standard VLSI Processes to Increase Performance of Wire-Bonded BGA Packaging
Current Solution #1 - Cost

Limitations of Approach

1) Use Standard VLSI Processes to Increase Performance of Wire-Bonded BGA Packaging

- Modern IC’s only implement low-risk solutions
- Advanced techniques are not in use yet.
Current Solution #2 – Power Delivery

Use Redundant Wire Bonds in Power/Ground Path

1) Wire Bonds in Parallel Reduce the Total Inductance

\[ L_{Total} = \frac{L_{wb}}{n_{wb}} \quad \implies \quad V_{Noise} = L_{Total} \left( \frac{di}{dt} \right) \]

Many Wire Bonds in Parallel to Carry Power
Current Solution #2 – Power Delivery

Use Bypass Capacitors to Provide Instantaneous Current

2) On-Chip Capacitance Provides Current Blocked by Wire-Bond
3) On-Mother Board Capacitance Provides Current Blocked by Planes

\[ I_{Cap} = C \left( \frac{dv}{dt} \right) \]
Current Solution #2 – Power Delivery

Limitations of Approach

1) Wire Bonds in Parallel Reduce the Total Inductance
   • The total number of wires is limited by die size

2) On-Chip Capacitance Provides Current Blocked by Wire-Bond
   • We want as much as possible, limited by die size

3) On-Mother Board Capacitance Provides Current Blocked by Planes
   • Adding discrete components adds cost
Current Solution #3 – Reflections

Live with the Signal Path Reflections

1) Run the signals slow enough so that reflections are small

\[ \Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} < 10\% \]

2) Terminate Signals on the Mother board so that reflections are absorbed

On Mother Board Termination
Current Solution #3 – Reflections

Limitations of Approach

1) Run the signals slow enough so that reflections are small
   • Limits System Performance

2) Terminate Signals on the Mother board so that reflections are absorbed
   • This only eliminates secondary reflections, the primary still exists
Proposed Solutions – Power Delivery 1

1) Use Device-Based Capacitors Beneath Wire-Bond Pads

A) Placing capacitors beneath the bond wire pad eliminates impact on circuit area

- Area beneath the wire bond pads is typically not used.
- Today’s processes have proved that this area is in fact useable.
- Using this area is effectively “free” and doesn’t impact circuitry
Proposed Solutions – Power Delivery 1

1) Use Device-Based Capacitors Beneath Wire-Bond Pads cont…

B) Placing beneath the bond wire pad is the optimal location

- We want the capacitor as close as possible to the bond wire inductance.
- This is the closest that we can get it.
Proposed Solutions – Power Delivery 1

1) Use Device-Based Capacitors Beneath Wire-Bond Pads cont…

C) Device-based (PolySilicon) capacitors are the highest density on-chip capacitors

• Device-Based = 13 fF/um²
• MIM-Based = 1.1 fF/um²
Proposed Solutions – Power Delivery 2

2) Use Embedded Capacitance on Package

- Using plane-to-plane capacitance on the package for additional bypassing

- Modern Packages can achieve plane-to-plane separations of $t=0.002"$
- This translates to $0.64pF/mm^2$
- For a 0.8”x0.8” package, this can mean an additional 256pF
3) Encode the Data to Avoid Worst Case Switching Pattern

- Getting rid of worst case switching patterns reduces max voltage noise.
- The off-chip bus can actually run faster encoded.
- The increase in encoded bus speed makes up for smaller symbol set.

\[
\text{Throughput of less vectors at higher data-rate} \quad \text{\quad} \quad \quad \quad \quad \text{\quad Throughput of more vectors at lower data-rate}
\]
Proposed Solutions – Power Delivery 3

3) Encode the Data to Avoid Worst Case Switching Pattern

ex) - 3-bit bus
- worst case SSN is on the transitions:

\[ 000 \Rightarrow 111 \quad \text{and} \quad 111 \Rightarrow 000 \]

- add encoder circuit to eliminate these transitions.
- the new data bus has less possible transitions but can run faster
- the increase in speed outweighs the reduction in transitions
Proposed Solutions – Reflections 1

1) Add Capacitance Near Bond Wire to Reduce Impedance

- adding addition capacitance lowers the wire bond’s impedance.
- matching the bond wire impedance to the system (50Ω’s) reduces reflections.

\[ Z_{\text{WireBond}} = \sqrt{\frac{L_{\text{WireBond}}}{C_{\text{WireBond}}}} \]

Add Capacitance to lower Z
Proposed Solutions – Reflections 2

2) Using Static Capacitance Before and After the Bond Wire

- Use embedded capacitors on the package before the wire bond.
- Use On-Chip MIM capacitors after the wire bond.

\[ Z_{WireBond} = \sqrt{\frac{L_{WB}}{C_{WB} + C_{pkg} + C_{MIM}}} = 50\Omega's \]
Proposed Solutions – Reflections 3

3) Using On-Chip Dynamic Capacitance near the Bond Wire

- A programmable capacitor circuit is placed beneath the wire-bond pad.
- The programmable range of the circuit covers wire bond variation.

On-Chip Programmable Compensation

\[ Z_{\text{WireBond}} = \sqrt{\frac{L_{\text{WB}}}{C_{\text{WB}} + C_{\text{Comp}}}} = 50 \Omega's \]
Proposed Solutions – Reflections 3

3) Using On-Chip Dynamic Capacitance near the Bond Wire cont…

- A programmable capacitor circuit is placed beneath the wire-bond pad.
- The programmable range of the circuit covers wire bond variation.
CASE STUDY

- A Modern BGA Package using Wire-Bond

- 340 I/O:
  - 60 Ground, 60 Power, 110 Input, 110 Output
- 1mm Pitch BGA:
  - 340 Controlled Collapse Solder Balls
- 125um Pitch Gold Bonds:
  - 100um x 100um On-Chip Ball Pads (dual row)
  - 100um x 400um On-Package Wedge Pads
  - 5mm Gold Wire Bond (diameter=25um)
CASE STUDY – Electrical Modeling

- Electrical Parameters are Extracted using EM Field Solver
- Values are then used in SPICE Simulations

**Wire Bond Example**

<table>
<thead>
<tr>
<th>Length</th>
<th>L</th>
<th>C</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>1mm</td>
<td>0.569nH</td>
<td>26fF</td>
<td>148Ω</td>
</tr>
<tr>
<td>2mm</td>
<td>1.138nH</td>
<td>52fF</td>
<td>148Ω</td>
</tr>
<tr>
<td>3mm</td>
<td>1.707nH</td>
<td>78fF</td>
<td>148Ω</td>
</tr>
<tr>
<td>4mm</td>
<td>2.276nH</td>
<td>104fF</td>
<td>148Ω</td>
</tr>
<tr>
<td>5mm</td>
<td>2.845nH</td>
<td>130fF</td>
<td>148Ω</td>
</tr>
</tbody>
</table>
CASE STUDY – Power Delivery 1

- Using On-Chip Device-Based Capacitance Beneath Wire Bond Pads

![Graphs showing current and voltage with waveform data](image)

2Gb/s Signal, 3Amp Peak

On-Chip Load

On-Chip Supply Voltage

Reduced from 10mV to 5mV
CASE STUDY – Power Delivery 2

• Adding On-Package Embedded Capacitance also

On-Chip Capacitance Only

On-Chip + On-Package

Reduced from 5mV to 3mV
CASE STUDY – Power Delivery 3

- **Encoding Data to Avoid Worst Case Patterns**
  (3-bit bus example)

1) Original Bus (un-encoded)
   - allowing all transitions
   - max per-pin toggle rate = 222 Mb/s
   - effective bus size = 3
   - Throughput = \((3 \times 222M)\)
     \[= 666 \text{ Mb/s}\]

2) Encoded Bus
   - eliminating \(000 \Rightarrow 111\) and \(111 \Rightarrow 000\)
   - max per-pin toggle rate = 617 Mb/s
   - effective bus size = 2
   - Throughput = \((2 \times 617M)\)
     \[= 1234 \text{ Mb/s}\]

Ground Bounce

September 15, 2005

“Compensation of SSN in VLSI Packaging”
CASE STUDY – Reflections 1

- Adding Static (fixed) Capacitance on both sides of wire-bond
  - Embedded Capacitance On Package
  - MIM Capacitance On-Chip
  - 3mm Wire Bond Example:

1) No Static Capacitance
   - Reflection due to wire-bond = 14%

2) With Static Capacitance
   - Reflection w/ Static Capacitance = 3%

Reflections (entire package)
CASE STUDY – Reflections 1

• Adding Static (fixed) Capacitance on both sides of wire-bond
  - Embedded Capacitance On Package
  - MIM Capacitance On-Chip
  - 3mm Wire Bond Example:

1) No Static Capacitance
   - Discontinuity > 10Ω = 850MHz

2) With Static Capacitance
   - Discontinuity > 10Ω = 3GHz

Input Impedance
(whole package)
CASE STUDY – Reflections 2

- Adding Dynamic (programmable) Capacitance on-chip
  - Device-Based Compensator Outperforms MIM-Based
  - 1mm to 5mm Wire Bond Range:

**Reflections (wire-bond)**

<table>
<thead>
<tr>
<th>Length</th>
<th>Γ-orig</th>
<th>Γ-comp</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>1mm</td>
<td>4.5%</td>
<td>1.0%</td>
<td>001</td>
</tr>
<tr>
<td>2mm</td>
<td>8.7%</td>
<td>1.3%</td>
<td>010</td>
</tr>
<tr>
<td>3mm</td>
<td>12.7%</td>
<td>3.0%</td>
<td>011</td>
</tr>
<tr>
<td>4mm</td>
<td>16.4%</td>
<td>3.3%</td>
<td>101</td>
</tr>
<tr>
<td>5mm</td>
<td>19.8%</td>
<td>5.0%</td>
<td>111</td>
</tr>
</tbody>
</table>

**Dynamic Compensation Holds reflections for all lengths to 5%**
CASE STUDY – Reflections 2

• Adding Dynamic (programmable) Capacitance on-chip
  - Device-Based Compensator Outperforms MIM-Based
  - 3mm Wire-Bond Example:

**Input Impedance (wire bond)**

1) No Dynamic Capacitance
   - Discontinuity > 10Ω
   - Frequency = 3GHz

2) With Dynamic Capacitance
   - Discontinuity > 10Ω
   - Frequency = 7GHz
Summary

• Package Interconnect is now the limiting factor in VLSI Performance

• The move toward Advanced Packaging is Resisted due to Cost

• VLSI Designers are looking for techniques to increase current package performance without adding cost

• Adding On-Chip circuitry does not add cost and is the desired solution
Summary

• Potential Solutions to increase Existing Package Technology

Power Delivery

1) On-Chip Device-Based Capacitance Under Wire Bond Pads
2) Embedded Capacitance on the Package
3) Encoding Data to Avoid Worst Case SSN Patterns

Reflections

1) Adding Static Capacitance to Package and IC
2) Adding Dynamic Capacitance to IC
Questions?