Reconfigurable Space Computing

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1. Research Statement
   • Enabling Reconfigurable Computing for Aerospace

2. Radiation Effects in Electronics
   • Sources & Types of Radiation
   • Effects (TID, SEE, Displacement Damage)
   • FPGA Specific Effects

3. Existing Mitigation Techniques
   • Physical (Shielding, RHBD, RHBP)
   • Architectural (TMR, Scrubbing, Error Correction Codes)

4. MSU’s Approach
   • Redundant Tiles (TMR+Spares+Scubbing)
   • Prototyping
   • Test Flights (Local Balloons, HASP, Future Sub-orbital)
Support the Computing Needs of Space Exploration & Science

- Computation (2,000 MIPs)
- Power Efficiency (200 MIPs/Watt)
- Mass ($100/lb by 2025)
- Reliability (99.99999% reliable, instant recovery during critical operation)
Provide a Radiation Tolerant Platform for Reconfigurable Computing

- Reconfigurable Computing as a means to provide:
  - Increased Computation of Flight Systems
  - Reduced Power of Flight Systems
  - Reduced Mass of Flight Hardware
  - Mission Flexibility through Real-Time Hardware Updates
- Support FPGA-based Reconfigurable Computing through an underlying architecture with inherent radiation tolerance to Single Event Effects

The Future

The Problem
What is Reconfigurable Computing?

Let’s start with what is NOT Reconfigurable Computing

- A CPU/GPU – while you have flexibility via programming, the hardware is still fixed
  - The instructions that can be executed are fixed in the sequence controller
  - The size of memory is pre-defined
  - The IO is pre-defined
- An ASIC – the hardware is fixed during fabrication.

Are There Advantages to these Conventional Systems?

- Yes, they are well understood and easy to program (particularly the single core model)
- Yes, when the task maps well to the hardware, they have high performance (e.g., GPU)
- Yes, they can handle a large array of tasks (albeit sometimes in an inefficient manner)

Are There Disadvantages to these Conventional Systems?

- Yes, unless the task does not map directly to the hardware, they perform poorly.
- Yes, much of the hardware that allows them to handle a variety of tasks sits idle most of the time.
A System That Alters Its Hardware as a **Normal Operating Procedure**

- This can be done in real-time or at compile time.
- This can be done on the full-chip, or just on certain portions.
- Changing the hardware allows it to be optimized for the application at hand.
What Technology is used for RC?

Field Programmable Gate Arrays (FPGA)

- Currently the most attractive option.
- SRAM-based FPGAs give the most flexibility
- Riding Moore’s Law feature shrinkage
What are the Advantages of RC?

Computational Performance
- Optimizing the hardware for the task-at-hand = architectural advantages
- Eliminating unused circuitry (minimize place/route area, reduces wiring delay)

Reduced Power
- Implement only the required circuitry
- Shutdown or un-program unused circuitry when not in use

Reduced Mass
- Reuse a common platform to conduct multiple sequential tasks in flight systems
- This effect is compounded when considering each flight system has backup hardware
- Mass is the dominant driver of cost for space applications
  - $10,000/lb to get into orbit.
  - NASA’s goal is $100/lb by 2025
  - Shuttle cost ~$300-$500M per launch with 50,000 lb capacity
Radiation Effects on Electronics

On Earth Our Computers are Protected
  - Our magnetic field deflects the majority of the radiation
  - Our atmosphere attenuates the radiation that gets through our magnetic field

Our Satellites Operate In Trapped Radiation in the Van Allen Belts
  - High flux of trapped electrons and protons

In Deep Space, Nothing is Protected
  - Radiation from our sun
  - Radiation from other stars
  - Particles & electromagnetic
Where Does Space Radiation Come From?

- Nuclear fusion in stars creates light and heavy ions + EM
- Stars consists of an abundant amount of Hydrogen ($^1\text{H} = 1 \text{ Proton}$) at high temperatures held in place by gravity

1. The strong nuclear force pulls two Hydrogen ($^1\text{H}$) atoms together overcoming the Columns force and fuses them into a new nucleus
   - The new nucleus contains 1 proton + 1 neutron
   - This new nucleus is called Deuterium ($D$) or Heavy Hydrogen ($^2\text{H}$)
   - Energy is given off during this reaction in the form of a Positron and a Neutrino

2. The Deuterium ($^2\text{H}$) then fuses with Hydrogen ($^1\text{H}$) again to form yet another new nucleus
   - This new nucleus contains 2 protons + 1 neutron
   - This nucleus is called Tritium or Hydrogen-3 ($^3\text{H}$)
   - Energy is given off during this reaction in the form of a Gamma Ray

3. Two Tritium nuclei then fuse to form a Helium nucleus
   - The new Helium nucleus ($^4\text{H}$) contains 2 protons + 2 neutrons
   - Energy is given off in the form of Hydrogen (e.g., protons)
Radiation Categories

1. Ionizing Radiation
   - Sufficient energy to remove electrons from atomic orbit
   - Ex. High energy photons, charged particles
2. Non-Ionizing Radiation
   - Insufficient energy/charge to remove electrons from atomic orbit
   - Ex., microwaves, radio waves

Types of Ionizing Radiation

1. Gamma & X-Rays (photons)
   - Sufficient energy in the high end of the UV spectrum
2. Charged Particles
   - Electrons, positrons, protons, alpha, beta, heavy ions
3. Neutrons
   - No electrical charge but ionize indirectly through collisions

What Type are Electronics Sensitive To?

- Ionization which causes electrons to be displaced
- Particles which collide and displace silicon crystal
Classes of Ionizing Space Radiation

1) Cosmic Rays
2) Solar Particle Events
3) Trapped Radiation
Classes of Ionizing Space Radiation

1. Cosmic Rays
   - Originating for our sun (Solar Wind) and outside our solar system (Galactic)
   - Mainly Protons and heavier ions
   - Low flux

2. Solar Particle Events
   - Solar flares & Coronal Mass Ejections
   - Electrons, protons, alpha, and heavier ions
   - Event activity tracks solar min/max 11 year cycle

3. Trapped Radiation
   - Earth’s Magnetic Field traps charged particles
   - Inner Van Allen Belt holds mainly protons (10-100’s of MeV)
   - Outer Van Allen Belt holds mainly electrons (up to ~7 MeV)
   - Heavy ions also get trapped
Which radiation is of most concern to electronics?

**Concern**

- Protons ($^1H$)
  - Makes up ~85% of galactic radiation
  - Larger Mass than electron (1800x), harder to deflect

- Beta Particles (electrons & positrons)
  - Makes up ~1% of galactic space
  - More penetrating than alphas

- Heavy Ions
  - Makes up <1% of galactic radiation
  - High energy (up to GeV) so shielding is inefficient

- Neutrons
  - Uncharged so difficult to stop

**No Concern**

- Alpha Particles (He nuclei)
  - Makes up ~14% of galactic radiation
  - ~ 5MeV energy level & highly ionizing but...
    - Low penetrating power
      - (50mm in air, 23um in silicon)
    - Can be stopped by a sheet of paper

- Gamma
  - Highly penetrating but an EM wave
  - Lightly ionizing
Radiation Effects on Electronics

What are the Effects?

1. Total Ionizing Dose (TID)
   - Cumulative long term damage due to ionization.
   - Primarily due to low energy protons and electrons due to higher, more constant flux, particularly when trapped
   - Problem #1 – Oxide Breakdown
     » Threshold Shifts
     » Leakage Current
     » Timing Changes

- Hole Trapping
  - EHP formed by ionization
  - Electrons recombine quicker due to faster mobility
  - Holes get “stuck” due to lower mobility
  - Lowers $V_T$ by effectively “thinning” the oxide
  - $V_T$ eventually goes negative turning on MOS

- Interface Trapping
  - The Si/SiO$_2$ interface typically contains Si/H bonds
  - This is due to the annealing process in hydrogen
  - When this bond is severed, H will bond with itself
  - This leaves a dangling Si bond with net positive charge
  - This initially lowers $V_T$ and then ultimately raises it
Radiation Effects on Electronics

What are the Effects?

1. Total Ionizing Dose (TID) Cont...

   ○ Problem #2 – Leakage Current
     
     » Hole trapping slowly “dopes” field oxides to become conductive
     
     » This is the dominant failure mechanism for commercial processes
2. Single Event Effects (SEE)
   - Electron/hole pairs created by a single particle passing through semiconductor
   - Primarily due to heavy ions and high energy protons
   - Excess charge carriers cause current pulses
   - Creates a variety of destructive and non-destructive damage
   - The ionization *itself* does not cause damage, the damage is secondary due to parasitic circuits

   “Critical Charge” = the amount of charge deposited to change the state of a gate
Radiation Effects on Electronics

What are the Effects?

2. Single Event Effects (SEE) - **Non-Destructive** (e.g., soft faults)

**Single Event Transients (SET)**
- An induced pulse that can flip a gate
- Temporary glitches in combinational logic

**Single Event Upsets (SEU)**
- The pulse is captured by a storage device resulting in a state change
Radiation Effects on Electronics

What are the Effects?

2. Single Event Effects (SEE) - **Non-Destructive** (e.g., soft faults)

**Multiple Bit Upsets (MBU)**
- A single particle causes multiple SEUs due to its path being non-orthogonal

**Single Event Functional Interrupt (SEFI)**
- The system is put into a state that causes function failure
  - Typically requires reset, power cycle or reprogramming
What are the Effects?

2. Single Event Effects (SEE) – **Destructive** (e.g., hard faults)

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**Single Event Latchup (SEL)**
- Parasitic NPN/PNP transistors are put into positive feedback condition (PNPN).
- Runaway current damages device.
- Due to heavy ions, protons, neutrons.

**Single Event Burnout (SEB)**
- Localized current in body of device turns on parasitic bipolar transistors.
- Runaway current causes heat.
- Due primarily to heavy ions.

**Single Event Gate Rupture (SEGR)**
- Permanent short through gate oxide due to hole trapping.
- Thin oxides are especially immune.
- Due to heavy ions.
Current Mitigation Techniques

Shielding

- Shielding helps for protons and electrons <30MeV, but has diminishing returns after 0.25”.
- This shielding is typically inherent in the satellite/spacecraft design.

![Graph showing Shield Thickness vs. Dose Rate (LEO)]
Current Mitigation Techniques

Radiation Hardened by Design (RHBD)

- Uses commercial fabrication process
- Circuit layout techniques are implemented which help mitigate effects

Enclosed Layout Transistors
- Eliminates edge of drain terminal
- This eliminates any leakage current between source & drain due near edge of gate (STI Region 1)

Guard Rings
- Reduces leakage between NMOS & PMOS devices due to hole trapping in Field Oxide (STI Region 2)
- Separation of device + body contacts
- Adds ~20% increase in area

Thin Gate Oxide
- This oxide reduces probability of hold trapping.
- Process nodes <0.5um typically are immune to Vgs shift in the gate.
Current Mitigation Techniques

**Radiation Hardened by Process (RHBP)**

- An insulating layer is used beneath the channels
- This significantly reduces the ion trail length and in turn the electron/hole pairs created
- The bulk can also be doped to be more conductive so as to resist hole trapping
1. Triple Module Redundancy
   o Triplicate each circuit
   o Use a majority voter to produce output
   o Advantages
     » Able to address faults in real-time
     » Simple
   o Disadvantages
     » Takes >3x the area
     » Voter needs to be triplicated also to avoid single-point-of-failure
     » Doesn’t handle Multiple-Bit-Upsets
Current Mitigation Techniques

Radiation Tolerance Through Architecture Cont...

2. Scrubbing
   - Compare contents of a memory device to a “Golden Copy”
   - Golden Copy is contained in a radiation immune technology (fuse-based memory, MROM, etc…)
   - Advantages
     » Simple & Effective
   - Disadvantages
     » Sequential searching pattern can have latency between fault & repair
Current Mitigation Techniques

Effects Overview

- Primary Concern is Heavy Ions & high energy protons
- All modern computer electronics experience TID and will eventually go out
- Heavy Ions causing SEEs cannot be stopped and an architectural approach is used to handle them.
Our Approach

FPGAs are Uniquely Susceptible

1. Total Ionizing Dose
   - All gates and memory cells are susceptible to TID due to high energy protons

2. Single Event Effects
   - SETs/SEUs in the logic blocks
   - SETs in the routing
   - SEUs in the configuration memory for the logic blocks (SEFI)
   - SEUs in the configuration memory for the routing (SEFI)
Our Approach

What is needed for FPGA-Based Reconfigurable Computing

1. SRAM-based FPGAs
   - To support fast reconfiguration

2. A TID hardened fabric
   - Thin Gate Oxides to avoid hole trapping and threshold shifting (inherent in all processes)
   - Radiation Hardened by Design to provide SEL immunity (rings, layout, etc…)

Does This Exist?

1. Yes, Xilinx Virtex-QV Space Grade FPGA Family
   - TID Immunity > 1Mrad
   - RHBD for SEL immunity
   - CRC in configuration memory

The Final Piece is SEE Fault Mitigation due to Heavy Ions

- SEU will happen due to heavy ions, nothing can stop this.
- A computer architecture that expects and response to faults is needed.
Our Approach

A Many-Tile Architecture

- The FPGA is divided up into *Tiles*
- A Tile is a quantum of resources that:
  - Fully contains a system (e.g., processor, accelerator)
  - Can be programmed via partial reconfiguration (PR)

Fault Tolerance

1. TMR + Spares
2. Spatial Avoidance and Background Repair
3. Scrubbing

16 MicroBlaze Soft Processors on a Virtex-6
Our Approach

1. **TMR + Spares**
   - 3 Tiles run in TMR with the rest reserved as spares.
   - In the event of a fault, the damaged tile is replaced with a spare and foreground operation continues.

2. **Spatial Avoidance & Repair**
   - The damaged Tile is “repaired” in the background via Partial Reconfiguration.
   - The repaired tile is reintroduced into the system as an available spare.

3. **Scrubbing**
   - A traditional scrubber runs in the background.
   - Either blind or read-back.
   - PR is technically a “blind scrub”, but of a particular region of the FPGA.
Why do it this way?

*With Spares, it basically becomes a flow-problem:*

- If the repair rate is faster than the incoming fault rate, you're safe.
- If the repair rate is slightly slower than the incoming fault rate, spares give you additional time.
- The additional time can accommodate varying flux rates.
- Abundant resources on an FPGA enable dynamic scaling of the number of spares. (e.g., build a bigger tub in real time)
Our Approach

Practical Considerations

• Foreground operation can continue while repair is conducted in the background. Since scrubbing/PR is typically slower than reinitializing a tile, foreground “down time” is minimized.

• Using PR tiles, the system doesn’t need to track the exact configuration memory addresses. Partial bit streams contain all the necessary information about a tile configuration.

• PR of a tile also takes care of both SEUs in the circuit fabric & configuration SRAM so the system doesn’t care which one occurred.

• The “spares” are held in reset to reduce power. This is as opposed to running in N-MR with every tile voting.
Our Approach

Modeling Our Approach

- We need to compare our approach to a traditional TMR+scrubbing system
- We use a Markov Model to predict *Mean-Time-Before-Failure*
  - 16 tile MicroBlaze system on Virtex-6 (3+13)
  - $\lambda$ is fault rate
  - $\mu$ is repair rate
Our Approach

Modeling Our Approach: Fault & Repair Rates

Fault Rate ($\lambda$)
- Derived from CREME96 tool for 4 different orbits
- Used LET fault data from V4

<table>
<thead>
<tr>
<th>Orbit</th>
<th>Average</th>
<th>Worst Week</th>
<th>Peak 5 Minutes</th>
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<td>GEO</td>
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Repair Rate ($\mu$)
- Measured empirically in lab on V6 system

<table>
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<tr>
<th>Clock Rate</th>
<th>Blind</th>
<th>Readback, undamaged</th>
<th>Readback, damaged</th>
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<tbody>
<tr>
<td>25 MHz</td>
<td>2.97</td>
<td>5.31</td>
<td>6.35</td>
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</table>
## Our Approach

### Modeling Our Approach: Results

<table>
<thead>
<tr>
<th>MTBF for Baseline TMR+Scrubbing System (in seconds)</th>
<th>Baseline System</th>
<th>Proposed System</th>
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<tr>
<td>Average</td>
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<td>Peak 5 Min.</td>
</tr>
<tr>
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<tr>
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<tr>
<td>E1P</td>
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<td>1.25E-02</td>
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<tr>
<td>GEO</td>
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<tr>
<td>Blind</td>
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### Improvement

<table>
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<th>Increase in MTBF after Addition of Spares (%)</th>
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<th>Peak 5 Min.</th>
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<td>GEO</td>
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<td>GEO</td>
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<td>1024.00%</td>
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Ok, it looks promising…
Our Approach

Let’s Build It

• Xilinx Evaluation Platforms (Virtex 4/5/6) for Lab Testing

• Custom Virtex-6 platform for Flight Testing
Our Approach

Let’s Fly It

- Local Balloon Flights (MSGC Borealis)
- HASP Program
- Suborbital Vehicle

- 4 Flights in MT to 100k ft in 2011/12
  - Thermal evaluation of form-factor
- 1st test flight in Sept-12
  - 2nd test flight planned Sept-13
- Payload design training (June-12)
  - Flight planned 2013
Conclusion

What is Missing

- Faults in the routing
- MBUs
- Addressing Single-Point-of-Failure

What’s Next

- Collect flight data
- Address above mentioned issues
Questions?
References

Content


Images

- If not noted, images provided by www.nasa.gov or MSU
- Displacement Image 2/3: Vacancy and divacancy (V-V) in a bubble raft. Source: University of Wisconsin-Madison
- RHBD Images: Giovanni Anelli & Alessandro Marchioro, “The future of rad-tol electronics for HEP”, CERN, Experimental Physics Division, Microelectronics Group, [Available Online]:

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