QUICK START GUIDE TO VERILOG
The classical digital design approach (i.e., manual synthesis and minimization of logic) quickly becomes impractical as systems become more complex. This is the motivation for the modern digital design flow, which uses hardware description languages (HDL) and computer-aided synthesis/minimization to create the final circuitry. The purpose of this book is to provide a quick start guide to the Verilog language, which is one of the two most common languages used to describe logic in the modern digital design flow. This book is intended for anyone that has already learned the classical digital design approach and is ready to begin learning HDL-based design. This book is also suitable for practicing engineers that already know Verilog and need quick reference for syntax and examples of common circuits. This book assumes that the reader already understands digital logic (i.e., binary numbers, combinational and sequential logic design, finite state machines, memory, and binary arithmetic basics).

Since this book is designed to accommodate a designer that is new to Verilog, the language is presented in a manner that builds foundational knowledge first before moving into more complex topics. As such, Chaps. 1–6 provide a comprehensive explanation of the basic functionality in Verilog to model combinational and sequential logic. Chapters 7–11 focus on examples of common digital systems such as finite state machines, memory, arithmetic, and computers. For a reader that is using the book as a reference guide, it may be more practical to pull examples from Chaps. 7–11 as they use the full functionality of the language as it is assumed the reader has gained an understanding of it in Chaps. 1–6. For a Verilog novice, understanding the history and fundamentals of the language will help form a comprehensive understanding of the language; thus it is recommended that the early chapters are covered in the sequence they are written.
Acknowledgments

For Kylie. Your humor brings me laughter and happiness every day. Thank you.
# Contents

1: **THE MODERN DIGITAL DESIGN FLOW** ................................................................. 1

   1.1 **HISTORY OF HARDWARE DESCRIPTION LANGUAGES** ................................. 1
   1.2 **HDL ABSTRACTION** .................................................................................. 4
   1.3 **THE MODERN DIGITAL DESIGN FLOW** ....................................................... 8

2: **VERILOG CONSTRUCTS** .................................................................................. 13

   2.1 **DATA TYPES** ............................................................................................ 13
      2.1.1 **Value Set** ......................................................................................... 14
      2.1.2 **Net Data Types** ................................................................................ 14
      2.1.3 **Variable Data Types** ........................................................................ 15
      2.1.4 **Vectors** ............................................................................................. 15
      2.1.5 **Arrays** ............................................................................................... 16
      2.1.6 **Expressing Numbers Using Different Bases** ...................................... 16
      2.1.7 **Assigning Between Different Types** .................................................. 17
   2.2 **VERILOG MODULE CONSTRUCTION** ....................................................... 17
      2.2.1 **The Module** ....................................................................................... 18
      2.2.2 **Port Definitions** ................................................................................ 18
      2.2.3 **Signal Declarations** .......................................................................... 19
      2.2.4 **Parameter Declarations** ..................................................................... 20
      2.2.5 **Compiler Directives** .......................................................................... 20

3: **MODELING CONCURRENT FUNCTIONALITY IN VERILOG** ......................... 23

   3.1 **VERILOG OPERATORS** .............................................................................. 23
      3.1.1 **Assignment Operator** ........................................................................ 23
      3.1.2 **Continuous Assignment** ................................................................... 23
      3.1.3 **Bitwise Logical Operators** ................................................................ 24
      3.1.4 **Reduction Logic Operators** ............................................................... 25
      3.1.5 **Boolean Logic Operators** .................................................................. 25
      3.1.6 **Relational Operators** .......................................................................... 25
      3.1.7 **Conditional Operators** ..................................................................... 26
      3.1.8 **Concatenation Operator** ..................................................................... 26
      3.1.9 **Replication Operator** ......................................................................... 27
      3.1.10 **Numerical Operators** ....................................................................... 27
      3.1.11 **Operator Precedence** ...................................................................... 28
   3.2 **CONTINUOUS ASSIGNMENT WITH LOGICAL OPERATORS** .................... 29
      3.2.1 **Logical Operator Example: SOP Circuit** ........................................... 29
      3.2.2 **Logical Operator Example: One-Hot Decoder** .................................... 30
      3.2.3 **Logical Operator Example: 7-Segment Display Decoder** ................. 31
      3.2.4 **Logical Operator Example: One-Hot Encoder** .................................... 34
      3.2.5 **Logical Operator Example: Multiplexer** ............................................ 36
      3.2.6 **Logical Operator Example: Demultiplexer** ....................................... 36