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Broadband Impedance Matching for Inductive Interconnect in VLSI Packages

Authors: Brock J. LaMeres, University of Colorado
         Sunil P. Khatri
         Texas A&M University

Presenter: Nikhil Jayakumar
           Texas A&M University
Problem Statement

• Reflections from interconnect will limit VLSI system performance

• This is caused by:

  1) Inductive Package Interconnect
  2) Faster Risetimes in Off-chip Driver Circuitry
Agenda

1) Inductive Package Interconnect

2) Proposed Solution

3) Experimental Results
Why is packaging limiting performance?

Transistor Technology is Outpacing Package Technology
Why is packaging limiting performance?

- **Package Interconnect Looks Inductive**
  - Long interconnect paths
  - Large return loops

\[ L = \frac{\Phi}{I} \]
Why is packaging limiting performance?

- **Inductive Interconnect Leads to Reflections**
  - Interconnect is not matched to system
  - Reflections occur due to interconnect

\[
\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}
\]

\(Z_L > 50\Omega\)

\(Z_0 = 50\Omega\)
Why is packaging limiting performance?

• **Aggressive Package Design Helps, but is expensive…**
  
  - 95% of VLSI design-starts are wire bonded
  - Goal: Extend the life of wire bonded packages

  \[
  \begin{align*}
  &\text{QFP – Wire Bond : } 4.5\text{nH} \rightarrow \$0.22 / \text{pin} \\
  &\text{BGA – Wire Bond : } 3.7\text{nH} \rightarrow \$0.34 / \text{pin} \\
  &\text{BGA – Flip-Chip : } 1.2\text{nH} \rightarrow \$0.63 / \text{pin}
  \end{align*}
  \]
Why Now?

Cost
- Historically, the transistor delay has dominated performance.
- Inexpensive packaging has met the electrical performance needs.

Faster Risetimes
- As transistors shrink, faster risetimes can be created.
- Everything in the package becomes a transmission line.

Impedance Matching
- The impedance of the package is not matched to the system.
- This leads to reflections from the inductive wire bond in the package.
Current Solution to Reflections

• **Live with the Signal Path Reflections**

1) Run the signals slow enough so that reflections are small

\[ \Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} < 10\% \]

2) Terminate Signals on the Mother board so that reflections are absorbed
Current Solution to Reflections

• Limitations of Approach

1) Run the signals slow enough so that reflections are small
   • Limits System Performance

2) Terminate Signals on the Mother board so that reflections are absorbed
   • This only eliminates primary reflections, the second still exists
Proposed Solutions – Impedance Compensation

• Add Capacitance Near Bond Wire to Reduce Impedance

- Adding additional capacitance lowers the wire bond impedance
- Impedance can be matched to system, reducing reflections

\[ Z_{WireBond} = \sqrt{\frac{L_{WireBond}}{C_{WireBond}}} \]

Add Capacitance to lower Z
Proposed Solutions – Impedance Compensation

- If the capacitance is close to the wire bond, it will alter its impedance.
- Electrical lengths less than 20% of risetime are treated as lumped elements.
- For modern dielectrics, anything within 0.15” of wire bond is lumped.

![Graph showing impedance matching](image)
Proposed Solutions – Impedance Compensation

• Capacitance on the IC or Package is close enough to alter impedance

\[
Z_{WireBond} = \sqrt{\frac{L_{WB}}{C_{WB} + C_{pkg} + C_{MIM}}} = 50\Omega'
\]
Static Compensator

- Capacitor values chosen prior to fabrication

- Equal amounts of capacitance are used on-chip and on-package

\[ Z_{\text{WireBond}} = \sqrt{\frac{L_{\text{WB}}}{C_{\text{WB}} + C_{\text{pkg}} + C_{\text{MIM}}}} = 50\,\Omega' \]
Static Compensator

- **On-Package Capacitors**
  - Embedded capacitor construction is used
  - No components are needed, reducing package cost
  - Capacitance values needed can be implemented using this construction

  - Modern Packages can achieve plane-to-plane separations of \( t=0.002'' \)
  - This translates to 0.64\( pF/mm^2 \)
Static Compensator

• On-Chip Capacitors

- Device and MIM capacitors are evaluated
- Targeting area beneath wire bond pad, which is typically unused

0.1um BPTM Process

• Device-Based Capacitor : 13 fF/um²
• MIM-Based Capacitor : 1.1 fF/um²
Static Compensator

- **Inductor Modeling**

  - Typical VLSI wire bond lengths range from 1mm to 5mm
  - Electrical parameter extraction is used to find L and C or wire bond

<table>
<thead>
<tr>
<th>Length</th>
<th>L</th>
<th>C</th>
<th>Z₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>1mm</td>
<td>0.569nH</td>
<td>26fF</td>
<td>148Ω</td>
</tr>
<tr>
<td>2mm</td>
<td>1.138nH</td>
<td>52fF</td>
<td>148Ω</td>
</tr>
<tr>
<td>3mm</td>
<td>1.707nH</td>
<td>78fF</td>
<td>148Ω</td>
</tr>
<tr>
<td>4mm</td>
<td>2.276nH</td>
<td>104fF</td>
<td>148Ω</td>
</tr>
<tr>
<td>5mm</td>
<td>2.845nH</td>
<td>130fF</td>
<td>148Ω</td>
</tr>
</tbody>
</table>
Static Compensator

• On-Package Capacitor Sizing

- Capacitor values are found to match wire bond to \(50\Omega\)
- Area is evaluated for feasibility

<table>
<thead>
<tr>
<th>Length</th>
<th>(C_{\text{comp}1})</th>
<th>(C_{\text{comp}2})</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(C)</td>
<td>(A_{\text{Area}})</td>
</tr>
<tr>
<td>1mm</td>
<td>102 fF</td>
<td>388 um(^2)</td>
</tr>
<tr>
<td>2mm</td>
<td>208 fF</td>
<td>554 um(^2)</td>
</tr>
<tr>
<td>3mm</td>
<td>325 fF</td>
<td>692 um(^2)</td>
</tr>
<tr>
<td>4mm</td>
<td>450 fF</td>
<td>815 um(^2)</td>
</tr>
<tr>
<td>5mm</td>
<td>575 fF</td>
<td>921 um(^2)</td>
</tr>
</tbody>
</table>
Experimental Results: Static Compensator

- **Time Domain Analysis (TDR)**

<table>
<thead>
<tr>
<th>Length(_{\text{wb}})</th>
<th>(\Gamma_{\text{No-Comp}})</th>
<th>(\Gamma_{\text{MIM-Comp}})</th>
<th>(\Gamma_{\text{Device-Comp}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 mm</td>
<td>4.5%</td>
<td>0.05%</td>
<td>0.5%</td>
</tr>
<tr>
<td>2 mm</td>
<td>8.7%</td>
<td>0.4%</td>
<td>1.2%</td>
</tr>
<tr>
<td>3 mm</td>
<td>12.7%</td>
<td>1.3%</td>
<td>2.4%</td>
</tr>
<tr>
<td>4 mm</td>
<td>16.4%</td>
<td>2.7%</td>
<td>4.1%</td>
</tr>
<tr>
<td>5 mm</td>
<td>19.8%</td>
<td>4.8%</td>
<td>6.0%</td>
</tr>
</tbody>
</table>

Worst Case: 5mm

No Static Capacitance = **19.8%**

w/ Static Capacitance = **4.8%**
Experimental Results: Static Compensator

- Frequency Domain Analysis ($Z_{in}$)

Worst Case: 5mm

- $f_{+/-10\%}$ No Static Capacitance = 1.9 GHz
- $f_{+/-10\%}$ w/ Static Capacitance = 3.0 GHz

<table>
<thead>
<tr>
<th>Length $w_b$</th>
<th>$f_{\text{No-Comp}}$</th>
<th>$f_{\text{MIM-Comp}}$</th>
<th>$f_{\text{Device-Comp}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 mm</td>
<td>9.3 GHz</td>
<td>14 GHz</td>
<td>12 GHz</td>
</tr>
<tr>
<td>2 mm</td>
<td>4.7 GHz</td>
<td>7.1 GHz</td>
<td>5.7 GHz</td>
</tr>
<tr>
<td>3 mm</td>
<td>3.1 GHz</td>
<td>4.8 GHz</td>
<td>3.8 GHz</td>
</tr>
<tr>
<td>4 mm</td>
<td>2.4 GHz</td>
<td>3.7 GHz</td>
<td>2.9 GHz</td>
</tr>
<tr>
<td>5 mm</td>
<td>1.9 GHz</td>
<td>3.0 GHz</td>
<td>2.5 GHz</td>
</tr>
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Static Compensator

• Limitations of Approach

- Process/Design variation in wire bonds and capacitors lead to error
- Each wire bond must be evaluated for compensation requirements

• Possible Enhancement

- Altering compensation capacitance after fabrication
- i.e., Dynamic Compensator
Dynamic Compensator

- Programmable capacitance is placed on-chip
  - On-chip capacitance is close enough to alter wire bond impedance
  - Active circuitry on-chip can switch in different amounts of capacitance

\[ Z_{WireBond} = \sqrt{\frac{L_{WB}}{C_{WB} + C_{Comp}}} = 50\Omega 's \]
Dynamic Compensator

• **Pass Gates are used to switch in on-chip capacitors**

- Pass gates connect on-chip capacitance to the wire bond inductance
- Pass gates have control signals which can be programmed after fabrication
Dynamic Compensator

• **On-Chip circuitry is independent of package**

- Compensation works across multiple package technologies
- This decouples IC and Package design

Only IC technology is used for compensation
Dynamic Compensator

- On-Chip capacitor sizing

- The on-chip capacitance performs the compensation to 50Ω
- The circuit must cover the entire range of wire bond inductances
- The diffusion capacitance of the pass gates must be included in the analysis

<table>
<thead>
<tr>
<th>Length</th>
<th>$C_{comp}$</th>
</tr>
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<tbody>
<tr>
<td>1mm</td>
<td>202 fF</td>
</tr>
<tr>
<td>2mm</td>
<td>403 fF</td>
</tr>
<tr>
<td>3mm</td>
<td>605 fF</td>
</tr>
<tr>
<td>4mm</td>
<td>806 fF</td>
</tr>
<tr>
<td>5mm</td>
<td>1008 fF</td>
</tr>
</tbody>
</table>

$200 \text{ fF} \leq C_{comp} \leq 1010 \text{ fF}$
### Dynamic Compensator

- **Compensator Design**

- The on-chip capacitance performs the compensation to **50Ω**
- The diffusion capacitance of the pass gates must be included in the analysis

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</tbody>
</table>

\[
C_{bank} = \frac{1}{3}(C_{bank}) + \frac{2}{3}(C_{bank})
\]
Dynamic Compensator

• Capacitance Design

- Pass Gates are sized to drive the on-chip capacitance
- Each bank of capacitance includes the pass gates

\[ C_{\text{bank1}} = C_{pg1} + C_{\text{int1}} \]

\[ C_{\text{bank2}} = C_{pg2} + C_{\text{int2}} \]

\[ C_{\text{bank3}} = C_{pg3} + C_{\text{int3}} \]

\[ C_{\text{Off}} = \text{Range Offset} \]
Dynamic Compensator

- Capacitance Design

- Again, both MIM and Device-based capacitors are evaluated for area

<table>
<thead>
<tr>
<th>Component</th>
<th>MIM-Based Area (W × L)</th>
<th>Device-Based Area (W × L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pass Gate #1</td>
<td>32.4μm x 0.1μm</td>
<td>32.4μm x 0.1μm</td>
</tr>
<tr>
<td>Pass Gate #2</td>
<td>62.5μm x 0.1μm</td>
<td>62.5μm x 0.1μm</td>
</tr>
<tr>
<td>Pass Gate #3</td>
<td>129.6μm x 0.1μm</td>
<td>129.6μm x 0.1μm</td>
</tr>
<tr>
<td>$C'_{off}$</td>
<td>8.5μm x 8.5μm</td>
<td>2.5μm x 2.5μm</td>
</tr>
<tr>
<td>$C_1$</td>
<td>11μm x 11μm</td>
<td>3.3μm x 3.3μm</td>
</tr>
<tr>
<td>$C_2$</td>
<td>15.5μm x 15.5μm</td>
<td>4.6μm x 4.6μm</td>
</tr>
<tr>
<td>$C_3$</td>
<td>22μm x 22μm</td>
<td>6.6μm x 6.6μm</td>
</tr>
<tr>
<td>Total</td>
<td>65μm x 65μm</td>
<td>25μm x 25μm</td>
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Experimental Results: Dynamic Compensator

• Time Domain Analysis (TDR)

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<td>4.5%</td>
<td>1.0%</td>
<td>1.0%</td>
<td>001</td>
</tr>
<tr>
<td>2 mm</td>
<td>8.7%</td>
<td>1.8%</td>
<td>1.3%</td>
<td>011</td>
</tr>
<tr>
<td>3 mm</td>
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<td>3.6%</td>
<td>3.0%</td>
<td>100</td>
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Experimental Results: Dynamic Compensator

• Frequency Domain Analysis ($Z_{in}$)

Worst Case: 5mm

$f_{+/-10\%}$ No Dynamic Capacitance = 1.9 GHz

$f_{+/-10\%}$ w/ Dynamic Capacitance = 4.1 GHz

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3mm
Summary

• Inductive Package Interconnect causes reflections which limits system performance

• The move toward Advanced Packaging is Resisted due to Cost

• Adding On-Chip & On-Package capacitors does not add cost

• A Static and Dynamic Compensation Approach can match the package interconnect impedance to the system
Questions?