Electrical Characterization of a Novel Coaxial Die-to-Die Interconnect

Chris McIntosh
406-994-7548
cmmcintosh@gmail.com

Sam Harkness
406-994-7548
samuel.harkness@gmail.com

Brock J. LaMeres
406-994-5987
lameres@ece.montana.edu

Electrical & Computer Engineering Department, Montana State University, Bozeman, MT 59717

Abstract—This paper presents the electrical modeling and characterization of a new chip-to-chip interconnect scheme consisting of miniature coaxial cables. A Micro-Electrical-Mechanical System (MEMS) etching process is used to create trenches along the perimeter of a Silicon substrate to form interface features for the miniature coaxial cables. The coaxial cables use this transition trench to make contact to coplanar transmission lines implemented on-chip. This technique yields a fully impedance matched system for use in high speed signal propagation between dies. This approach promises to deliver higher signaling performance over the traditional wire bond or flip-chip bumping techniques by reducing or eliminating sources of electrical noise such as reflections, cross-talk, and simultaneous switching noise. This paper presents the electrical characterization of prototypes which were fabricated using this interconnect system. Adjacently placed dies are measured when using the new coaxial interconnect approach and compared to measurements of the same system when using wire-bonding. Finite Element Analysis is used to de-embed the system response to yield a comparison of the two interconnect structures (coaxial vs. wire bond). [1] [2]

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1. INTRODUCTION

The demand for high performance mobile aerospace computing has driven the development of 3-D packaging techniques such as chip and package stacking [1,2]. Integrating multiple IC technologies into a System-in-Package (SiP) has provided a way to achieve chip/package ratios greater than 200% [3]. The mobile aerospace application requires functionally diverse technology such as CMOS, RF, and passive components to be integrated into the smallest footprint, which is ideal for an SiP approach [4-6]. The most widely used combination of technology in SiP is the integration of a CMOS microprocessor and memory. The interconnection of the individual devices is typically accomplished using wire bonding. A wire bond provides a flexible approach to interconnecting arbitrary pad configurations and has been established as the most commonly used package interconnect over the past decades [7-9].

While a wire bond provides a mechanically attractive solution to SiP interconnect, it has a host of electrical drawbacks [10]. First, the high aspect ratio of the wire bond structure leads to a relatively high inductive property compared to the rest of the system. This becomes an issue as signaling speeds increase and the interconnect begins to behave as a distributed system. When the interconnect behaves as a transmission line, then propagation delay and impedance discontinuities have to be considered. The wire bond tends to have very high characteristic impedance relative to the traditional 50Ω system impedance. This impedance mismatch leads to reflections which may cause inadvertent switching of digital circuits. The second drawback of the wire bond is the unshielded nature of the structure. Electromagnetic (EM) field coupling between wire bonds leads to cross-talk noise on the signal lines. Finally, the inductive property of the wire bond causes Simultaneous Switching Noise (SSN) when the return current from high speed I/O circuitry travels through the interconnect and induces $^{di}/_{dt}$ noise [11]. These noise sources drive the need for a new high speed interconnect structure for SiP [12]. This need is especially present in mobile aerospace applications where diverse systems are being integrated to meet reduced spatial requirements. Applications such as antennas and sensors would especially benefit from a fully shielded and impedance matched SiP interconnect system [16].

We have developed and prototyped a novel interconnect system for SiP that uses miniature, semi-rigid, coaxial cables. Using a coaxial cable instead of a wire bond offers solutions to all of the electrical noise issues mentioned above by providing controlled impedance, a shielded signal

path, and a dedicated low impedance return path. In this paper, we present the electrical characterization of our proposed interconnect system. We used Time Domain Reflectometry (TDR) and Transmission (TDT) to measure the response of our system. An equivalent simulation model was then constructed of the system that matched the measured results. Finite Element Analysis was used to model the response of the on-chip coplanar transmission lines and was incorporated into the system model. From this model, the interconnect portion was de-embedded to provide the electrical performance of just the structures of interest. We performed this process on a system using wire bonds to connect adjacently placed dies and again on the same system using the new coaxial interconnect to compare the electrical performances of both approaches.

2. COAXIAL INTERCONNECT SYSTEM

Our interconnect system is accomplished by using semi-rigid, miniature coaxial cables that interface to on-chip coplanar transmission lines using an etched trench. The center conductor of the coaxial cable is exposed to make contact to the center trace of the coplanar signal trace while the outer shield of the semi-rigid cable makes contact with the two outer traces of the coplanar structure. Figures 1 and 2 show our system used with adjacently placed dies. Figure 3 shows the interface trench on the Silicon substrate with the coaxial cable removed.
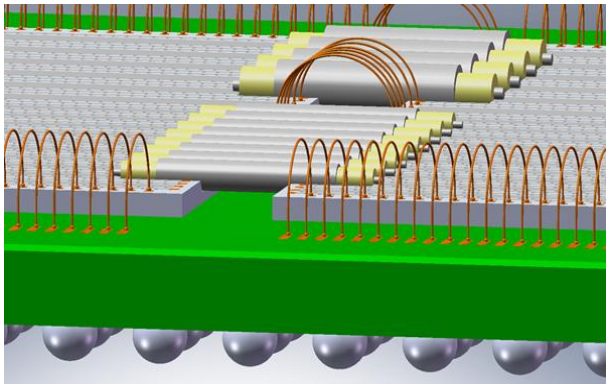

Fig. 1. 3-D Rendering of our interconnect approach used in an SiP application with adjacently placed dies.
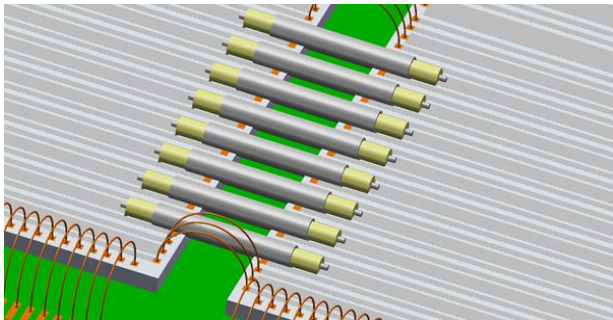

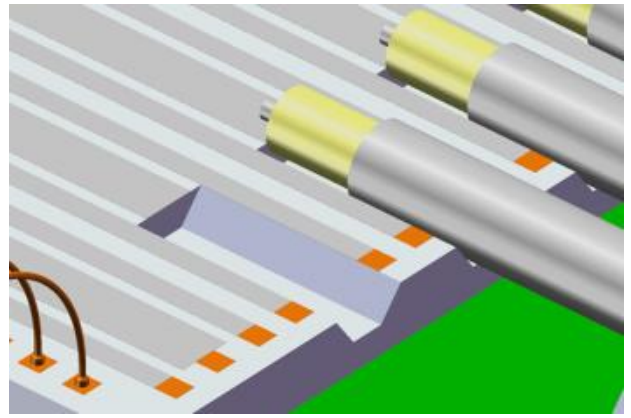Fig. 2. Magnified view of the coaxial interconnect system.

Fig. 3. Magnified view of the etched transition trenches with the coaxial cable removed.

Coaxial Cable Dimensions

The key dimensions that drive the design of the interconnect system are the features of the miniature coaxial cable. In our design, we have evaluated two versions of a miniature, semi-rigid, 50Ω, coaxial cable from *Micro-Coax©* [13]. The coaxial cable consists of a silver-plated, copper clad steel (SPCW) center conductor covered with an insulating layer of Polytetrafluoroethylene (PTFE). The outer conductor is created with a solid tubular layer of copper. The two semi-rigid coaxial cables that were evaluated in this work were the *Micro-Coax©* UT-013 and the *Micro-Coax©* UT-020 with overall diameters of 330μm and 584μm respectively. Figure 4 shows the variable names for the key dimensions of the coaxial cables used in our evaluation.

Coplanar Dimensions

A coplanar transmission line is created using 3 traces of metal residing on the same plane. The inner trace carries the signal wave while the two outer traces carry the ground or return current. The width and thickness of the traces (W_{sig}, W_{gnd}, and T_{sig}), the spacing between the traces (S_{copl}), and the materials of the structure (ε_{r1} and ε_{r2}) dictate the characteristic impedance of the transmission line. Figure 5 shows a cross-section of a coplanar transmission line fabricated on a p-type Silicon substrate. When constructing a coplanar structure on a p-type Silicon structure, a thin layer of Silicon Oxide (SiO_2) is inserted between the semiconductor substrate and the metal to provide a layer of adhesion and additional insulation (T_{ox}). In our system, we used Aluminium to form the 3 traces used in the coplanar transmission line. The impedance of the structure was designed to be 50Ω to match the impedance of the coaxial cable and eliminate reflections due to the off-chip interconnect path.
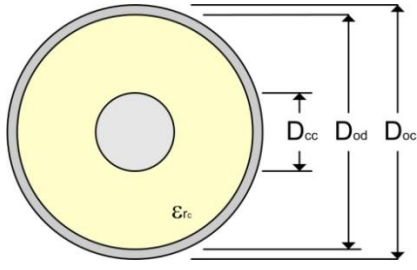
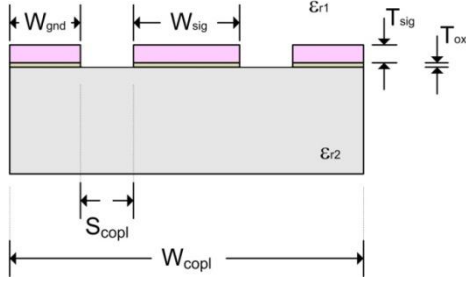Fig. 4. Key dimensions for the coaxial cables.

Fig. 5. Key dimensions for the on-chip coplanar transmission line.

Trench Dimensions

A trench is formed within the coplanar structure such that the coaxial cable can be inserted and make electrical contact between the signal and ground conductors for both the coplanar and coaxial structures. The return path is accomplished by etching the trench within the coplanar structure but without removing any of the metal forming the two outer layer return traces. When the coaxial cable is laid in the trench, its outer shield will be adjacent to the ground lines of the coplanar transmission line.

The signal path is formed by exposing the center conductor of the coaxial cable. When the coaxial cable is inserted into the trench, the center conductor will come to rest on top of the signal trace of the coplanar structure. The size of the coplanar transmission line (W_{sig}, W_{gnd}, and T_{sig}) and the size of the trench (W_{ttop}, W_{tbot}, H_{tsw}, and W_{tsw}) are designed to achieve both a 50Ω impedance and the proper alignment of the coplanar to coaxial transition. Figure 6 shows a cross-section of the trench formed within the coplanar structure annotating the critical dimensions. Figures 7 and 8 show side and top views of the assembled interconnect structure respectively.
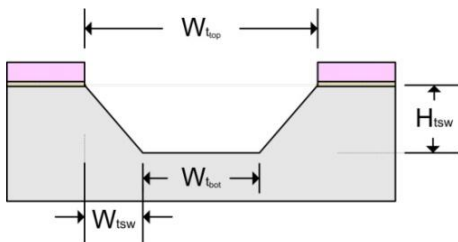

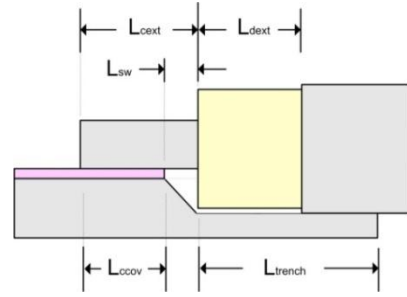Fig. 6. Key dimensions for the etched trench.

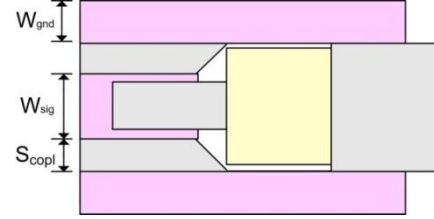Fig. 7. Side view of the assembled interconnect system.

Fig. 8. Top view of the assembled interconnect system.

Cable Spacing

Adjacent coplanar-to-coaxial structures can be placed on a pitch defined by S_{SS} as shown in Figure 9. Table I lists all of the dimensions for our proposed technique for two sizes of miniature, semi-rigid coaxial cable (UT-013 and UT-020).

This table illustrates the incremental area impact of our approach when compared to a typical wire bonded system. In a wire bonded system, a high speed net typically requires 3 bond pads in order to achieve a G-S-G configuration. The perimeter length required for this arrangement consists of the widths of the 3 wire bond pads (W_{pad}) plus the spacing between the pads (S_{pad}). Assuming a 100μm x 100μm bond pad (W_{pad}=100μm) with pad spacing of 100μm (S_{pad}=100μm), the total distance required is [3·Wpad + 2·S_{pad}] = 500μm along the perimeter. In our approach, when using the UT-013 coaxial cable the total distance needed consists of the width of the top of the trench (W_{ttop}=349μm) plus the width of the two ground pads (W_{pad}=100μm). This gives a total perimeter length of [W_{ttop} + 2·W_{pad}] = 549μm per signal. Our approach requires only a 9.8% increase in perimeter to accommodate the coplanar-to-coaxial transition.
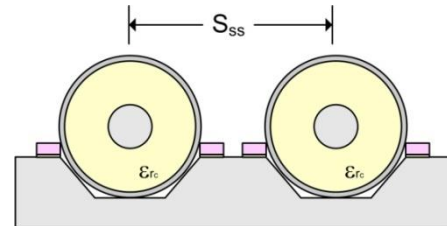

Fig. 9. Side view of two adjacent cables annotating the spacing

Region	Parameter	Units	Coaxial Line	
			UT-013	UT-020
Coaxial (ε_{rc}=2.1)	D_{oc}	µm	330	584
	D_{od}	µm	254	419
	D_{cc}	µm	79	127
Coplanar (ε_{r1}=1) (ε_{r2}=11.7)	T_{sig}	µm	1	1
	T_{ox}	µm	1	1
	W_{sig}	µm	190	400
	W_{gnd}	µm	100	100
	S_{copl}	µm	65	85
	W_{copl}	µm	520	770
	S_{ss}	µm	620	870
Trench	W_{ttop}	µm	320	570
	W_{tbot}	µm	300	530
	W_{tsw}	µm	10	20
	H_{tsw}	µm	123.5	226.5
Transition	L_{trench}	µm	900	900
	L_{dext}	µm	400	400
	L_{sw}	µm	10	20
	L_{cext}	µm	100	100
	L_{ccov}	µm	90	80

3. EXPERIMENTAL SETUP

A test chip was fabricated at the Montana Microfabrication Laboratory (MML) at Montana State University, Bozeman in order to evaluate the feasibility of creating the transition trenches for the coaxial system in Silicon [14]. Figure 10 shows the top view of the prototype die. Figures 10(a) and 10(b) show the coplanar transmission line structures. Figures 10(c) and 10(d) show the etched trenches for the coaxial cables.

(a)   (b)

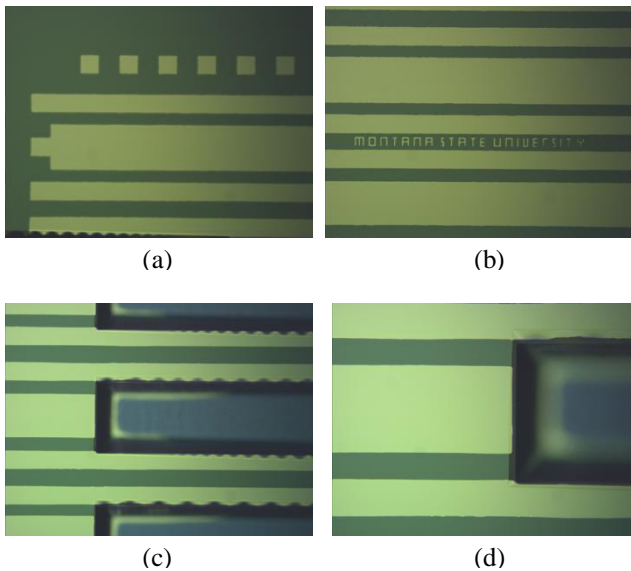(c)   (d)

Fig. 10. Top view of our prototype die showing the coplanar transmission lines (a & b) and the etched trenches (c & d).

A test fixture was created in order to evaluate the electrical performance of the new interconnect schemes. The test fixture is shown in Fig 11 and is loaded with 9 of the prototype dies. This fixture allows the evaluation of adjacently placed die configurations using either a wire bonded or coaxial interconnect approach.
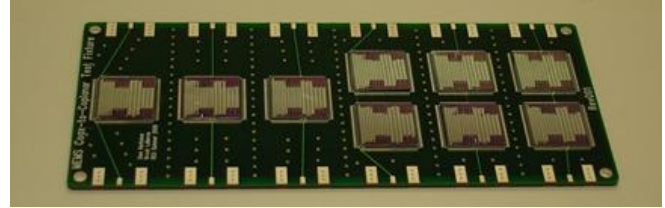

Fig. 11. Test fixture for assembly development and electrical evaluation.

Fig 12 shows a prototype assembly with the miniature coaxial cables attached to adjacently placed dies.
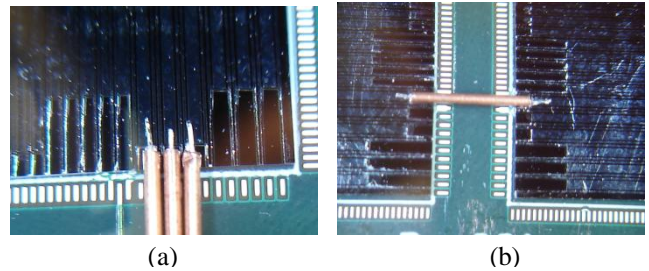

(a)   (b)

Fig. 12. Prototype assembly of adjacently placed dies using miniature coaxial cables (UT-020)

The test fixture was tested using Time Domain Reflectometry (TDR) and Time Domain Transmission (TDT). A Tektronix DSA8200 sampling oscilloscope with an 80E04 TDR module was used for the measurement. This setup is capable of stimulating the system with a 35ps voltage step and acquiring a signal with 20GHz of bandwidth. Figure 13 shows the test setup for the electrical characterization.
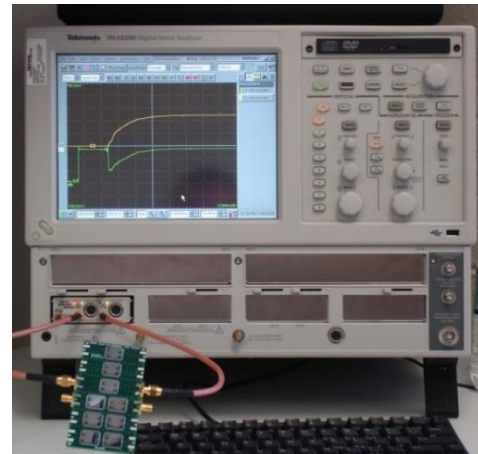

Fig. 13. TDR/TDT test system setup.

4. ASSEMBLY

The assembly for our prototype system was accomplished using a conductive epoxy. The semi rigid coaxial cable was manually stripped to expose its center conductor and inner dielectric. The coaxial cable was laid into the etched trench on the Silicon such that the cable center conductor rests on top of the coplanar center trace. A small amount of conductive epoxy was manually applied to form the bond between the conductors. When the cable is laid into the trench, its outer shield is positioned between the two outer traces of the trench. A small amount of conductive epoxy was brushed across the conductors to form the return path.
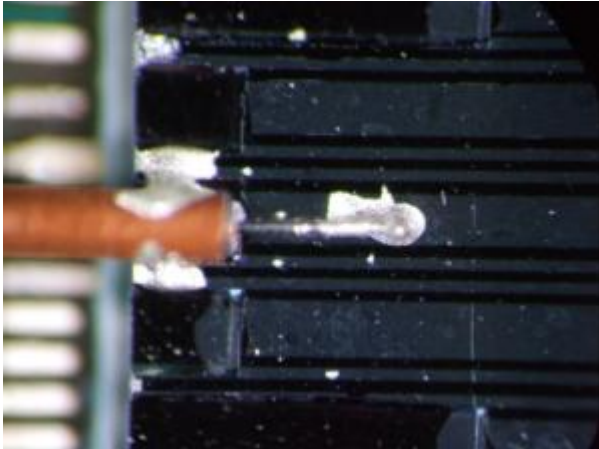

Fig. 14. Top view of prototype coaxial assembly.

The adhesive used for this prototype was an *EPO-TEK*® *H2OE* [15] which is a two component, silver based epoxy designed for microelectric applications. The volume resistivity of *EPO-TEK* is less than 0.4 *m* Ohm-cm at 23°C. The epoxy has a cure time of 15 minutes at 120°C or 5 minutes at 150°C. Figure 15 shows a side profile of the full coaxial system that was assembled using *EPO-TEK*®.
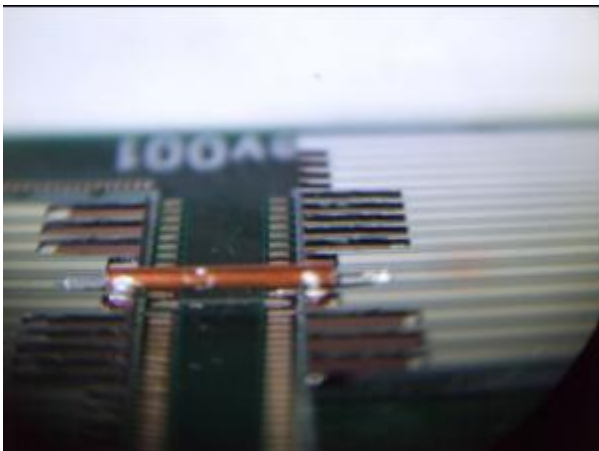

Fig. 15. Side view of prototype coaxial assembly.

5. MEASUREMENT & MODELING

Measurements

TDR/TDT measurements were taken on both the wire bonded system and the system using the miniature coaxial cables. Screenshots of both measurements are shown in figures 16 and 17.
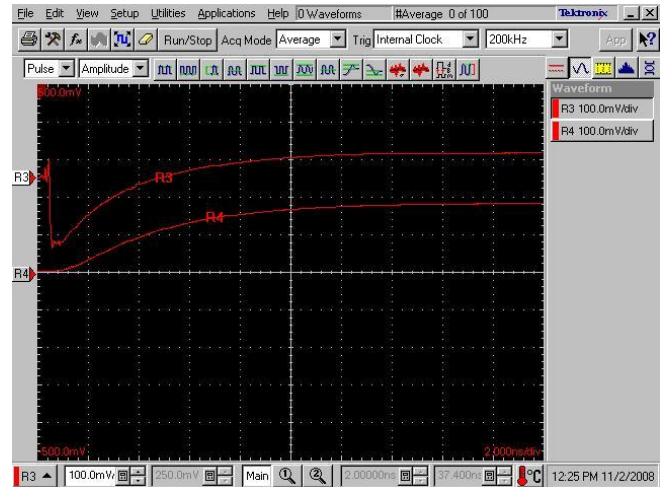

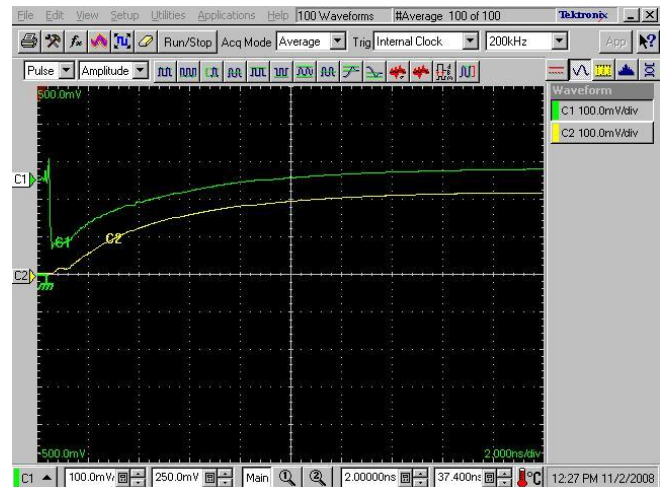Fig. 16. Screenshot of TDR/TDT measurements of the wire bonded system.

Fig. 17. Screenshot of TDR/TDT measurements of the coaxial interconnect system.

Modeling

An equivalent SPICE circuit model was constructed that matched the electrical response of the measurement data. Simple RLC and T-line elements were used to model the behavior of the test fixture cables, PCB traces, connectors, and wire bonds. The complex response of the Silicon coplanar traces required the use of Finite Element Analysis (FEA). The *Electromagnetic Design System* from *Agilent Technologies, Inc.* was used to predict the performance of the signal propagation on the semiconductor substrate of the

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p-type Silicon. An FEA model was used to produce S-parameters that were then incorporated in the system circuit model. Figure 18(a-d) shows the responses of the equivalent circuit model overlaid on top of the measurement data.
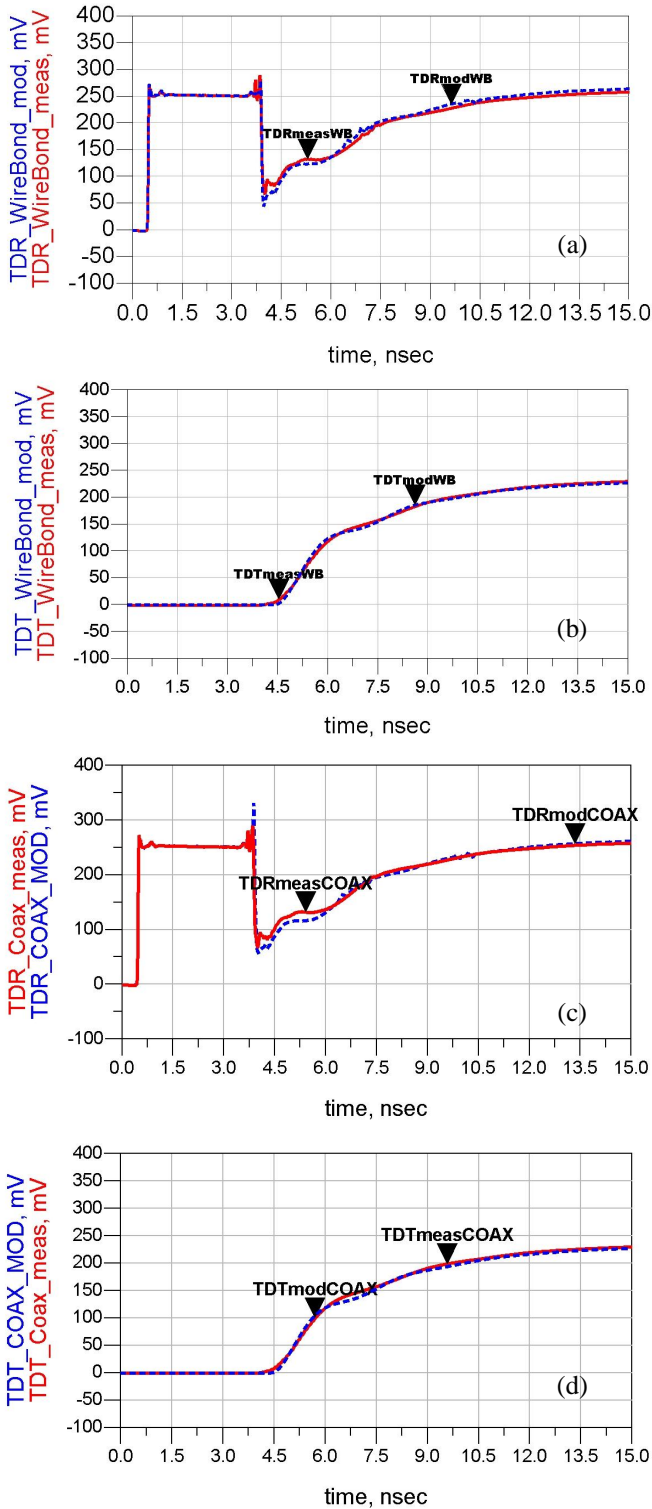

(a)

(b)

(c)

(d)

Fig. 18. Correlation of measurement and model responses: (a) TDR of wire bond; (b) TDT of wire bond; (c) TDR of coaxial cable; and (d) TDT of coaxial cable.

6. ELECTRICAL RESULTS

Once the equivalent models were correlated to the measurement data, they were then modified to extract only the interconnect portions of the circuit. This allowed a true comparison of the electrical performance of the two die-to-die interconnect schemes. These models where then stimulated with an ideal Gaussian step voltage with a risetime of 35ps.

Figure 19 shows a TDR simulation which compares the responses of the wire bond system to that of the system which uses the coaxial interconnect. The wire bond system resulted in reflections of 33% when stimulated with a 35ps voltage step. The coaxial system resulted in reflections of 8%, an improvement of 76%. The reduction in reflected noise in the coaxial interconnect is due to the elimination of impedance discontinuities caused by the inductive wire bonds.
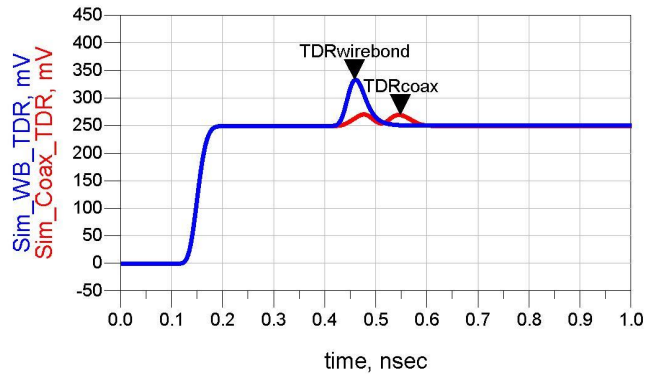

Fig. 19. Simulated TDR comparing the wire bonded system to the coaxial interconnect system.

Figure 20 shows a TDT simulation which compares the responses of the wire bond system to that of the system which uses the coaxial interconnect. The output 10-90 rise time of the coaxial system is modeled at 38ps compared to 49ps for the wire bond, an improvement of 22%. This improvement is due to the reduction of reflections from the inductive wire bond.
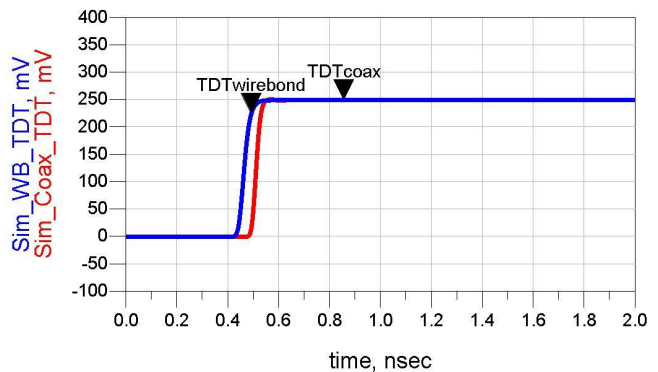

Fig. 20. Simulated TDT comparing the wire bonded system to the coaxial interconnect system.

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7. FUTURE WORK

Now that the electrical feasibility of this packaging approach has been verified, the mechanical reliability must be addressed. The next steps include developing an assembly method that is practical for high volume production. Further, the assembly method needs to be evaluated to determine the vibration tolerance of the coaxial cable under the typical stresses seen in aerospace applications. The increased mass of the coaxial cable relative to a traditional wire bond must be evaluated.

8. CONCLUSION

This paper presented the electrical characterization of a novel die-to-die coaxial interconnect system. The measurement and modeling process were described in addition to the techniques used to de-embed the structures of interest from the measurement data. Simulations were performed on both a wire bond and a coaxial interconnect system to compare the relative electrical performance. It was found that the coaxial interconnect system was able to reduce reflected energy by 76% and improve the transmitted rise time by 22% compared to the wire bond system. The improved electrical performance of the coaxial system makes it ideal for deployment in SiP applications where high speed die-to-die signaling is required.

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BIOGRAPHY

Christopher McIntosh received the B.S. degree in electrical engineering from Montana State University, Bozeman in 2006. He is currently an M.S. candidate in electrical engineering at Montana State University, Bozeman. He works as a Research Assistant at Montana State University where his focus is on the fabrication of novel 3-D package interconnect structures in Silicon. He also works for OnSemi Inc. as an ASIC Designer where he works on high performance mixed signal integrated circuit design.
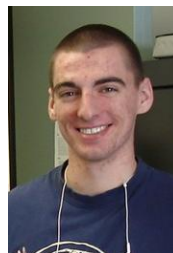
Sam Harkness is currently a B.S. candidate in the electrical engineering department at Montana State University, Bozeman. He works as an Undergraduate Research Assistant in addition to being in the Air Force ROTC. His research focus is on measurement techniques for IC packaging.

Brock J. LaMeres (M'98) received the B.S. degree in electrical engineering from Montana State University, Bozeman in 1998, and the M.S. degree in electrical engineering from the University of Colorado, Colorado Springs in 2001, and the Ph.D. degree in electrical engineering from the University of Colorado, Boulder in 2005. He is currently an Assistant Professor in the Department of Electrical and Computer Engineering at Montana State University (MSU), Bozeman. LaMeres conducts research in the area of radiation tolerant digital systems which is supported by the Montana Space Grant Consortium and NASA. Prior to joining the faculty at MSU in 2006, he worked as a Hardware Design Engineer for Agilent Technologies in Colorado Springs from 1999 to 2006. In this role, he designed acquisition hardware and electronic interconnect systems for digital test and measurement equipment.