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Electrical Characterization of a Novel Coaxial Die-to-Die Interconnect

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Motivation

High Density, High Performance Packaging



- Miniaturization & reliability in aerospace packaging is paramount
- Stacked Die and System-in-Package are emerging
- These systems have significant upside performance potential

Emerging Technologies in Aerospace

- 1) Stacked Die
 - Vertical integration saves footprint impact
- 2) System in Package
 - Multiple components in one package reduces board-level interconnect



Motivation

Drawback of Advanced Packaging

Unshielded interconnect leads to electrical noise:

impedance discontinuities
cross-talk
ground bounce







Our Approach

A New Die-to-Die Coaxial Interconnect System

- Ideal for multiple dies within one package
- Selectively added to high speed nets



Adjacent Dies

Stacked Dies



Our Approach

Electrical Advantages

Shielded Interconnect leads to:

Controlled Impedance
Cross-talk Avoidance
Ground Bounce Reduction







System Design

On and Off Chip Controlled Impedance





On-Chip Coplanar Transmission Lines

Off-Chip Miniature Coaxial Cables



System Design

Etched Trench Allows Interface Between On and Off Chip Interconnect





System Design

Critical Dimensions

Coax Cable Diameter

UT-013 = 330umUT-013 = 584um



Region	Parameter	Units	Coaxial Line	
			UT-013	UT-020
Coaxial	D _{oc}	μm	330	584
(ε _{rc} =2.1)	D_{od}	μm	254	419
	D _{cc}	μm	79	127
Coplanar	T _{sig}	μm	1	1
(ε _{r1} =1)	T _{ox}	μm	1	1
(ε _{r2} =11.7)	W_{sig}	μm	190	400
	W_{gnd}	μm	100	100
	S _{copl}	μm	65	85
	W _{copl}	μm	520	770
	S _{ss}	μm	620	870
Trench	W _{ttop}	μm	320	570
	W _{tbot}	μm	300	530
	W _{tsw}	μm	10	20
	H _{tsw}	μm	123.5	226.5
Transition	L _{trench}	μm	900	900
	L _{dext}	μm	400	400
	L _{sw}	μm	10	20
	L _{cext}	μm	100	100
	L _{ccov}	μm	90	80



Fabrication

- Dies created at the Montana Microfabrication Facility











Fabrication

- A test board was created to test Board-to-Die and Die-to-Die Performance





Fabrication

- Assembly of coaxial system accomplished with conductive silver epoxy





 $(EPO-TEK^{\mathbb{R}} H2OE)$



Test Setup

Time Domain Reflectrometry (TDR) and Transmission (TDT) was used to measure the performance of a wire bonded and coaxial system







Equivalent Modeling

- Equivalent SPICE Models were created to match measured results

Wire bonded System

Coaxial System



Model De-Embedding

- The model of just the interconnect system was de-embedded (deleting the effect of the test setup and long coplanar lines)
- A 35ps step response simulation was performed on the new model to understand the performance of the coaxial system vs. a wire bonded approach



Reflections reduced from <u>33% (wb) to 8% (coax)</u>



Rise time Improved to 38ps (coax) from (48ps)



Data Rate Simulation

An PRBS pattern was used to stimulate the interconnect system to evaluate the data rate.

"Eye Diagrams for the two systems at 5Gb/s (35ps rise times)"





Wire Bond System

Coaxial System



Ongoing Work

- Evaluation of Coplanar Fabrication using Back-End Process
- The height of the coplanar traces above the Semiconductor substrate is the largest source of loss in the on-chip coplanar transmission lines

"Effect of Height Above Si Substrate on Electrical Performance of Coplanar Lines"



• Thicknesses desired (~5um) requires different process rather than thermal oxide growth



Ongoing Work

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Questions







