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Spatial Avoidance of Hardware Faults using FPGA Partial Reconfiguration of Tile-Based Soft Processors

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Reconfigurable Computing Task

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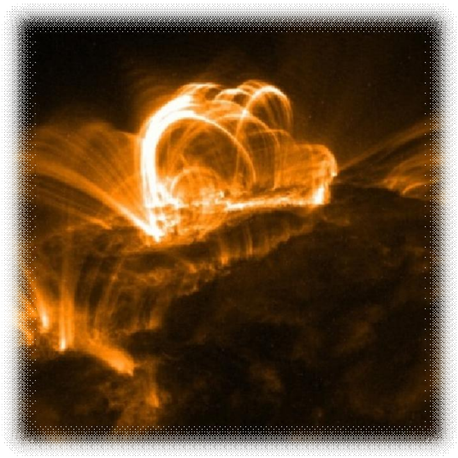
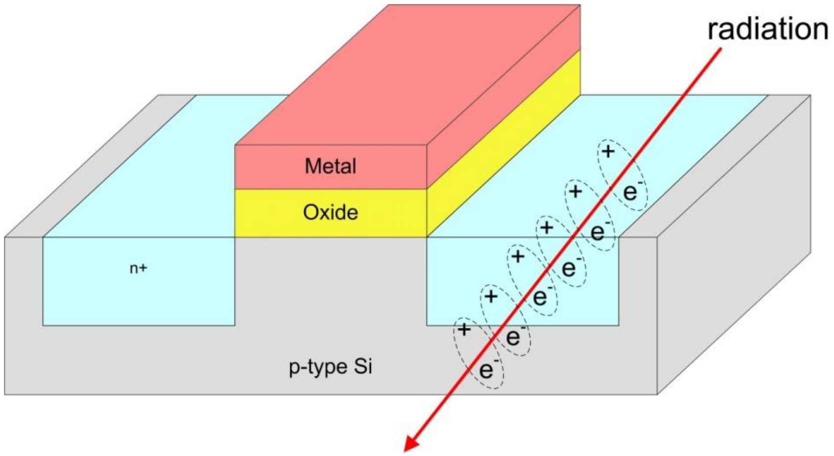
High Performance Processor Task

Motivation

- Radiation has a detrimental effect on electronics in space environments.
- The root cause is from electron/hole pairs creation as the radiation strikes the semiconductor portion of the device and ionizes the material.





Types

- *alpha particles*	(Terrestrial, from packaging/doping)
- *Neutrons*	(Terrestrial, secondary effect from Galactic Cosmic Rays entering atmosphere)
- *Heavy ions*	(Aerospace, direct ionization)
- *Proton*	(Aerospace, secondary effect)

Motivation

- Two types of failures mechanics are induced by radiation

1) Total Ionizing Dose (TID)

  - The cumulative, long term ionizing damage to the device materials
  - Caused by low energy protons & electrons

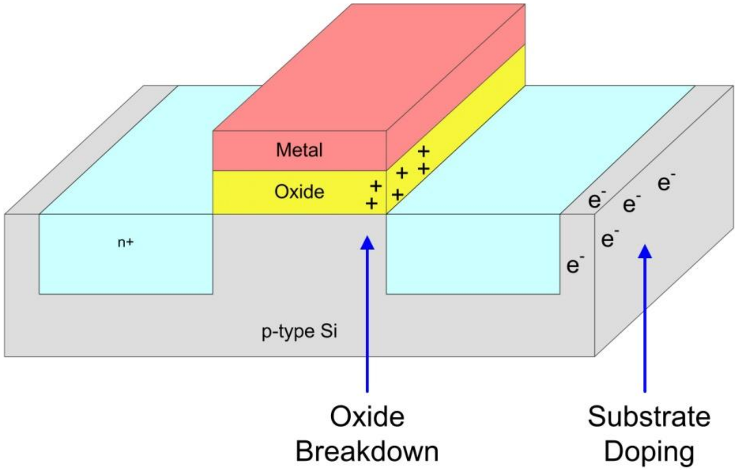
2) Single Event Effects (SEE)

  - Transient spikes caused by Heavy Ions and protons
  - Can be both destructive & non-destructive

Motivation (TID)

1) Total Ionizing Dose (TID)

- As the electron/holes try to recombine, they experience different mobility rates ($\mu_n > \mu_p$)
- Over time, the ionized particles can get trapped in the oxide or substrate of the device prior to recombination
- This can lead to:

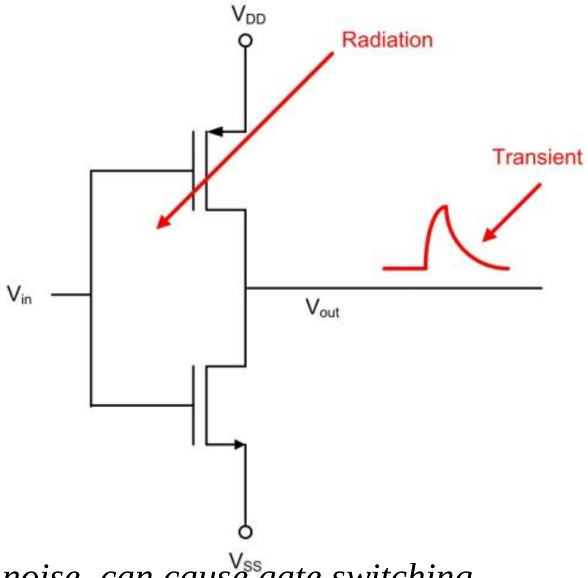


- Threshold Shifting
- Leakage Current
- Timing Skew

Motivation (SEEs)

2) Single Event Effects (SEEs)

- Transient voltage/current induced in devices
- This can lead to both Non-Destructive and Destructive effects



Non-Destructive	**Behavior**
Single Event Transient (SET)	*A transient spike of voltage/current noise, can cause gate switching*
Single Event Upset (SEU)	*A transient captured in a storage device (FF/RAM) as a state change*
Single Event Func. Interrupt (SEFI)	*A fault that cannot be recovered from using a reset.*
Multi-Bit Upsets (MBU)	*Multiple, simultaneous SEUs*

Destructive	**Behavior**
Single Event Latchup(SEL)	*Transient biases the parasitic bipolar SCR in CMOS causing latchup*
Single Event Burnout (SEB)	*Transient causes the device to draw high current which damages part*
Single Event Gate Rupture (SEGR)	*The energy is enough to damage the gate oxide*

Mitigation of TIDs

1) Current Mitigation Techniques (TID)

- Parts can be "hardened" to TID through:
  - layout techniques (sizing of Q_{crit}, enclosed layout)
  - guard rings
  - substrate doping
  - redundant circuitry

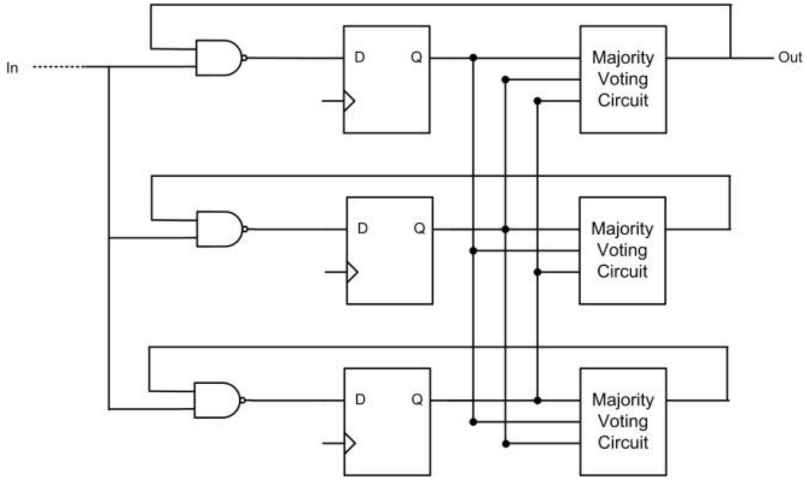
- Parts are specified in terms of:
  - "the amount of energy that can be tolerated by ionizing particles before the part performance is out of spec"
  - units are given in krad (Si), typically 300krad+

- Shielding Does Help
  - low energy protons/electrons can be stopped at the expense of weight

Mitigation of SEEs

2) Current Mitigation Techniques (SEEs)

- Triple Modular Redundancy (TMR)



- Reboot/Recovery Sequences

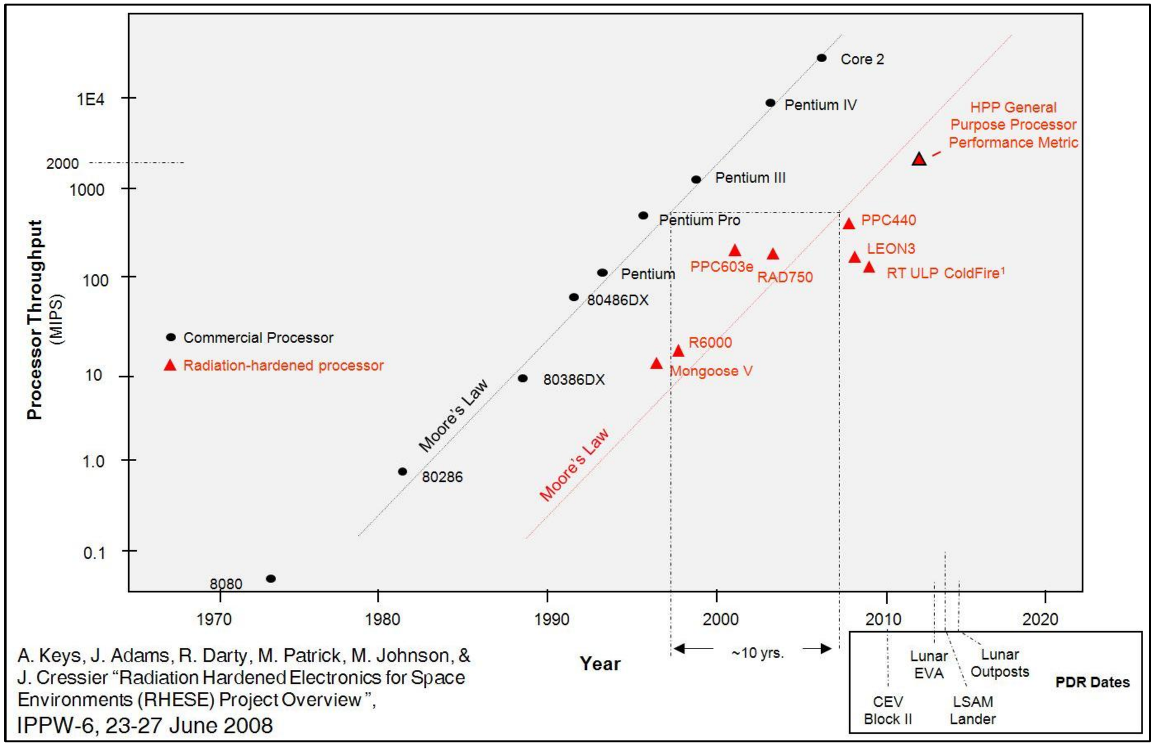
- Shielding <u>Does NOT</u> eliminate all SEEs

  - impractical to shield against high energy particles and Heavy Ions due to necessary mass

Drawback of Mitigation

- **Radiation Hardening = Slower Performance**

- All TID mitigation techniques lead to slower performance



A. Keys, J. Adams, R. Darty, M. Patrick, M. Johnson, & J. Cressier "Radiation Hardened Electronics for Space Environments (RHESE) Project Overview", IPPW-6, 23-27 June 2008

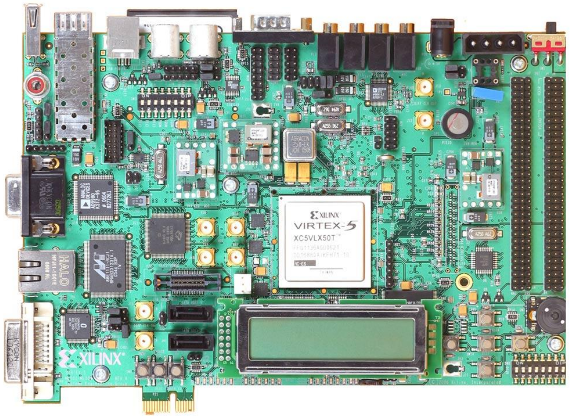
- TID mitigation **DOES NOT** prevent SEEs

FPGAs & Radiation

- **Radiation Mitigation in FPGAs**

  - RAM based FPGAs are traditionally *soft* to radiation

  - Fuse-based FPGAs provide some hardness, but give up the flexibility of real-time programmability



- **Exploiting Reconfiguration**

  - The flexibility of FPGAs enables novel techniques to radiation tolerant computing

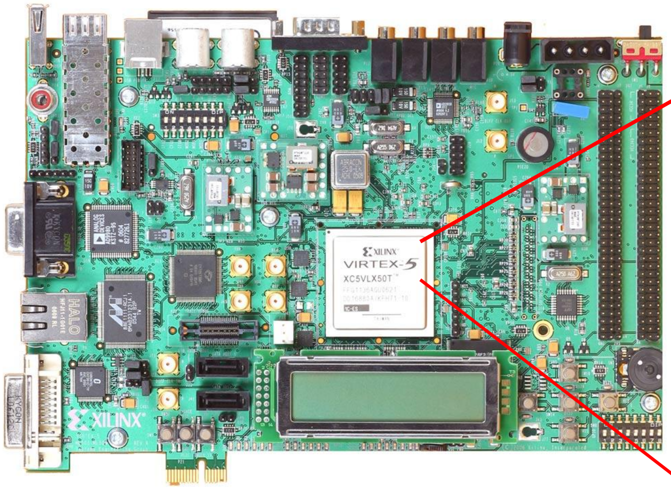
    ex) Dynamic TMR, Spatial Avoidance of TID failures,

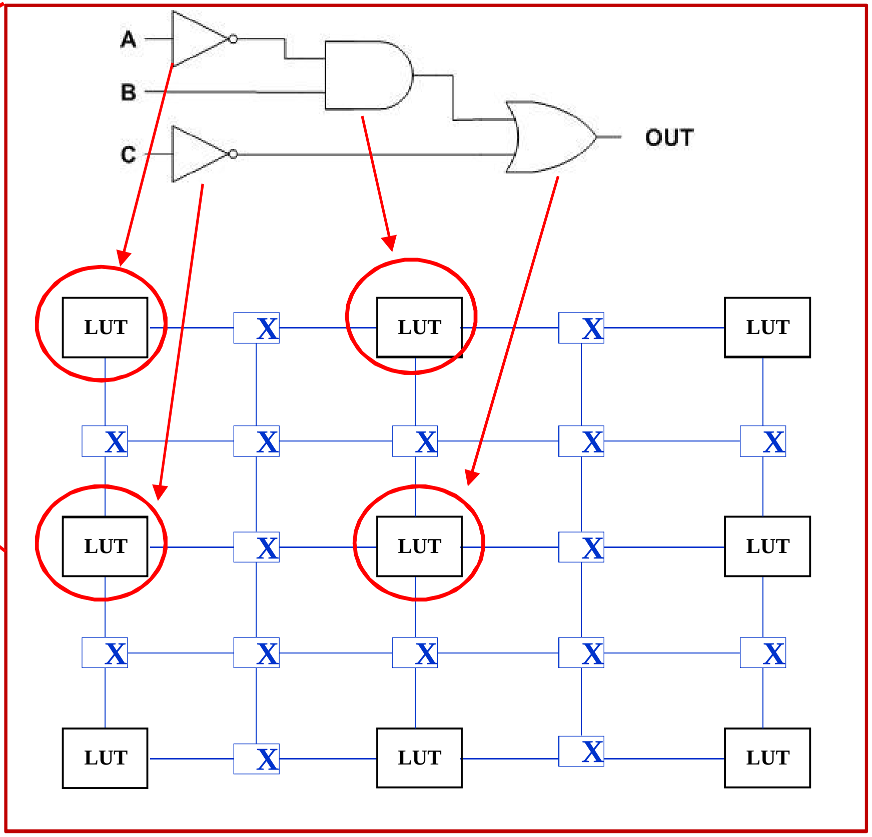
  - The flexibility of FPGAs is attractive to weight constrained Aerospace applications

    ex) Reduction of flight spares, internal spare circuitry

FPGAs as a Solution?

- **Field Programmable Gate Arrays**





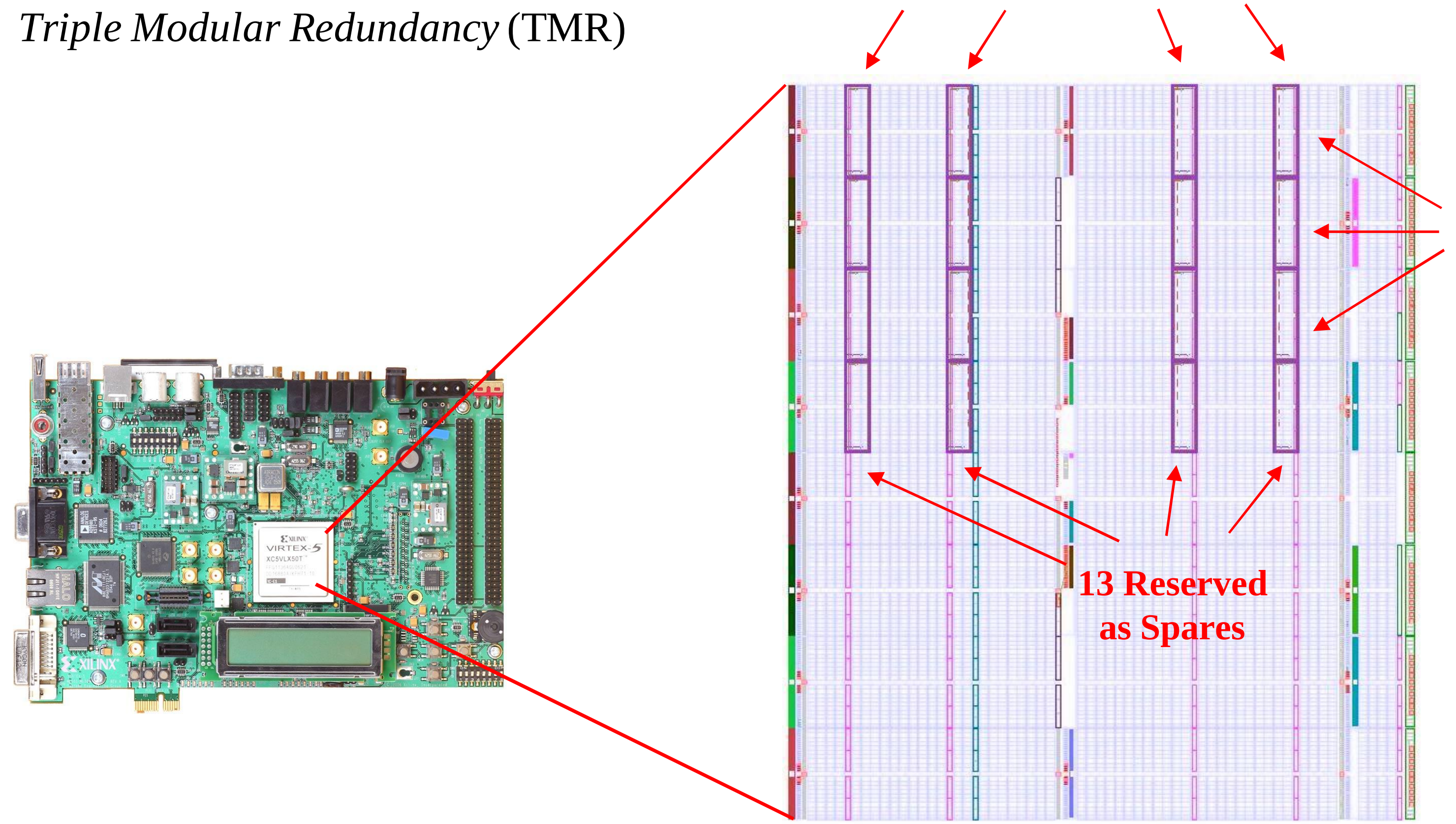
- FPGAs have followed Moore’s Law and now yield comparable processing power to ASICs

Many-Core Architecture

- **Radiation Tolerance Through Architecture**

  - Redundant, Homogenous, Soft Processors

  - At Any Given Time, 3 are configured in *Triple Modular Redundancy* (TMR)



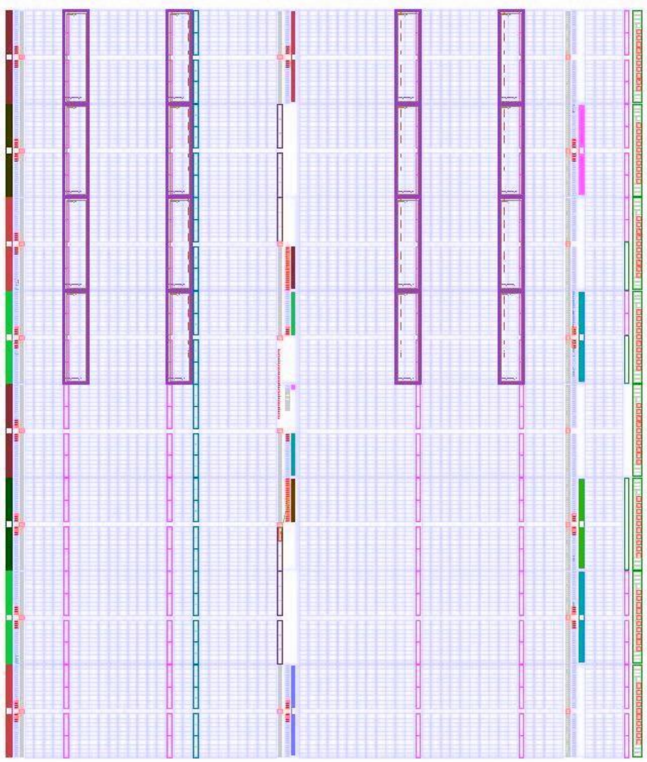
16 picoBlaze Soft Processors

3 Active in TMR

13 Reserved as Spares

Many-Core Architecture

- **Types of Radiation Faults Seen in FPGAs**



1) Soft (SEU, SET)

- *SEUs that can be recovered from using a reset*

2) Medium (SEFI)

- *SEUs in reconfiguration memory, can only be recovered using reconfiguration*

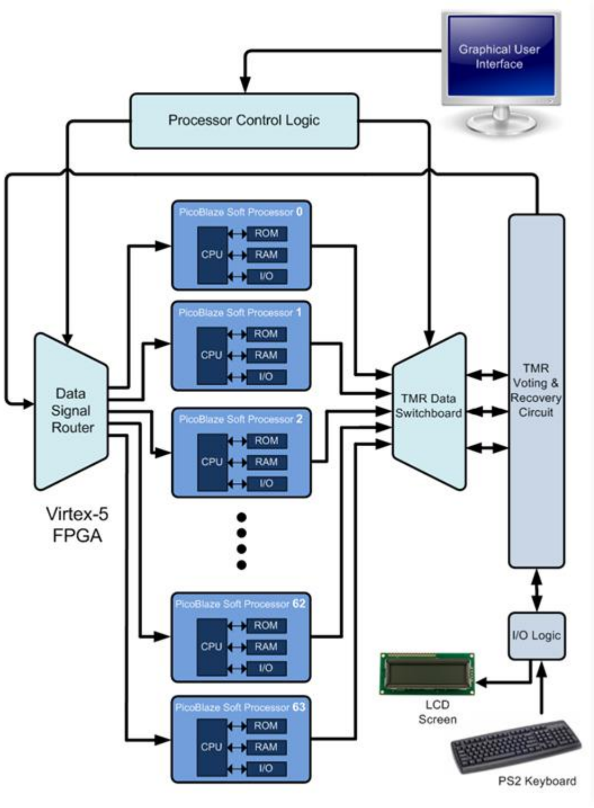
3) Hard (TID / Displacement Damage)

- *Damage to part of the chip due to TID or Displacement Damage*

Many-Core Architecture

- **Fault Recovery Procedures**

Fault Type	**Recovery Action**
Soft Faults	- TMR Voter detects fault - 2 good processors complete current task - Good 2 processors offload variable data - All 3 processors are reset - All 3 processors re-initialized with variable data - All 3 processors resume operation in TMR
Medium Faults	- Same general procedure, *except* Bad processors is **partially reconfigured** to reset configuration RAM
Hard Faults	- A spare processor is brought online to complete TMR - Bad processor is flagged as “DO NOT USE”



Many-Core Architecture

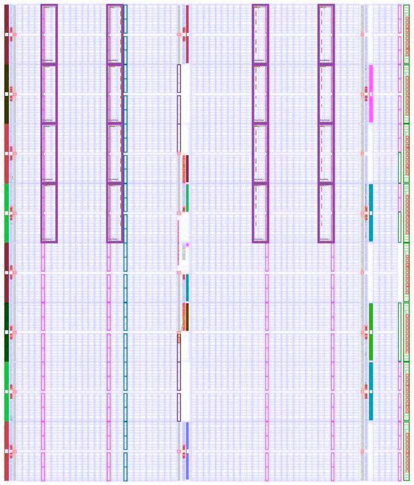
- **Advantages of this Approach**

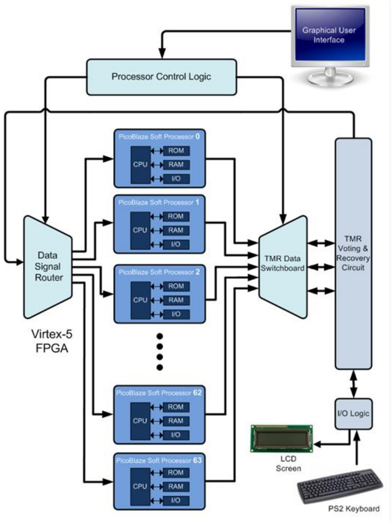
1) SEUs mitigated using traditional TMR

2) Partial Reconfiguration technique increases *hardness* of RAM-based FPGAs

3) Spatial avoidance of damaged regions of FPGA extend system lifetime

4) Logical approach can be applied to RHBD FPGA fabrics (*SIRF*, etc…) for increased radiation immunity



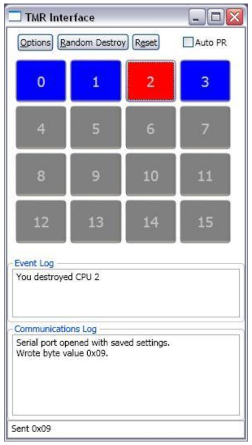


System Prototyping

- **Many-Core Computing Architecture**

  - 16 picoBlaze Processors (3+13) implement on a Virtex-5 LX50
  - The computer system controls basic peripherals
  - A push button is used to mimic soft SEUs
  - A PC GUI is created to inject hard failures
  - HyperTerminal is used to mimic medium severity faults requiring partial reconfiguration
  - Xilinx ChipScope used to monitor processor operation on all 16 processors

PC Gui to induce
Hard Failures

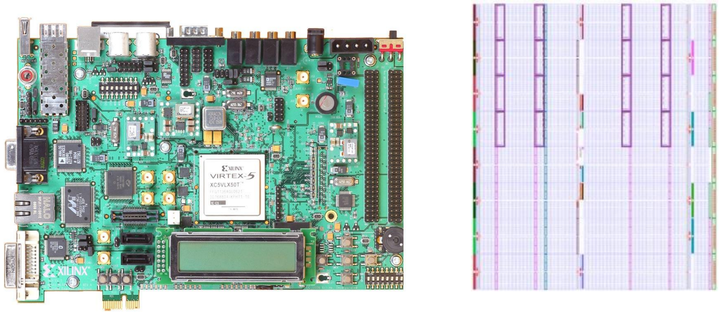


You destroyed CPU 2

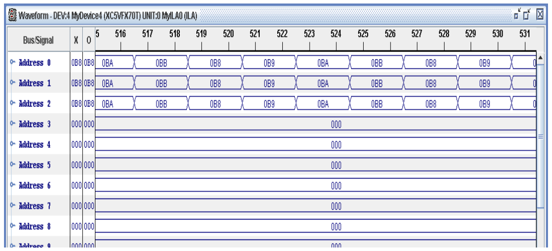
Serial port opened with saved settings.
Wrote byte value 0x09.

Sent 0x09

ML505 V5 Platform w 16 pBlaze uPs



ChipScope Internal Logic Analyzer

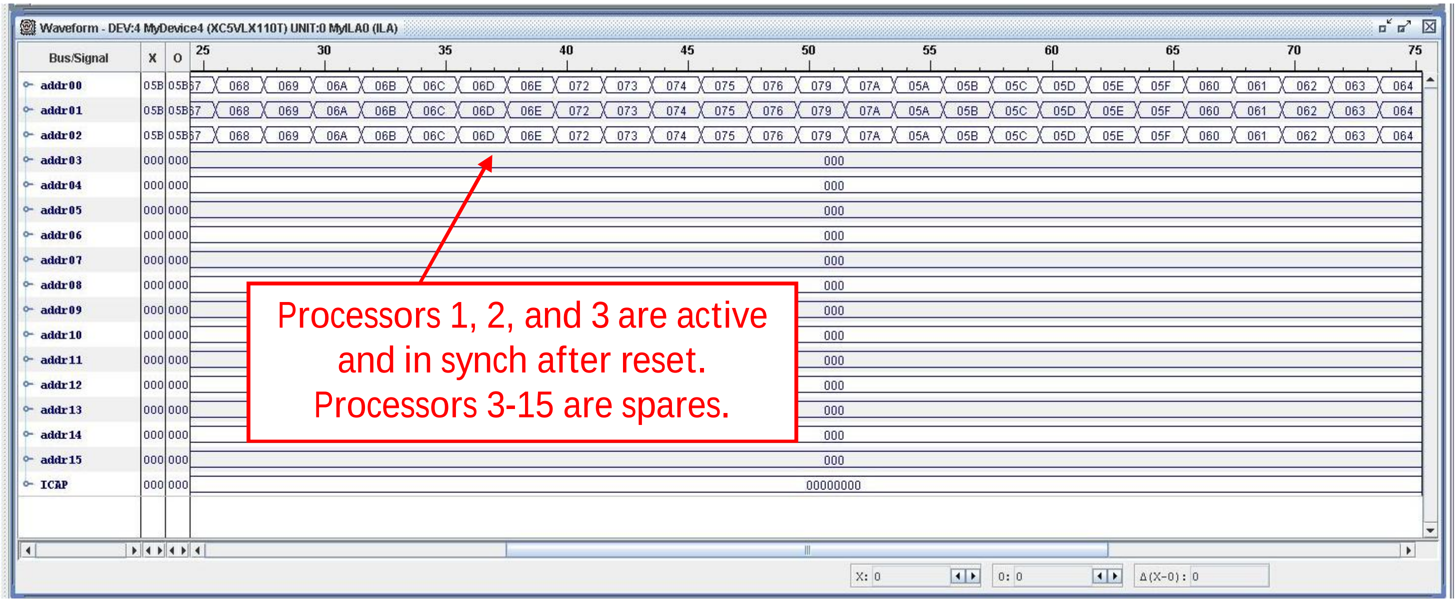


System Demonstration

- **Normal Operation**

  - Processors **0, 1, and 2** are active (blue) and operating in TMR
  - Processors **3-13** provide spare *picoBlaze* processors (gray)

Serial port opened with saved settings.



Bus/Signal	X	O	
addr00	05B	05B	67 068 069 06A 06B 06C 06D 06E 072 073 074 075 076 079 07A 05A 05B 05C 05D 05E 05F 060 061 062 063 064
addr01	05B	05B	67 068 069 06A 06B 06C 06D 06E 072 073 074 075 076 079 07A 05A 05B 05C 05D 05E 05F 060 061 062 063 064
addr02	05B	05B	67 068 069 06A 06B 06C 06D 06E 072 073 074 075 076 079 07A 05A 05B 05C 05D 05E 05F 060 061 062 063 064
addr03	000	000	000
addr04	000	000	000
addr05	000	000	000
addr06	000	000	000
addr07	000	000	000
addr08	000	000	000
addr09	000	000	000
addr10	000	000	000
addr11	000	000	000
addr12	000	000	000
addr13	000	000	000
addr14	000	000	000
addr15	000	000	000
ICAP	000	000	00000000

Processors 1, 2, and 3 are active and in synch after reset. Processors 3-15 are spares.

GUI indicates uP 0, 1, and 2 are active (blue)

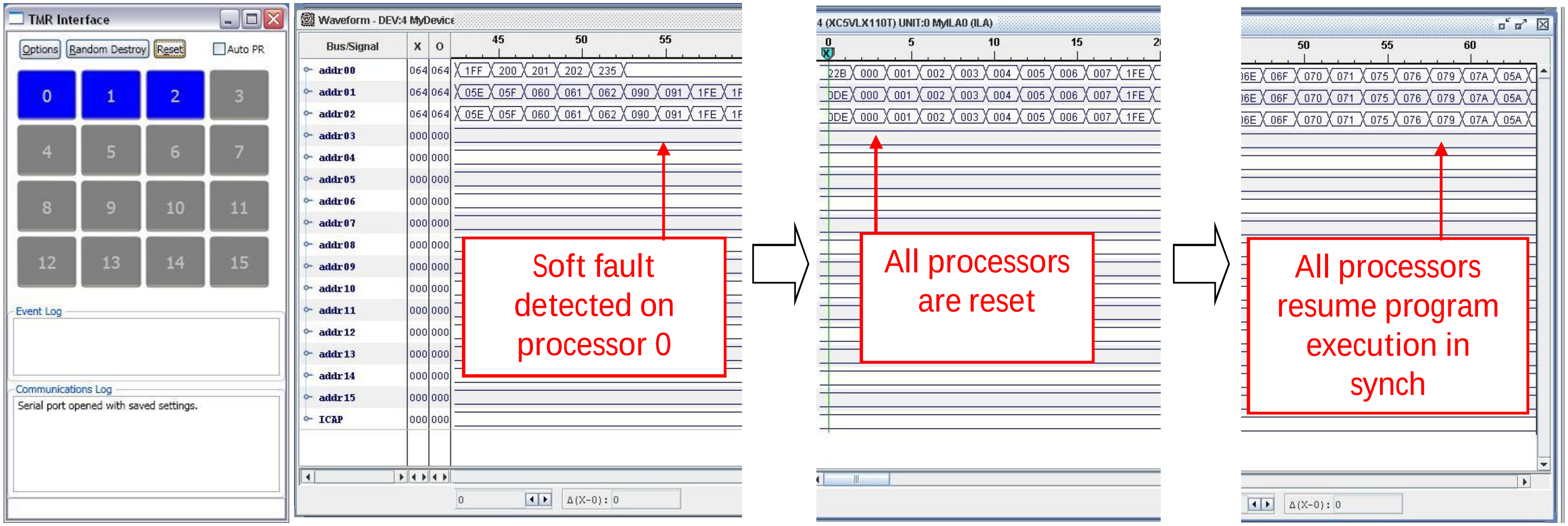
ChipScope shows uP 1,2,3 are running in synch with no faults

(showing address lines between uP and memory for all 16 processors)

System Demonstration

- **Soft Fault Recovery**

  - Processors **0, 1, and 2** are active (blue) operating in TMR
  - Processors **0** undergoes a soft fault and then recovers and resynchronizes



Soft fault detected on processor 0

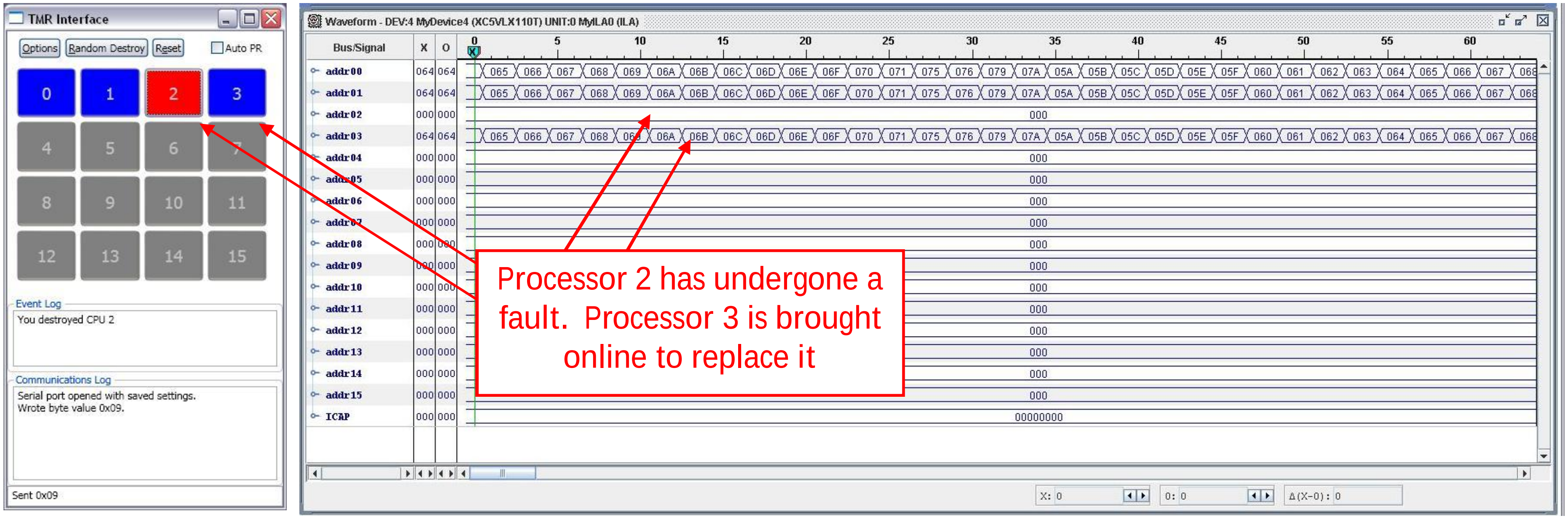
All processors are reset

All processors resume program execution in synch

System Demonstration

- ## Hard Fault Recovery

- Processors **2** undergoes hard fault (induced by GUI, **red**)
- The system shuts down uP #2 and brings on spare processor uP #3 into TMR



```
You destroyed CPU 2
```

```
Serial port opened with saved settings.
Wrote byte value 0x09.
```

```
Sent 0x09
```

Processor 2 has undergone a fault. Processor 3 is brought online to replace it

System Demonstration

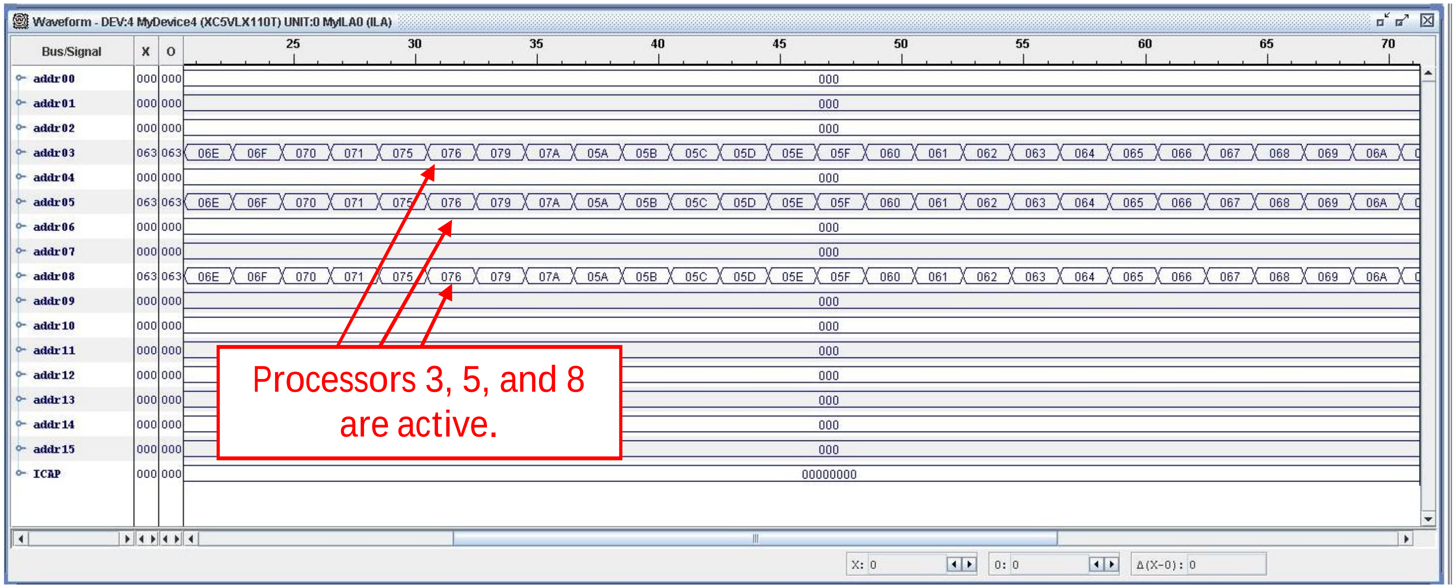
- **Multiple Hard Faults**

  - Multiple hard faults are present
  - uPs 3, 5, and 8 form TMR

```
You destroyed CPU 7
You destroyed CPU 1
Reconfiguring CPU 1
```

```
Wrote byte value 0x06.
    Performing reconfiguration for PicoBlaze 1
        filename = pblaze01.bit
        Bitstream Length = 9278
        Writing Data From SysAce to HWICAP...
        All Words Written to ICAP
```

Sent 0x06



Processors 3, 5, and 8 are active.

Timing/Area Impact

- **Soft Fault Recovery** (reset, reload variable information)

Timing Overhead

- TMR interrupt	2 clocks	
- Reset	2 clocks	
- Read variable data from good processors:	128 clocks	(2 clks/inst, 64 bytes of RAM)
- Write variable data to reset processor:	128 clocks	(2 clks/inst, 64 bytes of RAM)
Total	**260 clocks = 2.6 us**	(100 MHz V5 Clock)

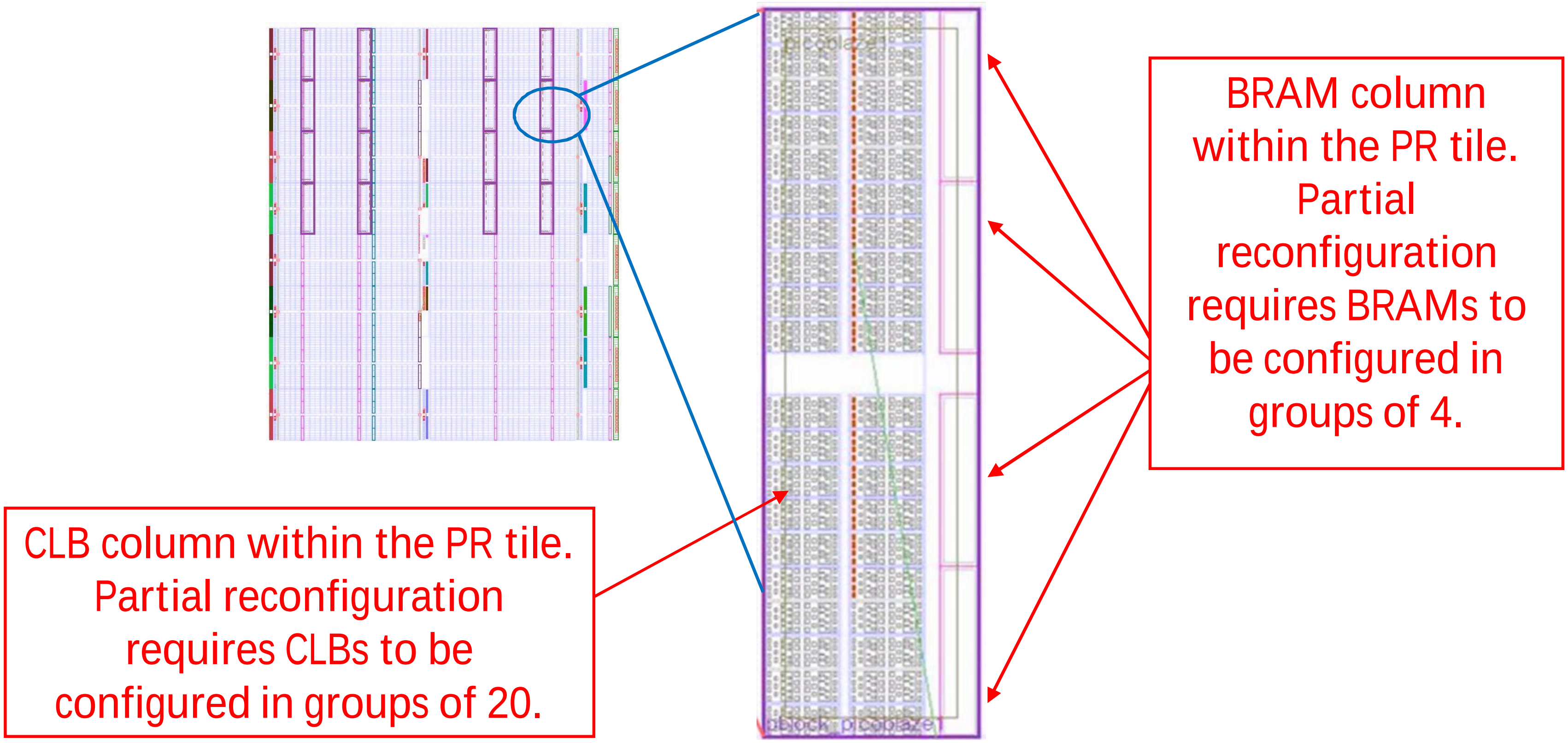
System Demonstration

- **Medium Severity Fault Recovery (SEFI)**

  - An initial hard failure can be *repaired* by going back to the effected processor and reconfiguring it.
  - This handles the situation where an SEU occurred in the configuration RAM
  - For this type of fault, a simple reset will not recover the processor

BUT

the processor hardware is still usable.



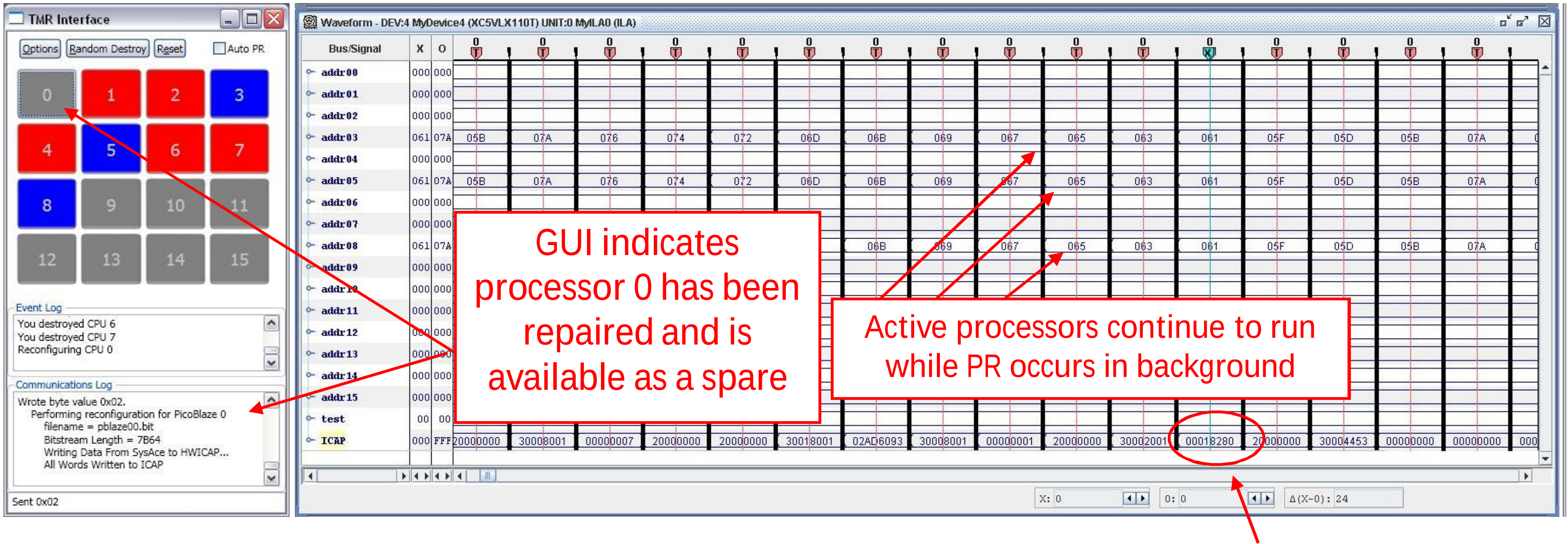
BRAM column within the PR tile. Partial reconfiguration requires BRAMs to be configured in groups of 4.

CLB column within the PR tile. Partial reconfiguration requires CLBs to be configured in groups of 20.

System Demonstration

- **Medium Severity Fault Recovery (SEFI on uP #0)**

  - Repairing Processor 0 using Partial Reconfiguration



You destroyed CPU 6
You destroyed CPU 7
Reconfiguring CPU 0

```
Wrote byte value 0x02.
    Performing reconfiguration for PicoBlaze 0
        filename = pblaze00.bit
        Bitstream Length = 7B64
        Writing Data From SysAce to HWICAP...
        All Words Written to ICAP
```

Sent 0x02

GUI indicates processor 0 has been repaired and is available as a spare

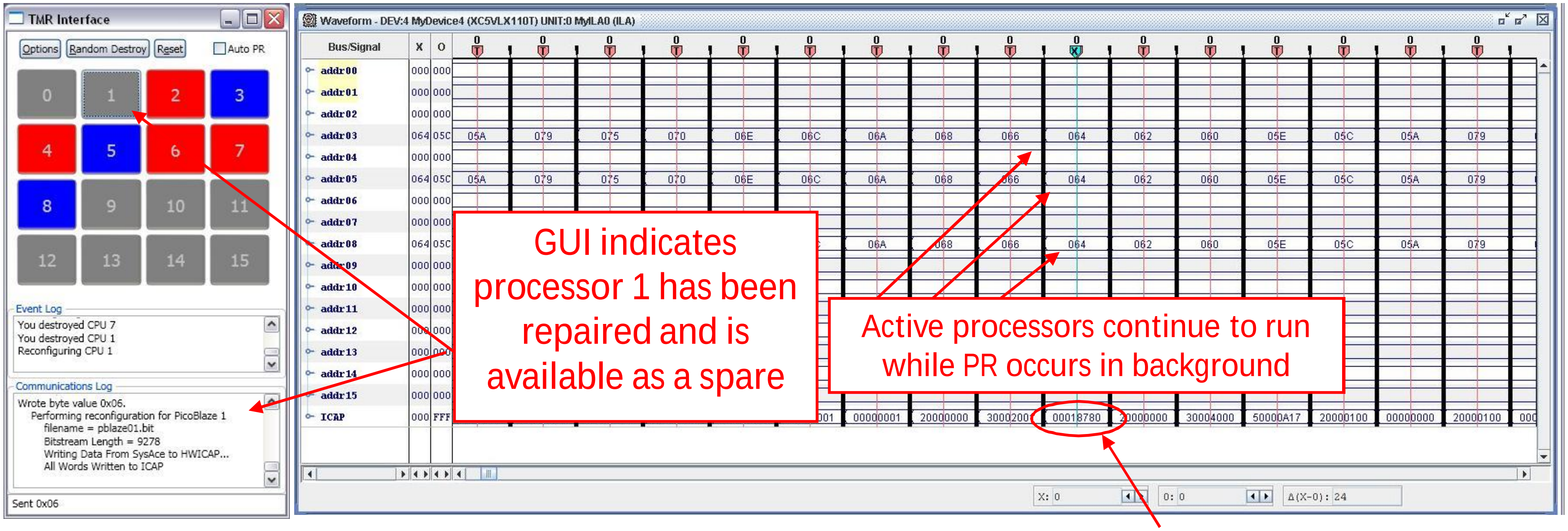
Active processors continue to run while PR occurs in background

ICAP address x00018280 corresponds to partial reconfiguration of Tile 0

System Demonstration

- **Medium Severity Fault Recovery (SEFI on uP #1)**

  - Repairing Processor 1 using Partial Reconfiguration



```
You destroyed CPU 7
You destroyed CPU 1
Reconfiguring CPU 1
```

```
Wrote byte value 0x06.
    Performing reconfiguration for PicoBlaze 1
        filename = pblaze01.bit
        Bitstream Length = 9278
        Writing Data From SysAce to HWICAP...
        All Words Written to ICAP
```

```
Sent 0x06
```

GUI indicates processor 1 has been repaired and is available as a spare

Active processors continue to run while PR occurs in background

ICAP address x00018780corresponds to partial reconfiguration of Tile 1

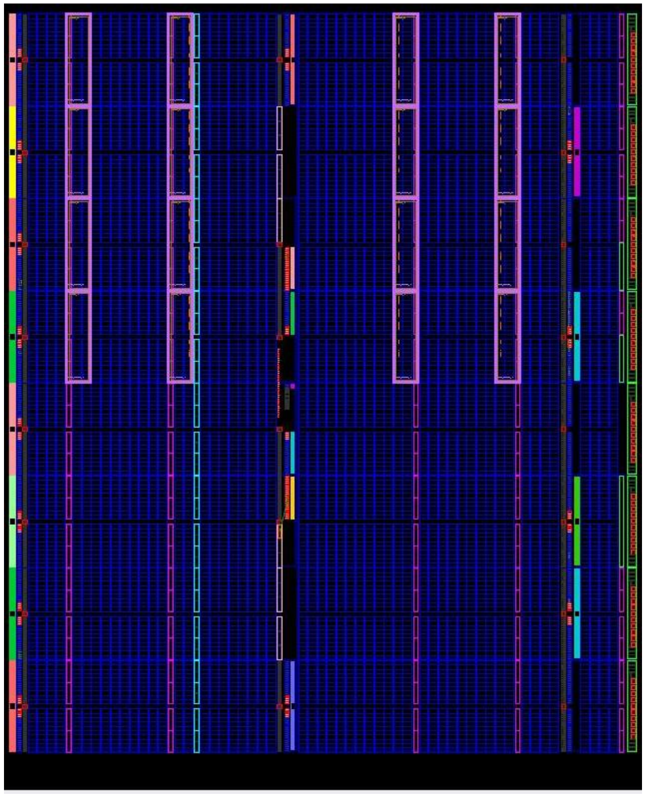
Design of a Radiation Tolerant Computing System
Based on a Many-Core FPGA Architecture

Partial Reconfiguration Constraints

- For our V5, the smallest quantum that can be partially reconfigured is 20 CLBs

  - 1 CLB contains: *2 Slices*

  - 1 Slice contains:
    - *four LUTs*
    - *four storage elements*
    - *wide-function multiplexers*
    - *carry logic*



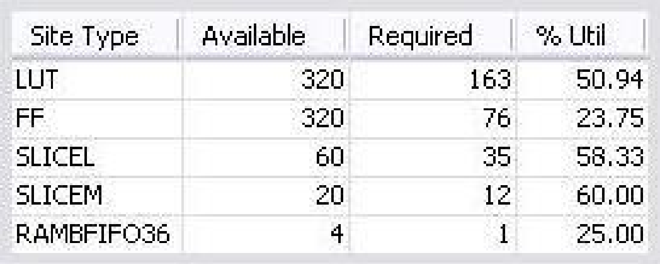
- If you use BRAM in your design, 4 BRAMs must be partially reconfigured together

- Care must be given to placing circuitry within the smallest partially reconfigured tile

- Bus Macros are used to provided fixed routing channels between tiles.

PR of a *picoBlaze* Core

Physical *picoBlaze* resource estimation:



Site Type	Available	Required	% Util
LUT	320	163	50.94
FF	320	76	23.75
SLICEL	60	35	58.33
SLICEM	20	12	60.00
RAMBFIFO36	4	1	25.00

- 24 CLBs, 1 BRAM

PR region resource use:

- 2 columns of 20 CLBs
- 1 column of BRAM

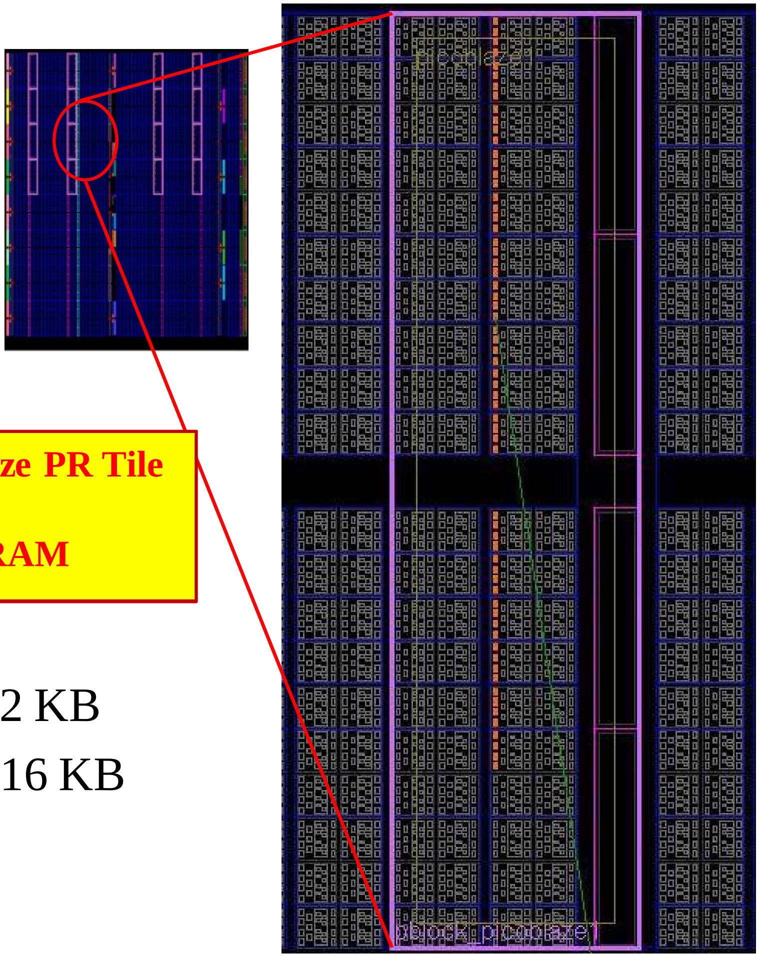
Smallest picoBlaze PR Tile
=
40 CLB + 4BRAM

Bitstream file size(LX50T):

- Partial bitstream for one PicoBlaze: 31.2 KB
- Full bitstream: 1,716 KB

Reconfiguration time:

- Roughly 200 clks/Byte (measured)
- Measured time: **66ms** (100 MHz clk)
- Using MicroBlaze driven ICAP processor



A single PicoBlaze PR region

Questions