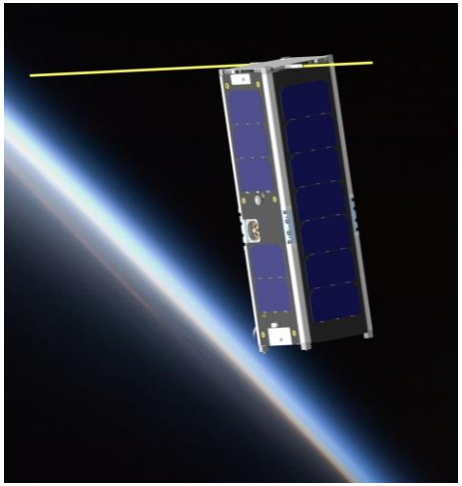
Power Efficiency Benchmarking of a Partially Reconfigurable, Many-Tile System Implemented on a Virtex-6 FPGA

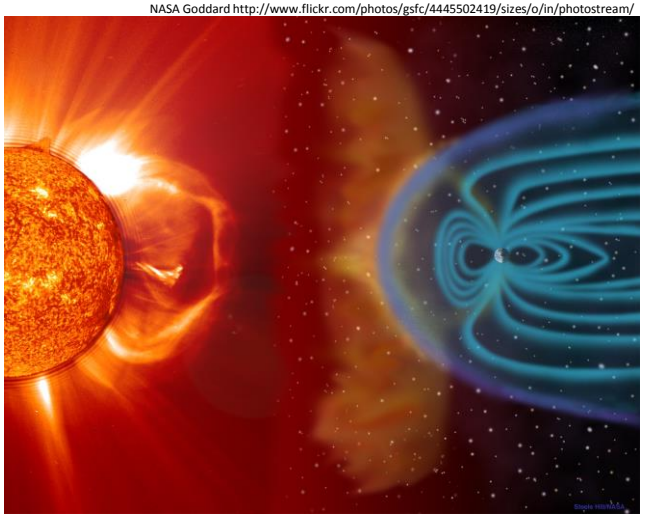


Brock J. LaMeres

Reconfigurable Space Computing

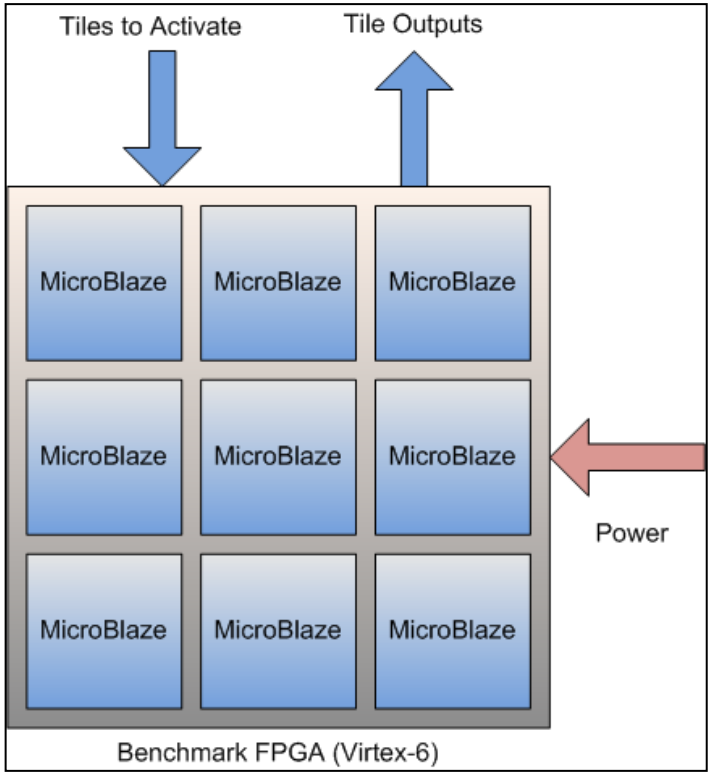
- FPGAs are uniquely suited to increase performance of space computers
- Radiation adversely affects FPGAs
- Reconfigurable computing techniques enable mitigation of radiation faults
- This research looks at improving performance of a custom radiation tolerant space flight computer

NASA Goddard http://www.flickr.com/photos/gsfc/4445502419/sizes/o/in/photostream/

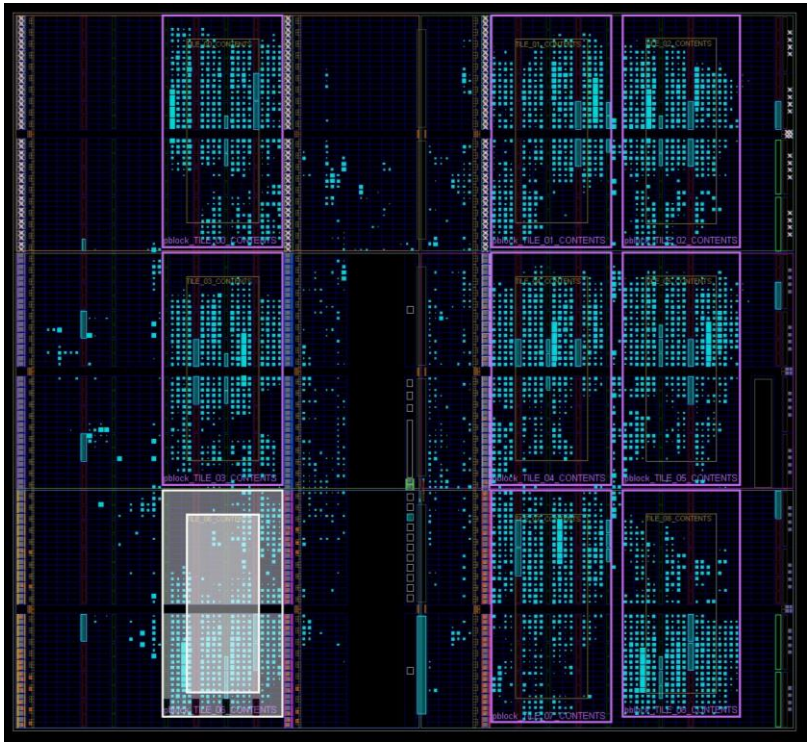


Benchmarking System

Basic system architecture

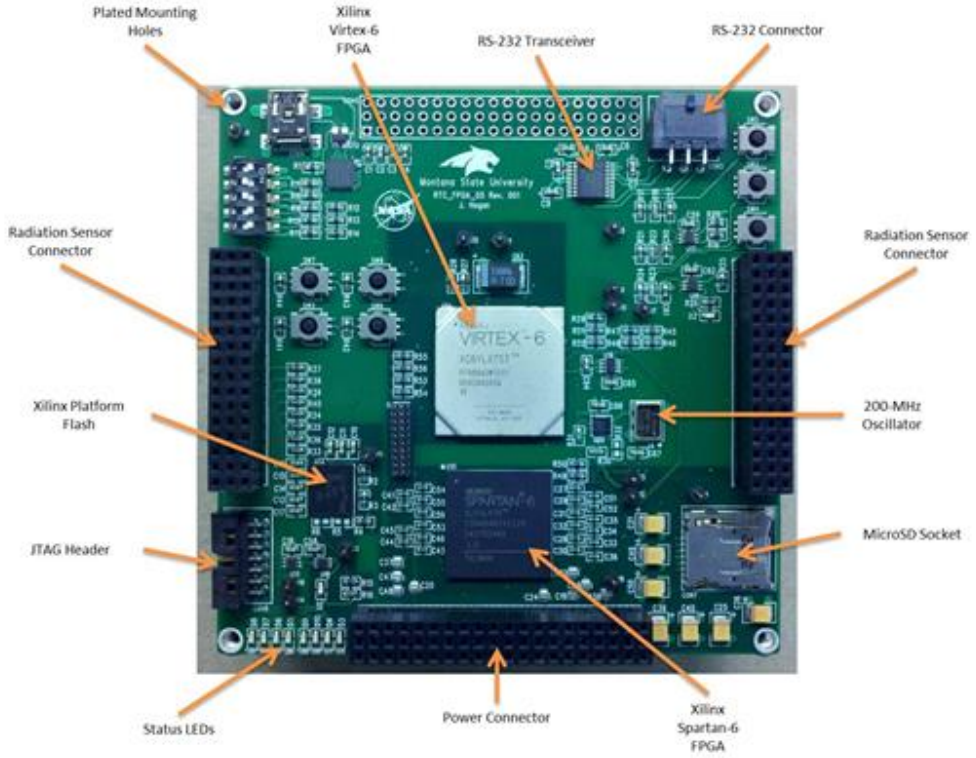


FPGA system floor plan



Research System Hardware

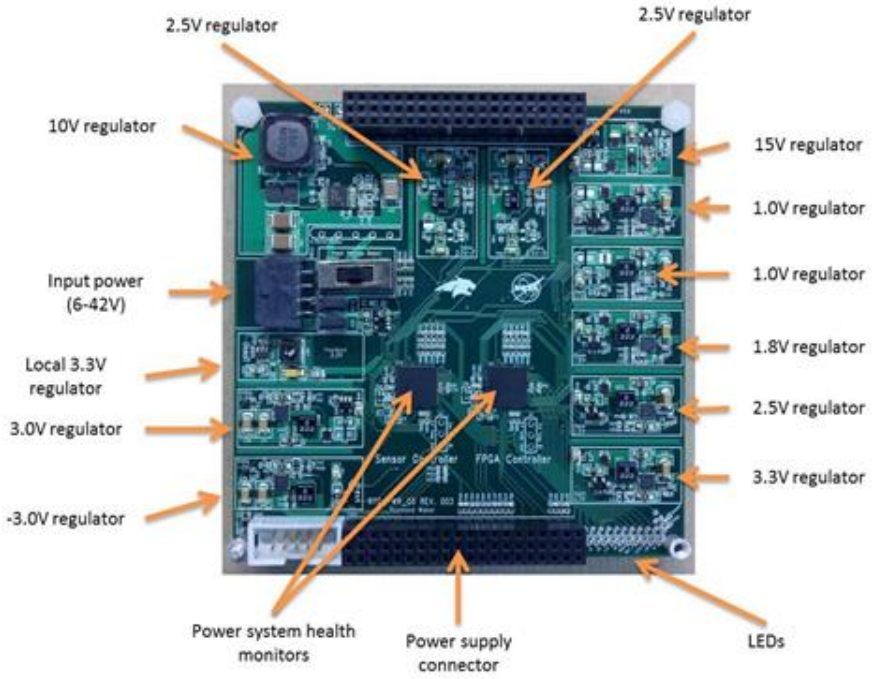
FPGA Computer Board



- Xilinx Virtex-6 XC6VLX75T
- Xilinx Spartan-6 XC6SLX75
- Research systems implemented on Virtex-6
- Control functions implemented on Spartan-6
  - Virtex full and partial reconfiguraion
  - Virtex configuration memory scrubbing
  - USB user interface

Research System Hardware

Power Supply Board



- Real-time voltage, current and power measurement
- 12 dynamically configurable voltage rails
- Over-current detection with automatic shutdown
- 6V to 42V input voltage supply range

Results

- Performed Dhrystone, Whetstone, LINPACK, and NAS-EP benchmarks
  - Native Microblaze ALU
  - Custom FPU for double precision floating point operations
- Measured Performance-per-Watt metric
- Scaled number of hardware cores to demonstrate substantial performance increase with minimal power increase
- Demonstrates benefit of runtime instantiation of hardware accelerators on as-needed basis

NAS-EP performance and power consumption versus number of cores

FPGA Tile Configuration	Results (2^{20} Iterations)			
	Completion Time	Speed Up Over 1 Core	Power Consumption	Power Increase Over 1 Core
1 Core	393 s	-	610mW	-
2 Cores	195 s	202%	618mW	1.3%
3 Cores	131 s	300%	626mW	2.6%
4 Cores	97 s	405%	634mW	3.9%
5 Cores	77 s	501%	642mW	5.2%