

Measuring the Impact of Adaptive Learning Modules in Digital Logic Courses

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Abstract

This paper presents the current status of a research project investigating the use of a novel web-based adaptive learning system to improve student mastery of digital logic concepts while considering the demographics of the individual student. Adaptive learning is a pedagogical approach that dynamically alters the difficulty of content based on an ongoing assessment of the student's capability. This technique is becoming more popular with the advancement of web-based learning solutions and increased student enrollment. Using this type of e-learning environment has the potential to address background deficiencies of students who lack the necessary prerequisite skills coming out of high school. This three-year project is currently in its second year through funding from the National Science Foundation's Improving Undergraduate STEM Education (IUSE). During the first year of this project our team developed a set of course materials and assessment instruments for the area of digital logic. This is content found in all accredited undergraduate electrical and computer engineering curriculums. In year two, our team used the material in a variety of course delivery formats including live, online to on-campus students, online to off-campus students, and online to remote community college students. Data was collected on student performance while also tracking student demographics such as gender, ethnicity, GPA, credits earned, ACT scores, and transfer credits. The data was analyzed to determine if there were any learning outcomes that had significantly lower student performance overall, and if there were any specific student sub-groups that performed lower on any of the outcomes. In year three of the project our team is deploying adaptive learning modules on targeted outcomes to measure their impact. This paper will present the course materials developed during year one, the data and the baseline results collected during year two, and the initial results of the adaptive learning modules. This paper will benefit engineering educators teaching logic circuits/design and are interested in using an online learning environment to either supplement or replace in-class instruction.

Introduction

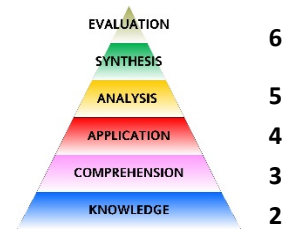
Engineering program enrollments have been increasing steadily for nearly a decade, and instructors are investigating ways to maintain or even improve the quality of the student learning experience in this challenging environment. Adding to the complexity is the wide range of preparedness students have when beginning college. E-learning environments offer one way to supplement face-to-face instruction; designed properly, e-learning can be scalable and can personalize instruction to address background deficiencies. An adaptive e-learning system is an exciting pedagogical tool that can provide individual instruction to students by dynamically altering the difficulty of content based on an ongoing assessment of the students' capability.

In its simplest form, an adaptive learning system consists of a bank of online quiz questions on a particular subject, each with an associated difficulty level. As students answer questions, the difficulty of the next question either increases or decreases based on the students' response. In a more comprehensive form, additional targeted instruction can be provided if students answer questions incorrectly. Additionally, more thought-provoking material can be presented to students who consistently answer questions correctly, providing challenge to students when

appropriate. Individualized, computer-based, adaptive learning has been shown to be nearly as effective as a live instructor guiding the student through the material when implemented carefully [1,2]. Most course management systems (i.e., Desire2Learn, Moodle, Blackboard) support question banks that are dynamically assigned based on difficulty and continual student assessment. Thus, the infrastructure to exploit adaptive learning systems for personalized instruction has greatly improved over the last decade.

Part 1 – Creating Curriculum Materials to Measure a Baseline of Understanding

The first portion of this project was to define the overall learning objectives and specific learning outcomes for students in introductory digital logic courses. The following figure shows the learning objectives and outcomes defined for this project. For each outcome, the associated learning category within Bloom’s Taxonomy. The taxonomy becomes important when designing the assessment tools to measure each learning outcome as they guide what information is actually being assessed.



Learning Objective <i>The overall learning goal of this module is to:</i>	Learning Outcome <i>After completing this module, a student will be able to:</i>	Learning Category					
		1	2	3	4	5	6
Module 1: To understand the basic principles of analog and digital systems.	1.1: Describe the fundamental differences between analog and digital systems.	x					
	1.2: Describe advantages of digital systems compared to analog systems.	x					
Module 2: To understand the basic principles of binary number systems.	2.1: Describe the formation and use of positional number systems.		x				
	2.2: Convert numbers between different bases.			x			
	2.3: Perform binary addition and subtraction by hand.			x			
	2.4: Use twos complement numbers to represent negative numbers.			x			
Module 3: To understand the basic electrical operation of digital circuits.	3.1: Describe the functional operation of a basic logic gate using truth tables, logic expressions, and logic waveforms.	x					
	3.2: Analyze the DC and AC behavior of a digital circuit to verify it is operating within specification.				x		
	3.3: Describe the meaning of a logic family and the operation of the most common technologies used today.	x					
	3.4: Determine the operating conditions of a logic circuit when driving various types of loads.				x		

Module 4: To understand the basic principles of combinational logic design.	4.1: Describe the fundamental principles and theorems of Boolean algebra and how to use them to manipulate logic expressions.		x				
	4.2: Analyze a combinational logic circuit to determine its logic expression, truth table, and timing information.				x		
	4.3: Synthesize a logic circuit in canonical form (Sum of Products or Product of Sums) from a functional description including a truth table, minterm list, or maxterm list.					x	
	4.4: Synthesize a logic circuit in minimized form (Sum of Products or Product of Sums) through algebraic manipulation or with a Karnaugh map.					x	
	4.5: Describe the causes of timing hazards in digital logic circuits and the approaches to mitigate them.		x				
Module 5: To understand the basic principles of hardware description languages.	5.1: Describe the role of hardware description languages in modern digital design.		x				
	5.2: Describe the fundamentals of design abstraction in modern digital design.		x				
	5.3: Describe the modern digital design flow based on hardware description languages.		x				
	5.4: Describe the fundamental constructs of VHDL.		x				
	5.5: Design a VHDL model for a combinational logic circuit using concurrent modeling techniques (signal assignments and logical operators, conditional signal assignments, and selected signal assignments).					x	
	5.6: Design a VHDL model for a combinational logic circuit using a structural design approach.					x	
	5.7: Describe the role of a VHDL test bench.		x				
Module 6: To understand the basic principles of medium scale integrated circuit logic.	6.1: Design a decoder circuit using both the classical digital design approach and the modern HDL-based approach.					x	
	6.2: Design an encoder circuit using both the classical digital design approach and the modern HDL-based approach.					x	
	6.3: Design a multiplexer circuit using both the classical digital design approach and the modern HDL-based approach.					x	
	6.4: Design a demultiplexer circuit using both the classical digital design approach and the modern HDL-based approach.					x	

Module 7: To understand the basic operation of sequential logic circuits.	7.1: Describe the operation of a sequential logic storage device.		x				
	7.2: Describe sequential logic timing considerations.		x				
	7.3: Design a variety of common circuits based on sequential storage devices (toggle flops, ripple counters, switch debouncers, and shift registers).						x
	7.4: Design a finite state machine using the classical digital design approach.						x
	7.5: Design a counter using the classical digital design approach and using an HDL-based, structural approach.						x
	7.6: Describe the finite state machine reset condition.		x				
	7.7: Analyze a finite state machine to determine its functional operation and maximum clock frequency.				x		
Module 8: To understand the full capability of hardware description languages.	8.1: Describe the behavior of a VHDL process and how it is used to model sequential logic circuits.		x				
	8.2: Model combinational logic circuits using a process and conditional programming constructs.						x
	8.3: Describe how and why signal attributes are used in VHDL models.		x				
	8.4: Design a finite state machine using the classical digital design approach.						x
	8.5: Describe the capabilities provided by the most common VHDL packages.		x				
Module 9: To understand how hardware description languages can be used to create behavioral models of synchronous digital systems.	9.1: Design a VHDL behavioral model for a sequential logic storage device.						x
	9.2: Describe the process for creating a VHDL behavioral model for a finite state machine.		x				
	9.3: Design a VHDL behavioral model for a finite state machine.						x
	9.4: Design a VHDL behavioral model for a counter.						x
	9.5: Design a VHDL register transfer level (RTL) model of a synchronous digital system.						x
Module 10: To understand the basic principles of semiconductor-based memory systems.	10.1: Describe the basic architecture and terminology for semiconductor-based memory systems.		x				
	10.2: Describe the basic architecture of non-volatile memory systems.		x				
	10.3: Describe the basic architecture of volatile memory systems.		x				
	10.4: Design a VHDL behavioral model of a memory system.						x

Module 11: To understand the basic principles of programmable logic devices.	11.1: Describe the basic architecture and evolution of programmable logic devices.		x				
	11.2: Describe the basic architecture of Field Programmable Gate Arrays (FPGAs).		x				
Module 12: To understand the basic principles of binary arithmetic circuits.	12.1: Design a binary adder using both the classical digital design approach and the modern HDL-based approach.					x	
	12.2: Design a binary subtractor using both the classical digital design approach and the modern HDL-based approach.					x	
	12.3: Design a binary multiplier using both the classical digital design approach and the modern HDL-based approach.					x	
	12.4: Design a binary divider using both the classical digital design approach and the modern HDL-based approach.					x	
Module 13: To understand the basic principles of a computer system.	13.1: Describe the basic components and operation of computer hardware.		x				
	13.2: Describe the basic components and operation of computer software.		x				

Figure 1. Learning Objectives and Outcomes in Digital Logic Developed for this Project

The next step was to design course materials to teach these objectives. To accomplish this a new textbook was developed and an associated set of short lecture videos were created. These tools were used to teach the material in both live and online versions of the courses. The following figure shows an example of the course materials created in this project.



Figure 2. Materials Developed to Teach the Digital Logic Learning Objectives/Outcomes.

Part 2 – Measuring the Baseline Level of Understanding

Over 600 assessment tools were created to measure student performance across all 55 learning outcomes. Approximately 400 of these were in the form of auto-graded, multiple choice quiz questions that were administered by the Desire2Learn course management system. Approximately 200 of these were VHDL design/simulations that were manually graded by the course instructor. The following figure shows an example of the assessment tools created to measure the baseline of student understanding.

The image shows two screenshots from a course management system. The left screenshot is a quiz question titled "Question 13 (1 point)" from "HW 4.4 - Combinational Logic Minimization - Quiz". It asks for the minimal sum of products (SOP) logic expression for a 4-input truth table. The truth table is:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	X
0	0	1	1	1
0	1	0	0	X
0	1	0	1	0
0	1	1	0	X
0	1	1	1	X
1	0	0	0	X
1	0	0	1	0
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

The right screenshot is a VHDL assignment titled "HW 8.2 - Conditional Programming Constructs" and "Problem 8.2.1". It asks for a VHDL model to implement a 4-input truth table. The truth table is:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Figure 3. Assessment Tools Developed to Measure the Digital Logic Learning Objectives/Outcomes.

Data was collected across multiple offerings of the 200-level course that covers learning objectives 1-7 and one offering of the 300-level course that covers learning objectives 8-13. Students were asked to complete a consent form so that demographic information could be collected and correlated to their scores. The following shows the overall performance on each outcome.

Performance on Learning Outcomes "200-Level + 300-Level Logic Courses"

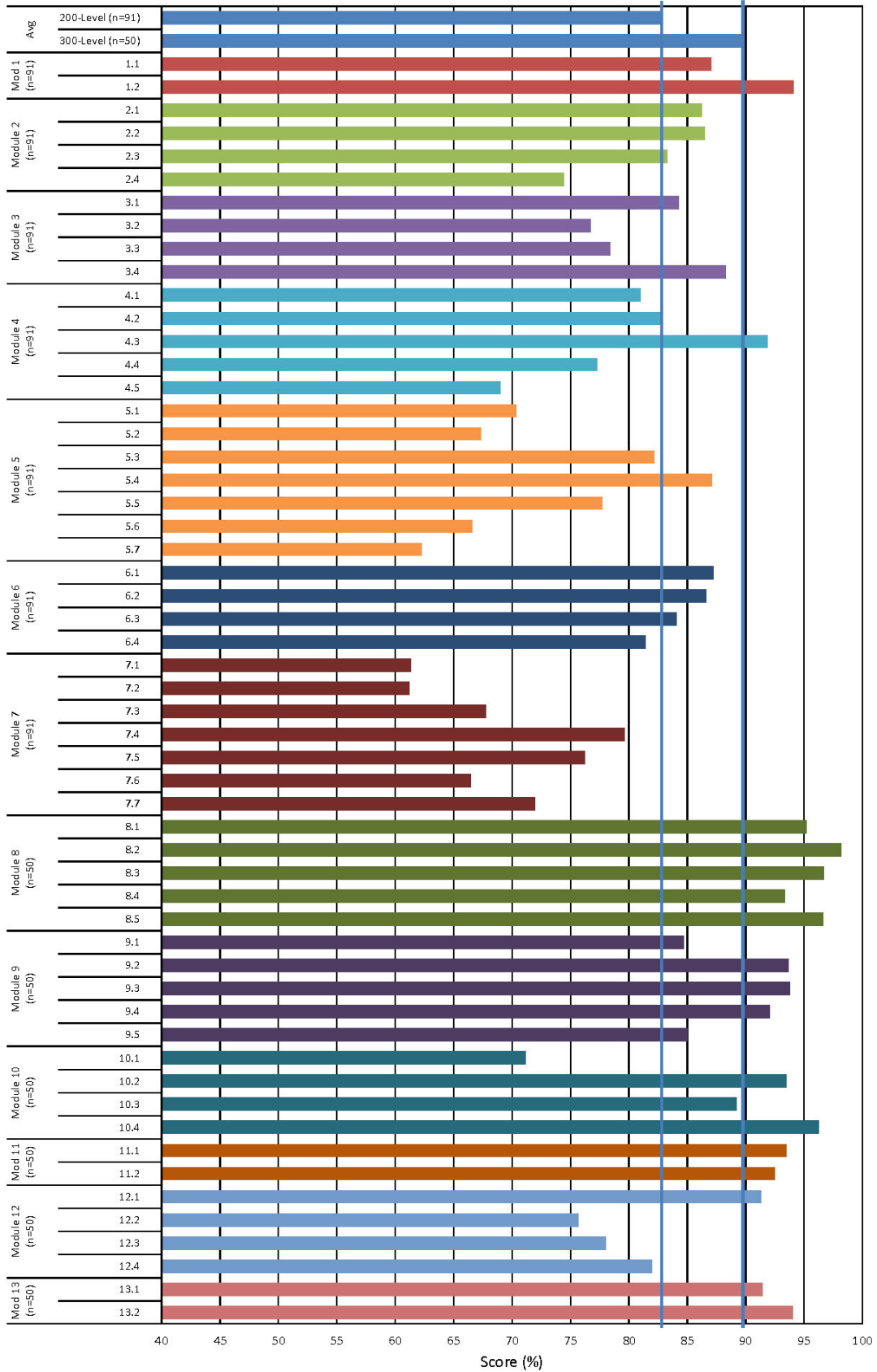


Figure 4. Baseline of Understanding on All Learning Outcomes.

From this data, outcomes 4.4 and 5.5 were selected for intervention. This was due to a variety of factors including lower than average performance, relative cognitive difficulty, and that they resided within the 200-level course, which had more data points. The following two figures show the breakdown of performance across all of the variables studied in this analysis. These plots are of the baseline data.

Performance on Learning Outcome "4.4: Combinational Logic Minimization"

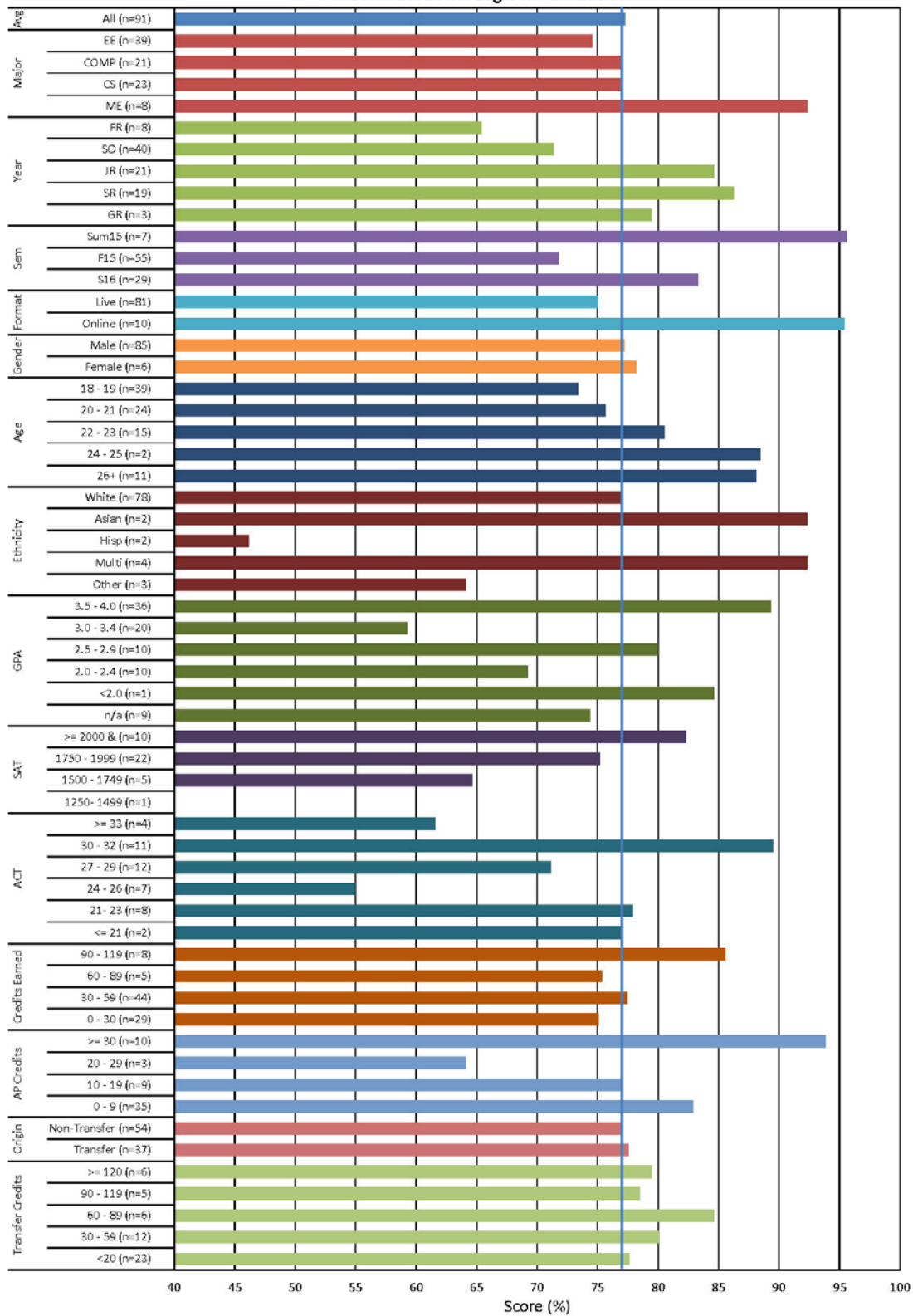


Figure 5. Baseline of Understanding on Learning Objective 4.4.

Performance on Learning Outcome "5.5: Concurrent Modeling Techniques in VHDL"

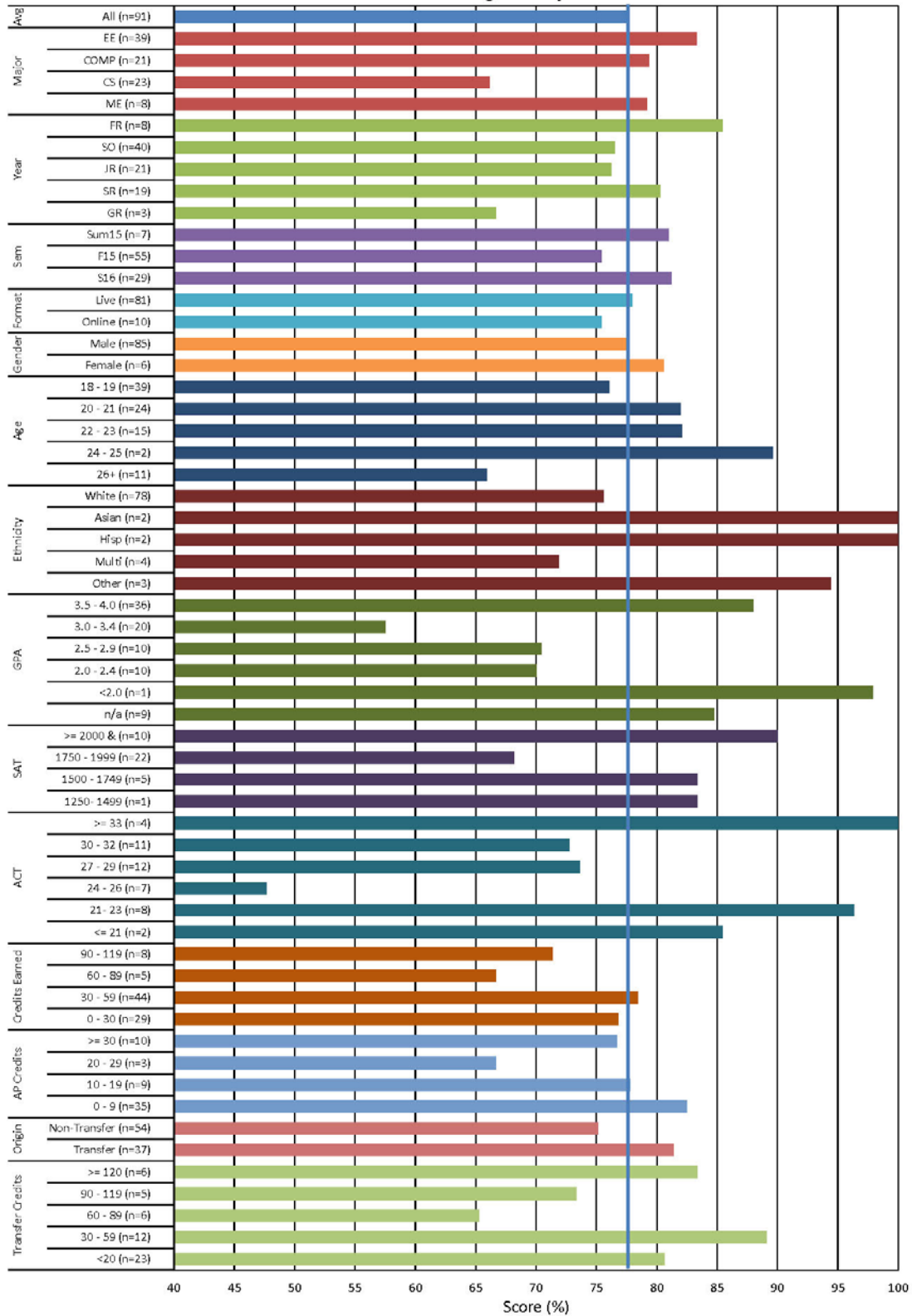
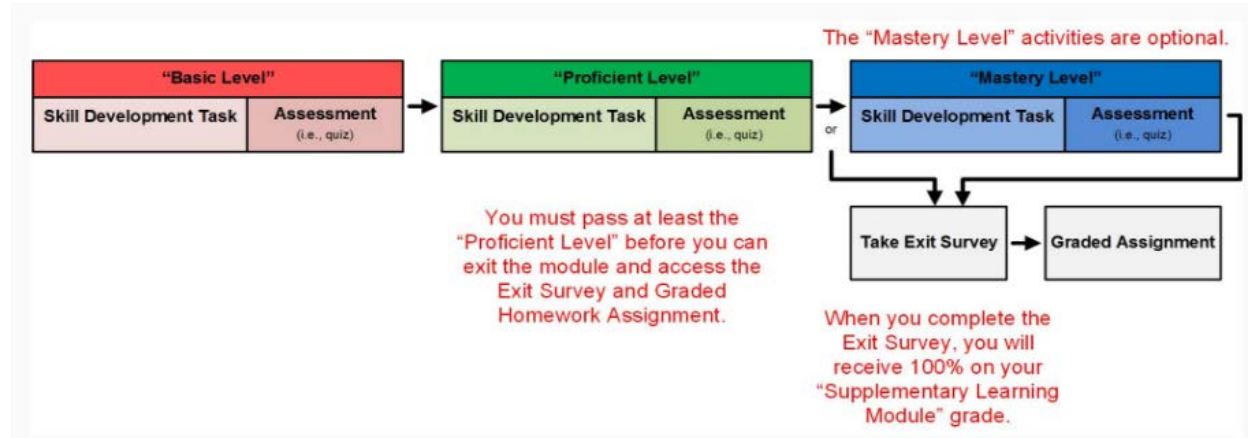


Figure 6. Baseline of Understanding on Learning Objective 5.5.

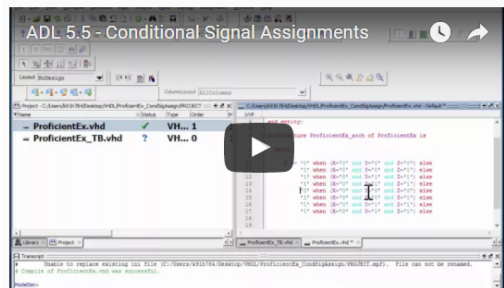
Part 3 – Creating Adaptive Learning Modules for 4.4 and 5.5

Two adaptive learning activities were created and deployed in the fall semester of 2016 in the 200-level digital logic course. The following figure shows an example of the content developed.



Design Example - Conditional Signal Assignments

Now let's design and simulate a model for the **ProficientEx** system using conditional signal assignments. The test bench will be the same as above. Follow along with the video and see if you can produce the same simulation result.

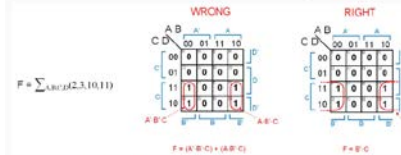


K maps with Circles That Wrap Around

Another common mistake that is made when using K-maps is not identifying groupings that occur along the borders of the grid. Notice that the left and right columns are considered "neighboring cells" because the input codes only differ by 1-bit in their input codes. Specifically, the leftmost column corresponds to AB=00 and the rightmost column corresponds to AB=10. This allows groupings to be formed between these columns. These are often called "wrap arounds" because of the way the circles are drawn.

Let's look at the following example. In this 4-input circuit, the functionality is described using a minterm list. The outputs are asserted for cells 2, 3, 10, and 11. If you don't recognize that the outer columns are neighbors, you may mistakenly form two circles, one for cells 2 & 3 and another for cells 10 & 11. While this is a valid circuit, it is not the most minimal.

The correct solution is to form a cell that "wraps around" the K-map and encompasses all four cells.



Keep in mind that the top and bottom cells are also neighboring cells. That means you can also wrap around the top/bottom in addition to the left/right.

Now you try...

Given the 4-input minterm list, use a K-map to derive the minimal SOP logic expression

$$F = \sum_{A,B,C,D} (4,6,12,14)$$

Hint: The circle wraps around the top/bottom.

SOLUTION: $F = B'D'$

Figure 7. Adaptive Learning Material Developed.

Part 4 – Analyzing the Impact of the Adaptive Learning Interventions.

The Adaptive Learning Modules (ADL) improved the performance of some students on the two outcomes, 4.4 and 5.5. The effect of the intervention was dampened by an overall ceiling effect of the scores on the two homework assignments associated with the outcomes. The overall means for the baseline (BL) group and the experimental (EXP) group are given below for both outcomes. The total number of points possible for both homework assignments was 100:

Outcome	Baseline Mean	Experimental Mean
4.4	89.86 (n=88)	91.98 (n=71)
5.5	95.29 (n= 81)	95.02 (n= 67)

Table 1. Mean Performance on Targeted Outcomes (Baseline vs. Experimental).

In regard to gender, we had too few female students to conduct any statistical tests. The means for males and females for outcomes 4.4 and 5.5 both BL and EXP are shown in the table below. Females scored quite a bit lower than males on outcome 4.4, but slightly better than males on outcome 5.5.

Outcome	Gender	Baseline	Experimental
4.4	Male	90.60 (n= 81)	92.90 (n=65)
	Female	81.32 (n=7)	82.10 (n=6)
5.5	Male	95.20 (n=76)	94.91 (n=63)
	Female	96.67 (n=5)	96.88 (n=4)

Table 2. Mean Grade vs. Gender on Targeted Outcomes (Baseline vs. Experimental).

Using the General Linear Model, which is an ANOVA procedure in which the calculations are performed using a least squares regression approach to describe the statistical relationship between one or more predictors and a continuous response variable, we analyzed the Baseline (BL) and Experimental (EXP) results to determine if the intervention affected lower-GPA students differently than the higher-GPA students. We grouped the students into the following groups:

- Group 1: 3.5-4.0 GPA
- Group 2: 3.0-3.4 GPA
- Group 3: 2.5-2.9 GPA
- Group 4: 2.0-2.4 GPA
- Group 5: < 2.0 GPA

When these groups and BL/EXP were used as independent variables and the 4.4 outcome was used as the dependent variable, we found a significant interaction ($F = 2.89; p = .038$). See the table below for detailed results.

Analysis of Variance for HW 4.4, using Adjusted SS for Tests						
Source	DF	Seq SS	Adj SS	Adj MS	F	P
MSU GPA Group	3	581.2	604.5	201.5	1.72	0.165
BL or EXP	1	120.6	47.7	47.7	0.41	0.524
MSU GPA Group*BL or EXP	3	1013.5	1013.5	337.8	2.89	0.038
Error	131	15311.6	15311.6	116.9		
Total	138	17026.9				

S = 10.8112 R-Sq = 10.07% R-Sq(adj) = 5.27%

Table 3. ANOVA Results on Outcome 4.4 with GPA Groups as Independent Variables.

The table below shows the means and BL and EXP scores for all GPA groups. From these means, the source of the interaction is fairly clear: Group 2 scores actually went down from the BL to the EXP groups, and Group 3 scores went up.

GPA group	BASELINE	EXPERIMENTAL
1: 3.5-4.0	92.1 (n=37)	94.65 (n=23)
2: 3.0-3.4	92.79 (n=16)	87.63 (n=23)
3: 2.5-2.9	83.08 (n=15)	93.33 (n=15)
4: 2.0-2.4	89.42 (n=8)	88.46 (n=2)
5: < 2.0	85 (n=2)	85 (n=1)

Table 4. Mean Grade vs. GPA Groups on Outcome 4.4 (Baseline vs. Experimental).

Post hoc Tukey procedure tests of the difference of means produced no significant results. The Tukey tests were followed by independent sample t-tests, with no assumption of equal variance. The t-tests did produce a significant difference between the BL and EXP scores of GPA group 3 ($t = -2.15; p = .044$). The number of students in each of these groups was relatively small: 15 in the BL group and 8 in the EXP group. The mean score for 4.4 for the BL group was 83.08 (sd = 24.00), and the mean for the EXP group was 93.27 (sd = 8.66). The table below details these results:

Two-sample T for 4.4b				
BL or EXPER	N	Mean	StDev	SE Mean
1	15	83.1	14.0	3.6
2	8	93.27	8.66	3.1

Difference = mu (1) - mu (2)
 Estimate for difference: -10.19
 95% CI for difference: (-20.08, -0.31)
 T-Test of difference = 0 (vs not =): T-Value = -2.15 P-Value = **0.044** DF = 20

Table 5. Two-Sample T-Test Results on Grade vs. GPA Groups on Outcome 4.4 (Baseline vs. Experimental).

The GPA groupings also showed a significant interaction in the same General Linear Model analysis for outcome 5.5 ($p = .05$). The table below shows the details of this analysis:

Analysis of Variance for HW 5.5, using Adjusted SS for Tests						
Source	DF	Seq SS	Adj SS	Adj MS	F	P
MSU GPA Group	3	2018.1	2041.0	680.3	4.54	0.005
BL or EXP	1	103.5	25.5	25.5	0.17	0.681
MSU GPA Group*BL or EXP	3	1201.1	1201.1	400.4	2.67	0.051
Error	119	17829.2	17829.2	149.8		
Total	126	21152.1				

S = 12.2403 R-Sq = 15.71% R-Sq(adj) = 10.75%

Table 6. ANOVA Results on Outcome 5.5 with GPA Groups as Independent Variables.

For outcome 5.5, the means for all GPA groups are given in the table below. Again the source of the interaction is fairly clear: GPA Group 2 had a positive gain from BL to EXP, and gpa Group 3 actually went down.

GPA group	BASELINE	EXPERIMENTAL
1: 3.5-4.0	99.02 (n=34)	98.48 (n=22)
2: 3.0-3.4	86.67 (n=15)	97.73 (n=22)
3: 2.5-2.9	92.01 (n=12)	86.22 (n=13)
4: 2.0-2.4	99.7 (n=7)	100 (n=2)
5: < 2.0	49 (n=2)	100 (n=1)

Table 7. Mean Grade vs. GPA Groups on Outcome 5.5 (Baseline vs. Experimental).

As with outcome 4.4, post hoc Tukey procedure tests of the difference of means produced no significant results. Follow-up independent sample t-tests, with no assumption of equal variance, also did not produce significant results. The results for Group 2 were $t = -1.64$ and $p = .122$. The table below shows these results.

Two-sample T for 5.5a				
BL or EXPE	N	Mean	StDev	SE Mean
1	15	86.7	25.4	6.5
2	22	97.73	7.79	1.7

Difference = mu (1) - mu (2)
 Estimate for difference: -11.06
 95% CI for difference: (-25.46, 3.34)
 T-Test of difference = 0 (vs not =): T-Value = -1.64 P-Value = 0.122 DF = 15

Table 8. Two-Sample T-Test Results on Grade vs. GPA Groups on Outcome 5.5 (Baseline vs. Experimental).

Using the General Linear Model, analyses were also conducted to find out if the intervention affected non-white students differently than white students and non-transfer students differently than transfer students. No significant differences were found. We also analyzed the data by major grouping (electrical engineering, computer engineering, computer science, mechanical engineering, and other) and found no significant differences.

Conclusion

This paper presented the current state of an NSF IUSE project that is studying the impact of deploying adaptive learning modules in digital circuits courses. Our research team has defined detailed learning outcomes for a sequence of courses in digital logic and created a comprehensive set of curriculum tools to teach the material. A baseline of understanding was collected using 600 new assessment tools to identify the most difficult outcomes. Two outcomes were selected for intervention: 4.4 – Combinational Logic Minimization and 5.5 – Concurrent Modeling in VHDL. Two adaptive learning activities were created and used in the fall semester of 2016. An analysis was completed to evaluate if the interventions had any statistically significant impact on student performance. We discovered that the intervention on outcome 4.4 had a significant impact on students with GPA's between 2.5-2.9 on a 4 point scale. No other impact was discovered. The next step in this project is to refine the adaptive learning activities based on this data and a focus group that was held in fall of 2016. Also, more outcomes will be targeted to provide additional data points.

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