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Connectorless Logic Analyzer Probing – Mechanical and Electrical Advantages

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Abstract

Logic Analysis is a powerful tool in aiding engineers while debugging digital systems. As system data rates continue to increase, making a successful logic analyzer measurement is becoming more and more difficult. The physical connection between the logic analyzer and the target PCB is now a major concern for engineers. The industry standard connection for logic analyzers over the past 10 years has been the Mictor connector. While this connector provides the high density connection desired, its electrical loading and mechanical reliability make it ill-suited for today's systems. Connectorless probing has emerged as the new industry standard to replace the Mictor connector. This new technology offers a host of electrical and mechanical advantages over the Mictor connector. This paper will describe the details of why this technology is superior and aid engineers in making a decision on when to upgrade to this new methodology.

Author(s) Biography

Brock J. LaMeres received his BSEE from Montana State University in 1998 and his MSEE from the University of Colorado in 2001. He is currently a Ph.D. candidate at the University of Colorado where his research focus is VLSI Circuit Design and High-Speed I/O for next generation IC's. For the past 6 years he has worked as a hardware design engineer for Agilent Technologies in Colorado Springs where he designs logic analyzer probes and acquisition boards. LaMeres has published 25 technical articles in the area of signal integrity and has a patent in the field of logic analyzer probing. LaMeres is a registered Professional Engineer in the State of Colorado.

Brent A. Holcombe received his BSME from the University of Washington in 1996. He is currently working on his Masters in Engineering Management from the University of Colorado, Boulder. For the past 8 years he has worked as a R&D Mechanical Engineer focused on development of high speed digital probing systems for multi channel test and measurement devices used to test computer systems. Brent has been issued 5 patents and has 5 patents pending in the area of Digital Probing design.

George M. Marshall received his BSEE in 1984 and his MSNE in 1987 from Louisiana State University. For the past 4 years he has worked as a product design engineer on cable assembly designs for Precision Interconnect, a Tyco Electronics company located in Portland, Oregon. George is a registered Professional Engineer in the State of Oregon.

I. Introduction

In order to make a high-density logic analyzer probing connection, digital system designers have traditionally had to place Mictor connectors on their PCB. The signals of interest on the target board are routed to the Mictor connector to be observed by a logic analyzer. The logic analyzer probe, whose interconnect consists of a mating Mictor connector, is then plugged into the target and logic analysis is performed. While this interconnect methodology has been sufficient for the past decade, today's data rates are pushing the limitations of the Mictor Connector. The physical structure of the Mictor connector possesses large electrical parasitics which load the target system and reduce the maximum speed of the logic analyzer. In addition, the combination of fine-pitch surface-mount and through-hole technology required to mount the connector make it sub-optimal for hand loading in the lab or in the field. This results in the Mictor needing to be machine loaded, which adds additional supply chain management and makes post production probing difficult.

Today's new connectorless probing technology addresses these limitations and is being adopted as the new industry standard for logic analysis probing. In connectorless probing, the designer includes surface mount pads on the target system that the signals of interest are routed to. The logic analyzer probe has compression interconnect that makes contact with the SMT pads and forms the electrical connection. A separate mechanical retention module is placed on the target PCB that aligns and retains the compression interconnect onto the SMT pads. This new methodology reduces the electrical loading on the target by reducing the physical structure of the interconnect. In addition, by eliminating the fine-pitch SMT pads of a Mictor connector, machine loading is not required. This simplifies the supply chain associated with having probe points on the board. In addition, post production probing is now enabled due to the simplicity of loading the retention module.



Figure 1. Physical Connection of a Connectorless Probing Technology

This paper describes the mechanical and electrical advantages of connectorless logic analyzer probing. Comparisons are made to the existing Mictor connector to present the improvements made in this new technology.

II. Mechanical Advantages of Connectorless Probing

Connectorless probing offers a number of mechanical advantages over traditional connector based probing. These advantages include simplification of the supply chain for printed circuit board components, the flexibility to probing on a target board post manufacturing, and increased mechanical reliability for probing on multiple PCB plating finishes.

A. Supply Chain Simplification

Until now, digital system designers have had two options for probing with a logic analyzer. The first is to include connectors in the design and have them loaded in the surface mount technology (SMT) process. The second is to attach flying leads to package pins or solder them to exposed pads and traces. Including a connector on the PCB requires a commitment to board real estate and the coordination to ensure that the part is available, purchased, and loaded onto the PCB. Using flying leads can sometimes be difficult when accessing large numbers of signals in small geographical regions.

Connectorless probing involves turning the printed circuit board into one half of the probing interconnect. This can essentially eliminate the need to include probing related components on the bill of materials for the PCB. This greatly reduces the supply chain headaches that are typically associated with making the decision to include probing capability early on. With connectorless probing, the PCB designer needs only to place and route signals to a non-intrusive footprint comprised of landing pads and small retention holes.

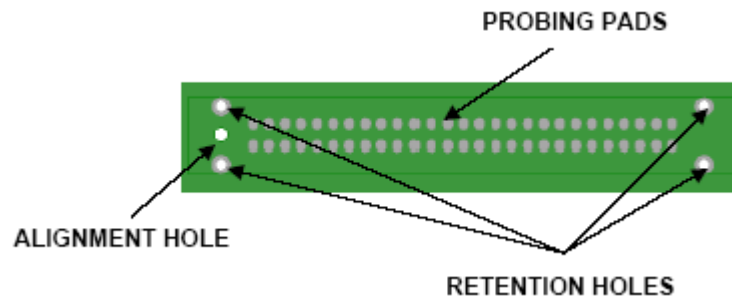


Figure 2. Footprint on Target PCB for Connectorless Probe

The footprint requires no planning, purchasing or logistical coordination with other parts of the manufacturing organization. Before connectorless technology, the designer would be forced to commit to probing capability before the PCB was loaded with components. Now the designer has the flexibility to enable it after getting boards back from the load shop. This enabling is done by simply adding a small plastic retention mechanism (RM) with the use of a standard soldering iron found in most labs. Once the RM is soldered down, the connectorless probe can be attached and used to capture signals. Compare the ease of installation of soldering down the RM with attempting to hand solder a hundred or more fine pitch connector leads by hand.

B. Post-Production Probing

The non-intrusive nature of connectorless technology enables engineers to leave the footprint in a production design. This allows designers to include probing capability at any point in the future after the product has been released. This helps reduce the cost associated with probing. For higher volume printed circuit boards, it is not cost effective to include even one extra connector on every board for probing. Now with connectorless probing, designers are no longer forced to make a cost trade off for debug. A product can ship with only the footprint on the board, which costs only the time to route signals to the pads. In the event that debug is needed in the field, all that is needed is to solder the RM onto the board and attach the probe.

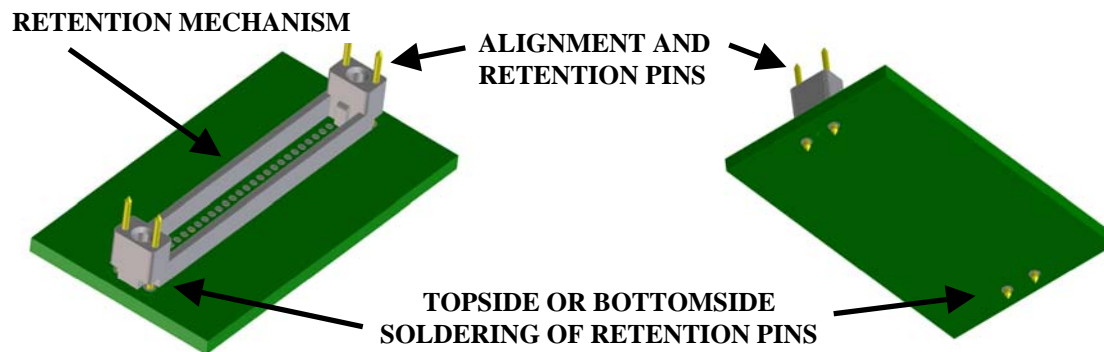


Figure 3. Process for attaching the Retention Module for Connectorless Probes

C. Mechanical Reliability

Not all products requiring debug and validation ever leave the lab. In many situations, the probing paradigm is one of developing large test systems with multiple probe points where probes are mated and de-mated hundreds of times. Connector-based probes are limited by a maximum number of mate and de-mate cycles before the connector is no longer capable of making reliable contact. This limit is typically around 50 – 100 cycles. This cycle limit can be reached quickly in a debug environment where probe cables are being shared across multiple platforms as a cost saving measure. The problem comes when a connector on a test board must be replaced due to damage from over cycling it. This puts the user back into the position where they must hand load a replacement connector. Not only is this a logistical challenge, but also creates the possibility that pins could be solder-shorted together, introducing false errors into the tests being run. Additionally, this limited number of cycles will damage the mating connector on the probe as well, requiring that replacement probes be purchased, increasing the overall cost of debug. Connectorless probing solves this cycle limit problem in two different ways. First, the interconnect used in a connectorless probe can typically be used for thousands of cycles as opposed to just hundreds. Second, since there is no connector on the board, there is nothing to replace. The compression interconnect on a connectorless probe has

up to .025” of compliance, capable of absorbing the variability of pads coated with HASL finish. It also has the ability to pierce through oxides and contaminates on the pad eliminating the need for cleaning of the surface to be probed.

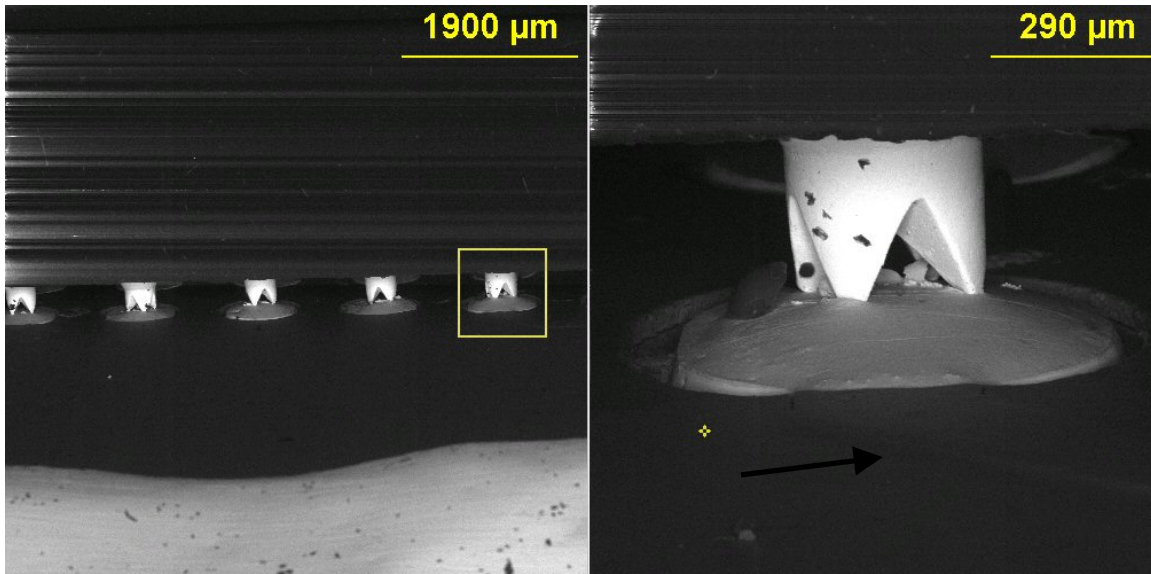


Figure 4. SEM Photo of Physical Connection between Connectorless Compression Interconnect and Target PCB

III. Electrical Advantages of Connectorless Probing

A. Electrical Considerations of Probing

The goal of the probing connection is to present the least electrically intrusive load on the target system. This is accomplished by putting the highest possible impedance at the point at which the probe contacts the system. If the impedance is infinite, then the target system will not be perturbed by this connection. However, there is a tradeoff that is made between the loading that the target experiences and the signal swing that the logic analyzer acquires. The industry has converged on a $20\text{k}\Omega$ tip impedance for high speed logic analyzer probing. This impedance is typically implemented using a discrete resistor. If there are no parasitics present, the load will look like a $20\text{k}\Omega$ resistor from DC to infinite frequency. However, the practicality of the implementation means that there is stray capacitance and inductance between the ideal tip resistor and the point at which the probe contacts the system. The largest contribution to these electrical parasitics is the physical interconnect between the resistor and the target signal. In the case of the two technologies in this paper, the Mictor connector and the compression interconnect add excess capacitance to the probing system. Figure 5 shows the ideal probing scenario.

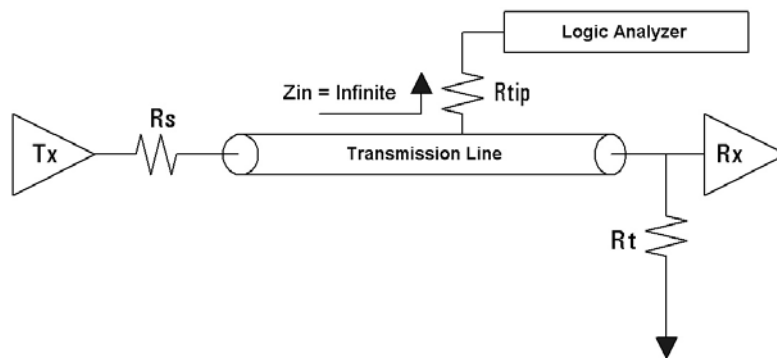


Figure 5. Theoretical Probing Connection

B. Reduced Loading on Target when Taking a Measurement

Loading is a term that refers to how much the original target signal is affected due to the probe. An ideal situation would be that when the probe is connected to a target system, the original signals are in no way altered. This is impractical in the real world, however if the loading contribution of the probe is small relative to the speeds at which the target system is running, then the probe can be ignored.

The majority of probe loading comes in the form of parasitic capacitance due to the interconnect structure. Probes contain tip circuitry that form the transport system into the

logic analyzer mainframe. This tip circuitry is implemented using discrete components, which contains self-capacitance on the order of ~ 350 fF. The remaining loading capacitance comes from the structure that connects the tip circuitry to the target signals. In the case of a Mictor-based probe, this structure consists of the mating Mictor connectors. In a connectorless probe, this structure comes from the compression interconnect used to contact the landing pads on the target PCB. The difference between these two types of probing technologies is significant. The loading of a Mictor-based probe is 3 pF while the loading of a connectorless probe is only 0.7 pF. Reducing the physical size of the probing interconnect yields greater than a 400% loading reduction when comparing connectorless to Mictor based probing technology. Figure 6 shows a profile view of the two probing technologies and illustrates the difference in the physical interconnect structure that results in excess capacitance.

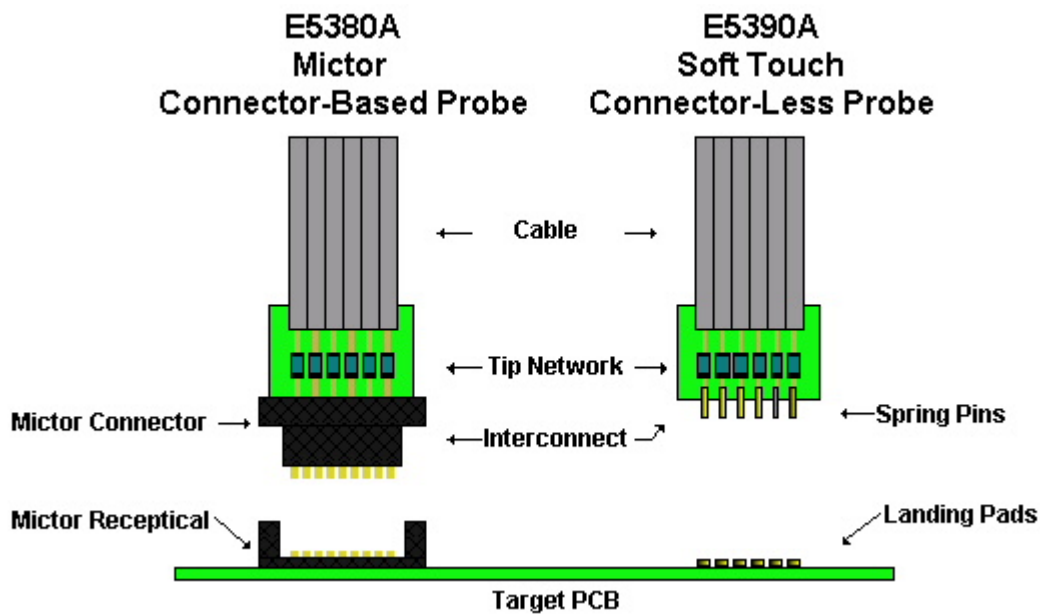


Figure 6. Side Profile View of Connectorless vs. Mictor Based Probing Interconnect

This capacitive loading has the effect of causing reflections and degrading the rise time of the signal on the target system. Since the load of the probe is an RLC system, its impedance will vary with frequency. In the case of a digital system, a faster rise time on the target will cause more of a discontinuity than a slower rise time. Logic analyzer vendors characterize the complex load impedance of each probe and provide SPICE models so that system engineers can simulate the probe's effect on their signals. The SPICE models are typically accurate up to 6GHz. Figure 7 shows the Time Domain Reflectometry (TDR) simulations comparing the loads of the two probing technologies. The Mictor's reflection is shown in Blue while the connectorless' reflection is shown in Red. Figure 8 shows the Time Domain Transmission (TDT) simulations comparing the two loads on the signal as seen at the receiver. In Figure 8, the Green waveform shows the signal without the probe connected. For both sets of simulations, various rise times are used to illustrate how the loading is more severe as the rise time gets faster.

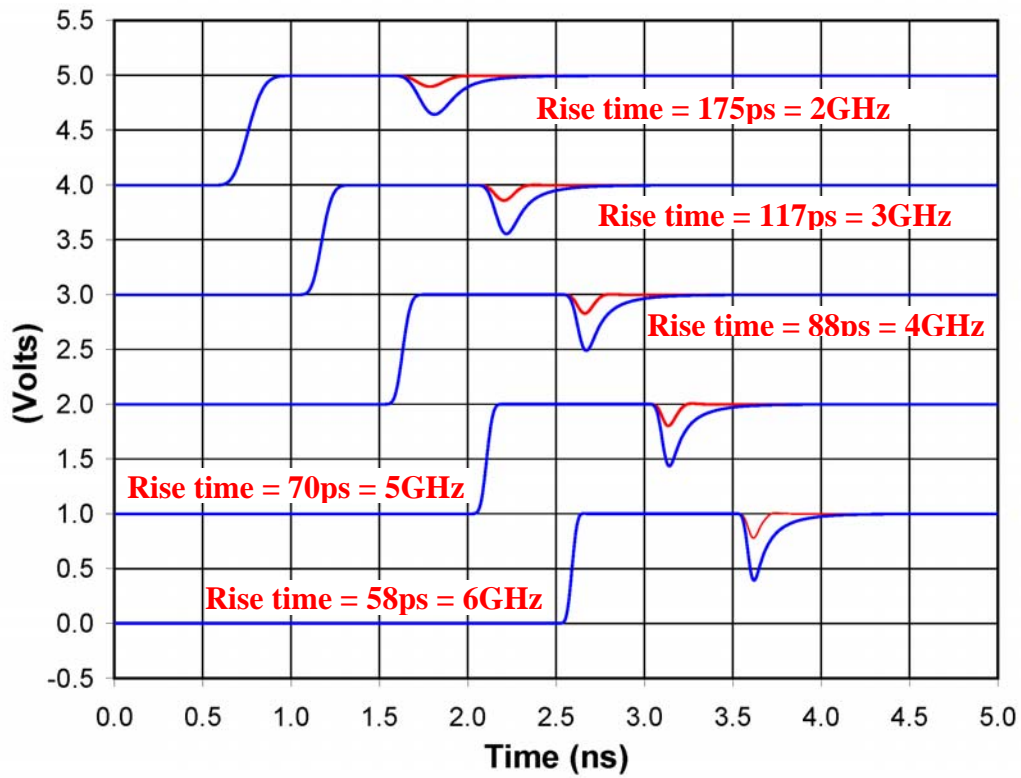


Figure 7. TDR Simulation of Mictor vs. Connectorless Probing

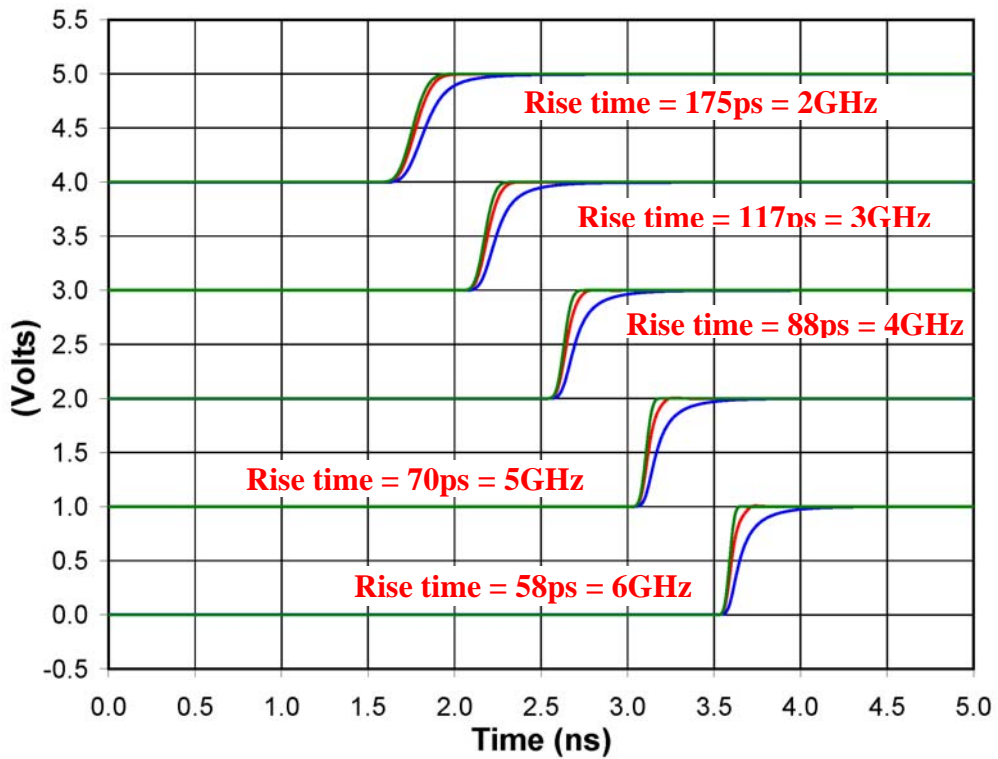


Figure 8. TDT Simulation of Mictor vs. Connectorless Probing

C. Reduced Loading when Disconnected

Another electrical advantage of connectorless probing is the reduced loading of the footprint when the probe is not connected. In Mictor-based probes, when the probe is disconnected, a mating connector still resides on the target PCB. In most cases, unused traces connected to the connector are also on the board. The parasitics of the unused probe point are large enough so that they cannot be ignored. Most designers take the connector and traces out of the design before going to production. Connectorless probes do not have this problem. Since only the landing pads are left on the board when the probe is disconnected, there is little to no loading due to the pads (~80fF). In addition, since the connectorless footprint allows minimal routing effort, there are no stubs present to add additional loading. This has the advantage that the connectorless footprint can be left in a production design without degrading the performance of the system. Designers can analyze field failures using the same test benches that they used during prototyping because the design still possesses logic analyzer probing points.

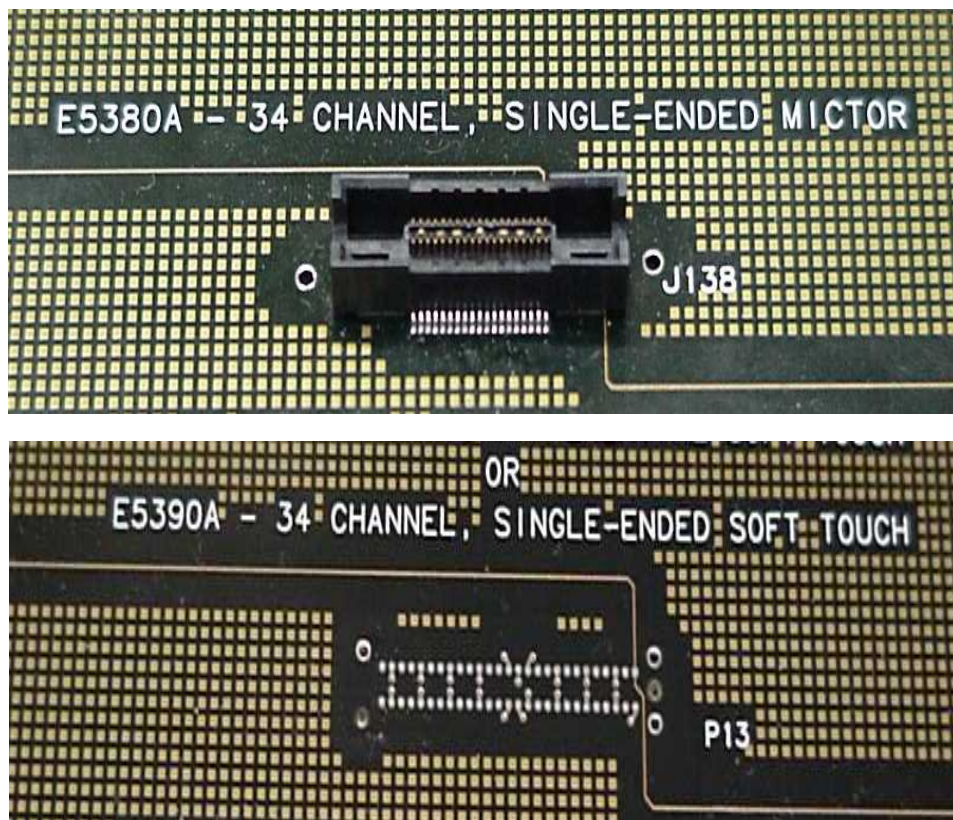


Figure 9. Physical Structure Remaining on Target PCB When Probe is Disconnected

D. Flow Through Routing

In connectorless probing, only landing pads are placed on the target PCB. These landing pads are spaced such that signals can be routed between the pads without changing signal layers. This is a new ability over traditional connector-based probes like the Mictor. In Mictor-based probes, the connector that resides on the target PCB actually prohibits any routing *through* the connector due to its use of SMT and through-hole technology. This means that when observing signals in a routing channel, the Mictor connector needs to be placed to the side of the traces and *stub-traces* are used to make the connection to the connector. Placing the connector off to the side has the disadvantage of increased loading due to the need for *stub-traces*. In addition, more PCB area is required to accommodate the connector placement. With connectorless probing, the footprint can be placed directly in the signal path with minimal disturbance to the routing of the signals.

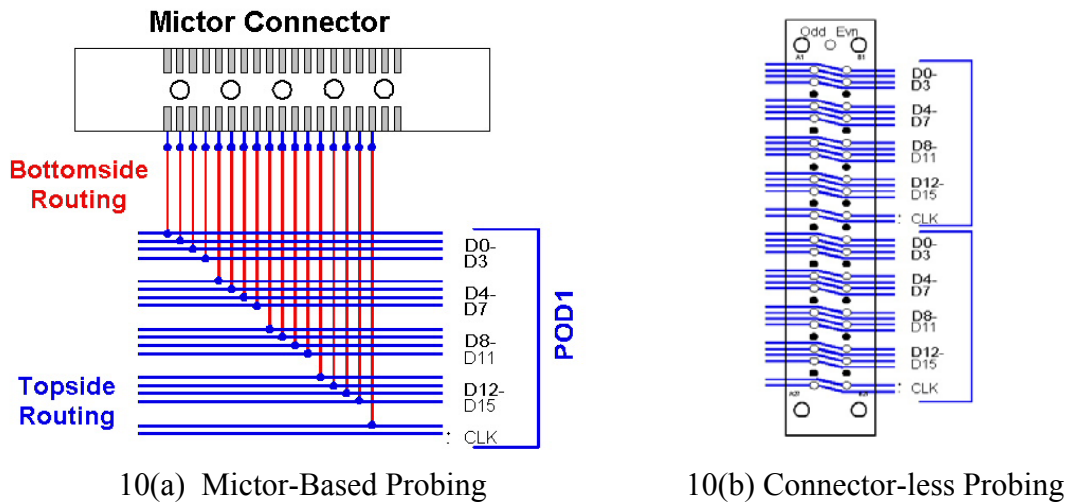


Figure 10. Routing Implications Between Mictor and Connectorless Probing

As edge rates increase, it becomes more and more important to reduce impedance mismatches along the transmission line. Any energy that is reflected as the wave front travels down the transmission line leads to degradation of the initial edge. When using differential signaling, one potential source of discontinuity is the uncoupling of the signal pair. As a differential signal propagates, it exchanges charge with its reference plane in addition to its complement signal within the pair. There is deterministic impedance for both charge-exchanging paths. These are referred to as Even and Odd mode impedances. If the signal pair experiences trace separation during the route, these impedances change. When the impedances change, there will be a reflection at the point at which the impedances are different from the original transmission line. The following example illustrates this point.

Example)

A standard 5" differential pair is routed using 0.005" traces widths with 0.010" trace separation. The signals are routed as microstrip transmission lines over 0.003" of dielectric with a dielectric constant of 4.0. This transmission line design yields $Z_{O\text{even}}=53.1\Omega$, $Z_{O\text{odd}}=48\Omega$, and $Z_o=50.6\Omega$'s. The differential pair is terminated into a 100 Ω resistor.

Suppose the differential pair above undergoes a trace separation that increases the separation to 0.030" (instead of 0.010") for a length of 1" in the middle of the route. The resulting 1" of trace has a $Z_{O\text{even}}=51.4\Omega$, $Z_{O\text{odd}}=51\Omega$, and $Z_o=51\Omega$'s. This impedance mismatch causes a reflection as the traces are separated. The following simulation shows the result of this case. The 1" trace separation causes a reflection that re-reflects off of the low impedance driver and appears at the receiver sometime after the initial edge. The risetime of the driver is 58ps (6GHz). In this case, the differential receiver will lose 5% of its voltage noise margin due to uncoupling of the differential pair.

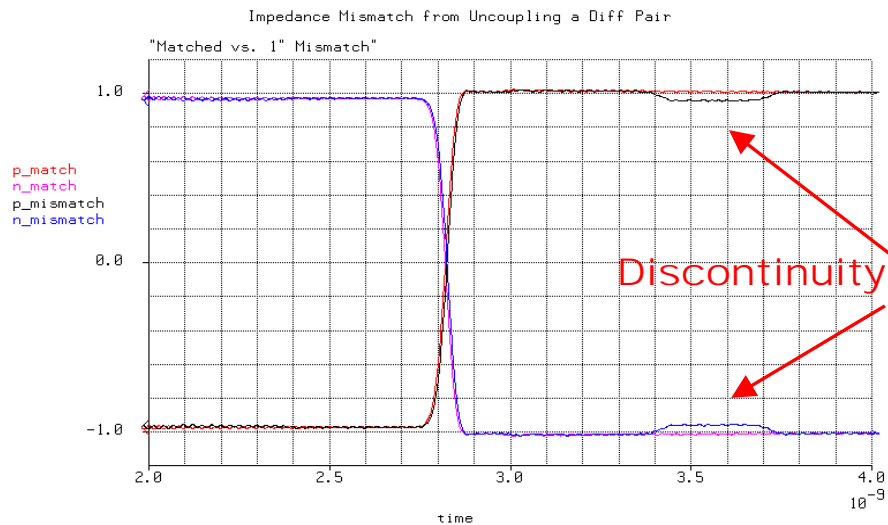


Figure 11. Discontinuity Caused by Separation of Differential Traces

The above example illustrates the importance of preserving the differential impedance of a signal pair as it is routed. Only the connectorless probing footprint allows differential pairs to be routed *through* the footprint without spacing separation.

IV. Conclusion

As digital data rates continue to increase, the standard technique for performing logic analyzer probing is becoming obsolete. Traditional Mictor-based probing is being replaced with connectorless probing technology. Connectorless probing possesses a suite of mechanical and electrical advantages over Mictor-based probes. Designers that are migrating to the new connectorless probing technology are reaping the benefits of a more reliable connection with minimal loading and simple to implement features on the target PCB. This new technology is allowing designers to achieve successful logic analysis as they push their systems to higher data rates.

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