DesignConEast 2005
Track 4: Power and Packaging (4-WA1)

Design of a Low-Power Differential Repeater Using Low-Voltage Swing and Charge Recycling

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Problem Statement

- Power is the largest problem facing IC/SoC designers

- On-chip trace delay limits performance in DSM
  1) Repeaters are used to reduce delay
  2) Repeaters add power
Agenda

1) Problem Motivation

2) Proposed Solution

3) Simulation Results
Problem Motivation

RC Trace Delay

$$t_{RC} = (0.69) \cdot RC$$
Problem Motivation

RC Trace Delay

\[ R = \frac{\rho L}{A} \propto L \]

\[ C = \frac{\varepsilon \cdot W \cdot L}{t_{ox}} \propto L \]

\[ t_{RC} \propto L^2 \]

Quadratic Increase
Problem Motivation

Interconnect Dominates DSM Performance

1948: Elmore Delay Presented
1959: First Integrated Circuit
1990: Gate Delay = Interconnect Delay (1um)
2000: Deep Sub Micron (<0.5um) Interconnect Delay Dominates Performance
2010: Nanometer Technology (<0.05um) Interconnect Delay Negates Moore's Law

Source: 2003 ITRS
Problem Motivation

**Standard Solution:** “Repeater Insertion”

- Break line into smaller segments: \( (L \rightarrow 0) \)
- Optimal sizing when: \( t_{buf} = t_{RC} \)
- Linear dependence: \( t_{delay} \propto L \)
Problem Motivation

**Repeaters Add Power**

\[
P_{\text{dynamic}} = C \cdot V_{\text{swing}}^2 \cdot f
\]

\[
P_{\text{short-circuit}} = I_{\text{sat}} \cdot V_{\text{DD}} \cdot f
\]

Power $\propto$ (# of Repeaters)
Problem Motivation

Repeater Power Scaling Isn’t Realistic

2003 ITRS Prediction:

- at 50nm, global interconnect will consume 40% of power in VLSI
- 0.25um $uP$ : 50,000 repeaters : 8 Watts
- 70nm $uP$ : 700,000 repeaters : 60 Watts
Problem Motivation

**Need to Reduce Power**

- Need techniques to reduce power of repeater scheme
- A small decrease in delay is acceptable
- Net improvement in PDP is the goal
Proposed Solution

Current Trends

- Differential signaling on clock traces for Noise Immunity
  - Well Suited for Low-Voltage Output Swing
  - Well Suited for Charge Sharing
Proposed Solution

**Differential Signaling**

- Complimentary Outputs for VLSI CMOS
- Receiver Performs \((\text{CLK}-\overline{\text{CLK}})\) which rejects coupled noise
- Receiver Performs \((\text{CLK}-\overline{\text{CLK}})\) which doubles effective amplitude
Proposed Solution

Low-Voltage Swing Outputs

- Reducing Output Swing Reduces Power

\[ P_{\text{dynamic}} = C \cdot V_{\text{swing}}^2 \cdot f \]

- Differential Signaling has extra margin to accommodate this

\[ \overline{\text{Clk}} \quad \text{Clk} \quad \implies \quad (\text{Clk}-\overline{\text{Clk}}) \]
Proposed Solution

**Low-Voltage Swing Outputs**

- Typical CMOS swings from $V_{SS}$ to $V_{DD}$
- Insert $V_t$ drops between supplies to reduce output swing
Proposed Solution

Low-Voltage Swing Outputs

- The reduced output swing is:

\[ V_{LV-swing} = V_{DD} - V_{t,n} - |V_{t,p}| \]

- The reduced power is:

\[ P_{dynamic} = C \cdot V_{LV-swing}^2 \cdot f \]
Proposed Solution

Charge Recycling

- Typical CMOS charges output from supply

\[ Q_{0\rightarrow 1} = C_{load} \cdot V_{swing} \]

\[ Q_{1\rightarrow 0} = C_{load} \cdot V_{swing} \]
Proposed Solution

**Charge Recycling**

- The Symmetry of Differential Signaling can be exploited

One Driver is always **charging** while the other is **discharging**
Proposed Solution

Charge Recycling

- During first half of the transition equal charge is distributed

\[
\text{Charging from } V_0 \text{ to } V_{\text{swing}}/2
\]

\[
\text{Discharging from } V_1 \text{ to } V_{\text{swing}}/2
\]

\[
Q_{\text{charge}} = -Q_{\text{discharge}}
\]
Proposed Solution

Charge Recycling

- Charge can be “Shared” between Clk & \( \overline{\text{Clk}} \) from \( t_0 \) to \( t_{V_{\text{swing/2}}} \)

\[
Q_{\text{charge}} = -Q_{\text{discharge}}
\]
Proposed Solution

**Charge Recycling**

- From $t_{V\text{swing}/2}$ to $t_{SS}$ charge is provided by Supplies as usual
Proposed Solution

Charge Recycling

- \( \text{Clk} \) & \( \text{Clk} \) are connected from \( t_0 \) to \( t_{Vswing/2} \)

\[
\begin{align*}
0 \rightarrow 1 \\
\text{Clk} \\
1 \rightarrow 0 \\
\bar{\text{Clk}} \\
\end{align*}
\]
Proposed Solution

**Charge Recycling**

- Clk & Clk are disconnected from $t_{Vswing/2}$ to $t_{SS}$

![Diagram showing the proposed solution with Clk and Clk being disconnected from $t_{Vswing/2}$ to $t_{SS}$]
Proposed Solution

Charge Recycling

- Circuit Description

```
<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>O</th>
</tr>
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<tbody>
<tr>
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<td>1</td>
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</tbody>
</table>
```
Simulation Results

Trace Modeling

- BSIM 0.1um Process (BPTM)
- 1cm Length
- Metal 3

\[ R_{\text{trace}} = 1333\Omega \]
\[ C_{\text{trace}} = 1.29\text{pF} \]
Simulation Results

Repeater Design

Using Optimal Sizing:

- Full-Swing Repeater: 15
- Low-Voltage Repeater: 9
- Low-Voltage Charge Recycling Repeater: 9
Simulation Results

Circuit Operation

- Circuit Operation

![Graph showing circuit operation](image)
Simulation Results

Current Profile vs. Time

Full-Swing

Low-Voltage

LV Charge-Recycling

Agilent Technologies
Simulation Results

**Performance**

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Figures of Merit</th>
<th>Improvement</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>Delay (ps)</td>
<td>Power (mV)</td>
</tr>
<tr>
<td>Full-Swing Repeater</td>
<td>639</td>
<td>12.06</td>
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<tr>
<td>Low-Voltage Repeater</td>
<td>699</td>
<td>7.54</td>
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<tr>
<td>Low-Voltage Charge Recycling Repeater</td>
<td>774</td>
<td>6.92</td>
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</table>

- **Lowest Delay** = Full-Swing Repeater
- **Lowest PDP** = Low-Voltage Repeater
  
  (32% improvement)

- **Lowest Power** = Low-Voltage Charge Recycling Repeater
  
  (43% improvement)

Both Improve PDP
Implementation Details

**Suggested Use**

- On-Chip Metal 3 or Greater

**Not Suggested**

- On-Chip Metal 1 or 2  
  (too much resistance, acts distributed)

- Off-Chip  
  (too much inductance, acts distributed)
## Implementation Details

### Sizing

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Section</th>
<th>Transistor</th>
<th>Size</th>
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</thead>
<tbody>
<tr>
<td>Full-Swing Repeater</td>
<td>INV</td>
<td>NMOS</td>
<td>2.5/0.1</td>
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<tr>
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<td></td>
<td>PMOS</td>
<td>8.0/0.1</td>
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<tr>
<td>Low-Voltage Repeater</td>
<td>INV</td>
<td>NMOS</td>
<td>5.0/0.1</td>
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<tr>
<td></td>
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<td>PMOS</td>
<td>16.0/0.1</td>
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<tr>
<td></td>
<td>V&lt;sub&gt;t&lt;/sub&gt; Drop</td>
<td>NMOS</td>
<td>25/0.1</td>
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<td></td>
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<td>80/0.1</td>
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<tr>
<td>Low-Voltage Charge Recycling Repeater</td>
<td>INV</td>
<td>NMOS</td>
<td>5.0/0.1</td>
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<tr>
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<td></td>
<td>PMOS</td>
<td>16.0/0.1</td>
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<td>0.8/0.1</td>
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<tr>
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<td>CS</td>
<td>NMOS</td>
<td>0.2/0.1</td>
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</table>

- Low Resistance
- Negligible Capacitance

< (20%) $\tau_{load}$
Summary

Trends

• Power and Delay are major problems in DSM
• Repeaters are expected to dominate power
• Differential signaling is being used for noise immunity on clocks

Proposed Technique

• Low-Voltage Swing enabled by differential signaling
• Charge Recycling enabled by differential signaling
• Suffer small delay penalty for decreased power (PDP ↑)
Questions?