Design of a Radiation Tolerant Computing System Based on a Many-Core Architecture

Erwin Dunbar, Pat Kujawa, & David Racek
Advisor: Dr. Brock J. LaMeres

In this project, we designed a redundant processor computing system on reprogrammable hardware for use in aerospace systems. The system is designed with 64 redundant PicoBlaze soft processors in order to detect and recover from faults that may occur due to radiation strikes. Three processors at a time run in Triple Modular Redundancy (TMR) voting to check whether a fault has occurred in one of the processors. A software interface was designed to allow a user to disable one of the active processors to simulate a processor failing due to a hard fault. The system should continue to run while seamlessly disabling the faulted processor and bringing a new processor online to take its place.

The advising entity for this design project was the NASA Radiation Hardened Electronics for Space Exploration (RHESE) program. This group specified the following design objectives:

Task #1: Design a graphical user interface (GUI) that shows an 8x8 array of processors. A user will be able to disable one of the processors using the GUI. This application mimics a processor being physically damaged by a radiation strike.

Task #2: Design digital hardware to communicate with a PC in order to receive the information from the application described in task 1.

Task #3: Design a computer system containing 64 redundant microprocessors to control a basic set of peripherals. The system will disable damaged processors and enable inactive processors, depending on the information received from the GUI.

In this project, we designed a redundant processor computing system based on a many-core architecture. The system is designed with 64 redundant PicoBlaze soft processors in order to detect and recover from faults that may occur due to radiation strikes. Three processors at a time run in Triple Modular Redundancy (TMR) voting to check whether a fault has occurred in one of the processors. A software interface was designed to allow a user to disable one of the active processors to simulate a processor failing due to a hard fault. The system should continue to run while seamlessly disabling the faulted processor and bringing a new processor online to take its place.

When high-energy cosmic particles strike integrated circuits, a variety of fault conditions occur. Such fault conditions are called Single Event Effects. Single Event Upsets (SEU), or soft faults, occur when the particles create soft errors such as bit flips. Soft faults can be remedied with a software reset. Single Event Damage, or a hard fault, causes physical damage to the circuit and cannot be remedied by a reset. Instead, other mitigation techniques, such as swapping in spare circuitry, must be investigated. Both of these failure conditions are of great concern to NASA as they develop the technology for interplanetary missions in the coming decades.

The electrical and computer engineering department at Montana State University, Bozeman, MT, sponsored this project.

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The user interface shows the status of each of the 64 processors:
- Blue: Active
- Gray: Inactive
- Red: Damaged

The CPU Destruction Log, System Communications Log, and Processor Control Logic block take in commands from the Graphical User Interface and tell the Router and Switchboard which processors have been damaged.

The design objectives were to:
- Develop a redundant processor computing system based on a many-core architecture.
- Design a graphical user interface that shows an 8x8 array of processors.
- Design digital hardware to communicate with a PC.
- Design a computer system containing 64 redundant microprocessors to control peripherals.

The system operation includes:
- User Interface: Shows the status of each processor.
- System Operation: Processor status window, Clicking on a processor damages it.
- System Overview: 64 redundant soft processors are implemented on a Xilinx Virtex-5 FPGA. Three processors are active at any given time.
- Results: The computer system is able to control 64 processors and seamlessly switch between them when a hard fault occurs.
- Acknowledgements: We would like to thank the Montana Space Grant Consortium and the NASA Exploration Systems Mission Directorate (ESMD) Higher Education Program for sponsoring this project.