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Session E: PLD Based System Architectures
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Design of a Radiation Tolerant Computing System Based on a Many-Core FPGA Architecture

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Dr. Robert E. Ray
Marshall Space Flight Center
Reconfigurable Computing Task

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RHESE Project Manager

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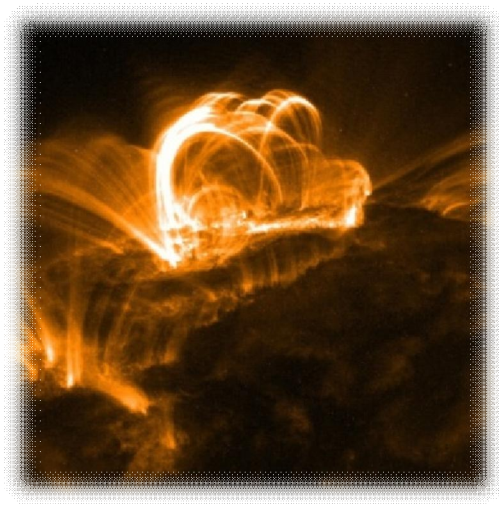
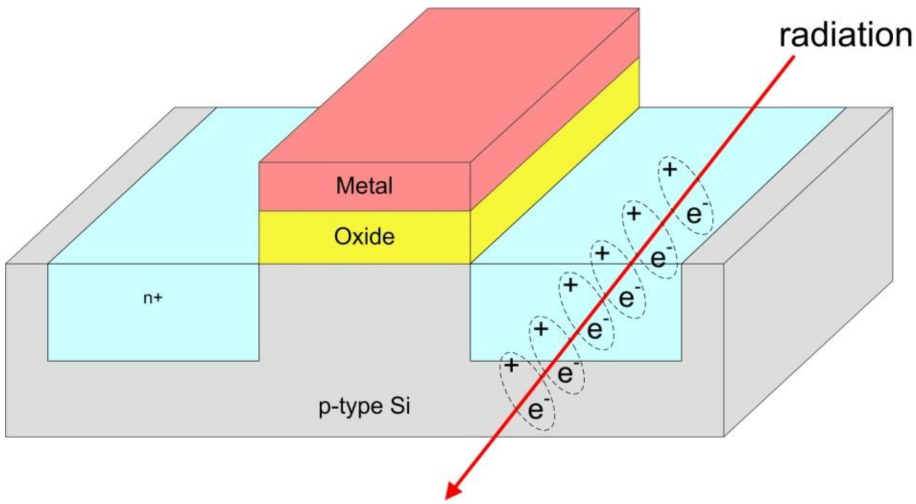
Goddard Space Flight Center
High Performance Processor Task

Motivation

- Radiation has a detrimental effect on electronics in space environments.
- The root cause is from electron/hole pairs creation as the radiation strikes the semiconductor portion of the device and ionizes the material.





Types

- *alpha particles* (Terrestrial, from packaging/doping)
- *Neutrons* (Terrestrial, secondary effect from Galactic Cosmic Rays entering atmosphere)
- *Heavy ions* (Aerospace, direct ionization)
- *Proton* (Aerospace, secondary effect)

Motivation

- Two types of failures mechanics are induced by radiation

  1) Total Ionizing Dose (TID)

  - The cumulative, long term ionizing damage to the device materials
  - Caused by low energy protons & electrons

  2) Single Event Effects (SEE)

  - Transient spikes caused by Heavy Ions and protons
  - Can be both destructive & non-destructive

Motivation (TID)

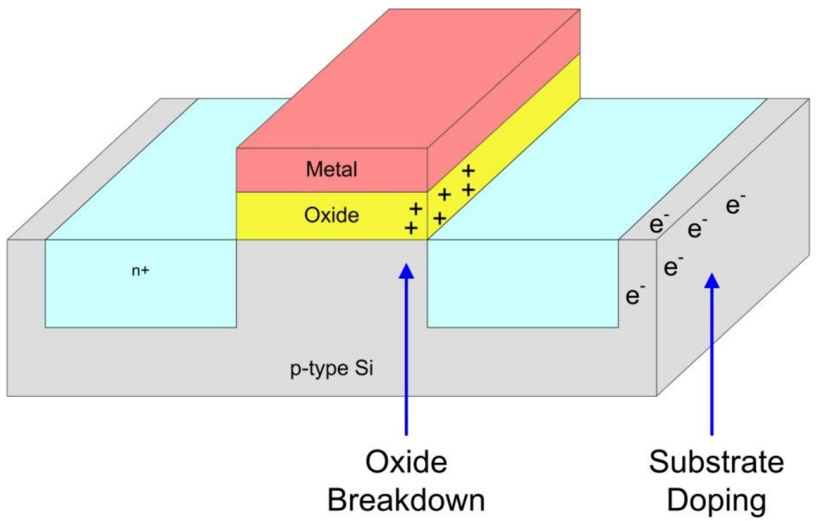
1) Total Ionizing Dose (TID)

– As the electron/holes try to recombine, they experience different mobility rates ($\mu_n > \mu_p$)

– Over time, the ionized particles can get trapped in the oxide or substrate of the device prior to recombination

– This can lead to:

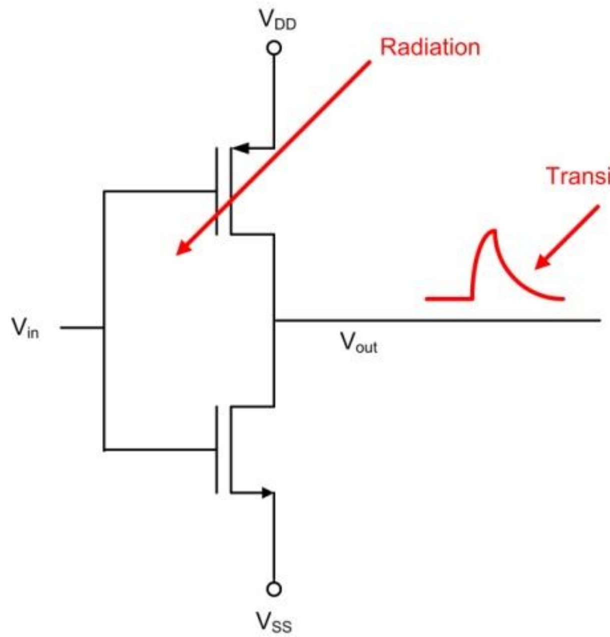
- Threshold Shifting
- Leakage Current
- Timing Skew



Motivation (SEEs)

2) Single Event Effects (SEEs)

- Transient voltage/current induced in devices
- This can lead to both Non-Destructive and Destructive effects



Non-Destructive	Behavior
Single Event Transient (SET)	*A transient spike of voltage/current noise, can cause gate switching*
Single Event Upset (SEU)	*A transient captured in a storage device (FF/RAM) as a state change*
Multi-Bit Upsets (MBU)	*Multiple, simultaneous SEUs*

Destructive	Behavior
Single Event Latchup(SEL)	*Transient biases the parasitic bipolar SCR in CMOS causing latchup*
Single Event Burnout (SEB)	*Transient causes the device to draw high current which damages part*
Single Event Gate Rupture (SEGR)	*The energy is enough to damage the gate oxide*

Mitigation of TIDs

1) Current Mitigation Techniques (TID)

- Parts can be "hardened" to TID through:

  - layout techniques (sizing of Q_{crit}, enclosed layout)
  - substrate doping
  - redundant circuitry

- Parts are specified in terms of:

  - "the amount of energy that can be tolerated by ionizing particles before the part performance is out of spec"

  - units are given in krad (Si), typically 300krad+

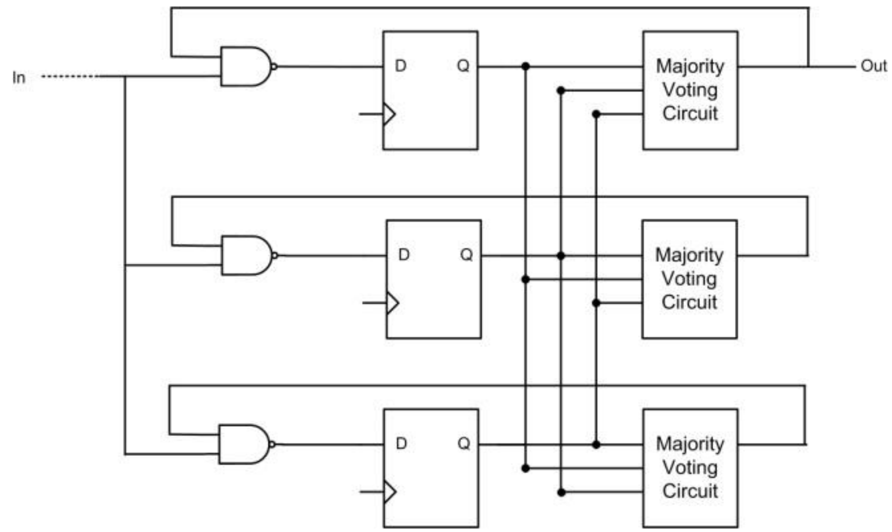
- Shielding <u>Does </u>Help

  - low energy protons/electrons can be stopped at the expense of weight

Mitigation of SEEs

2) Current Mitigation Techniques (SEEs)

- Triple Modular Redundancy (TMR)



- Reboot/Recovery Sequences

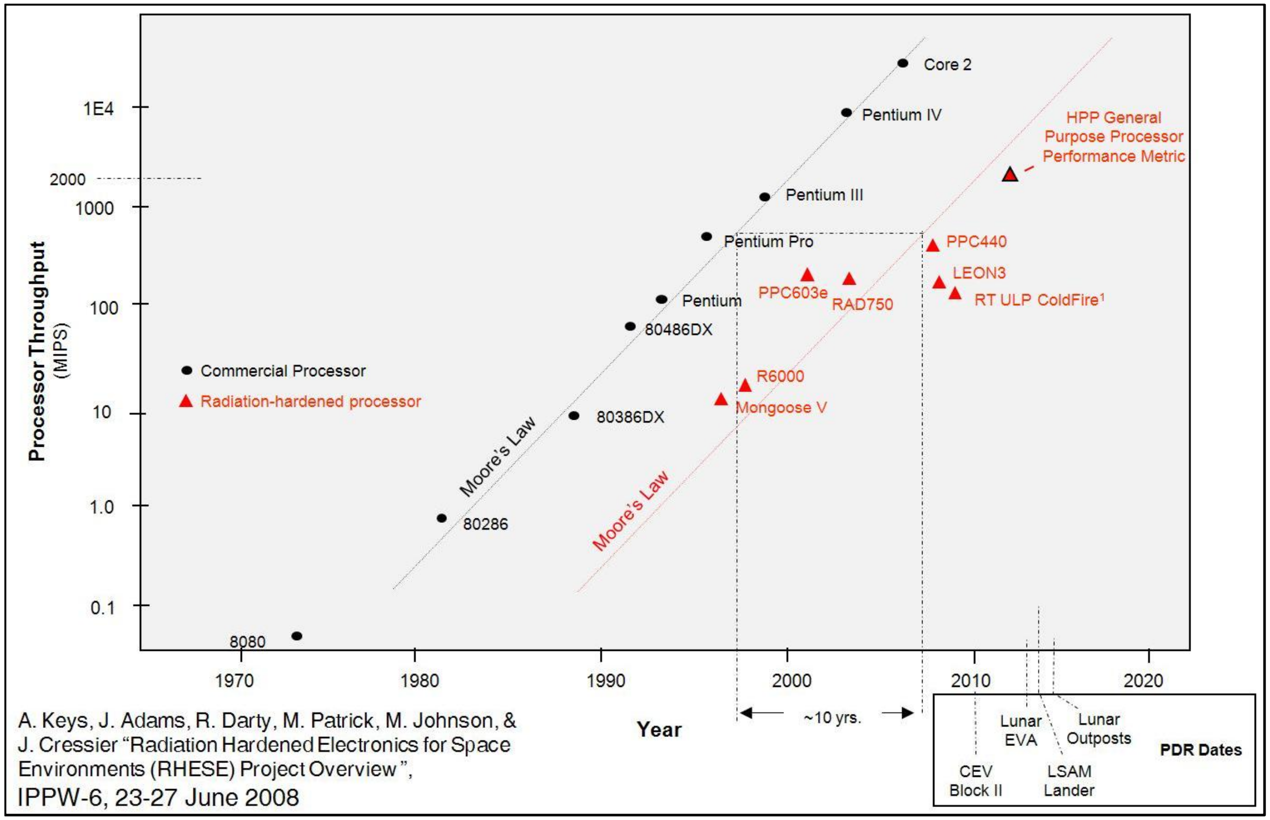
- Shielding Does NOT eliminate all SEEs

  - impractical to shield against high energy particles and Heavy Ions due to necessary mass

Drawback of Mitigation

- **Radiation Hardening = Slower Performance**

  - All TID mitigation techniques lead to slower performance



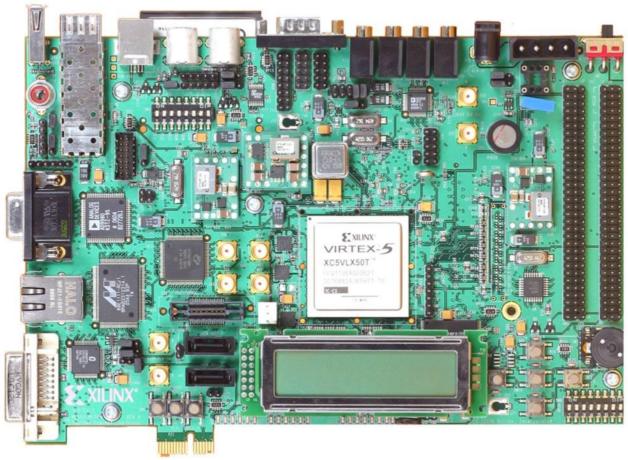
  - TID mitigation **DOES NOT** prevent SEEs

FPGAs & Radiation

- **Radiation Mitigation in FPGAs**

  - RAM based FPGAs are traditionally *soft* to radiation

  - Fuse-based FPGAs provide some hardness, but give up the flexibility of real-time programmability



- **Exploiting Reconfiguration**

  - The flexibility of FPGAs enables novel techniques to radiation tolerant computing

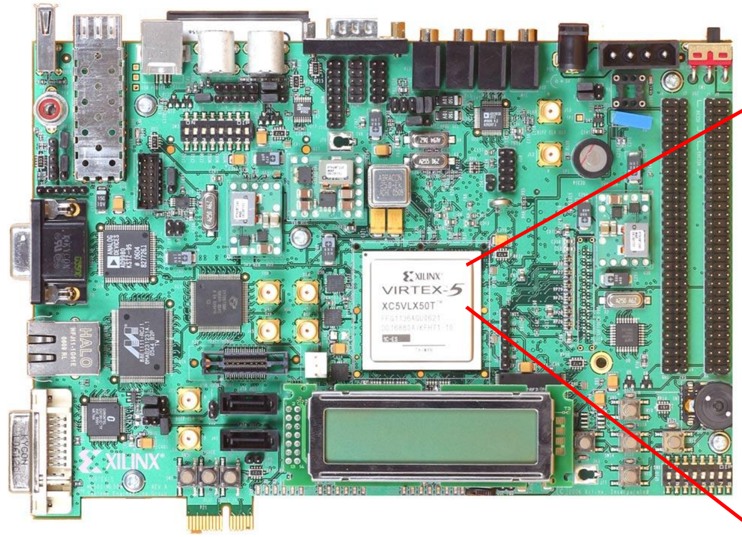
    ex) Dynamic TMR, Spatial Avoidance of TID failures,

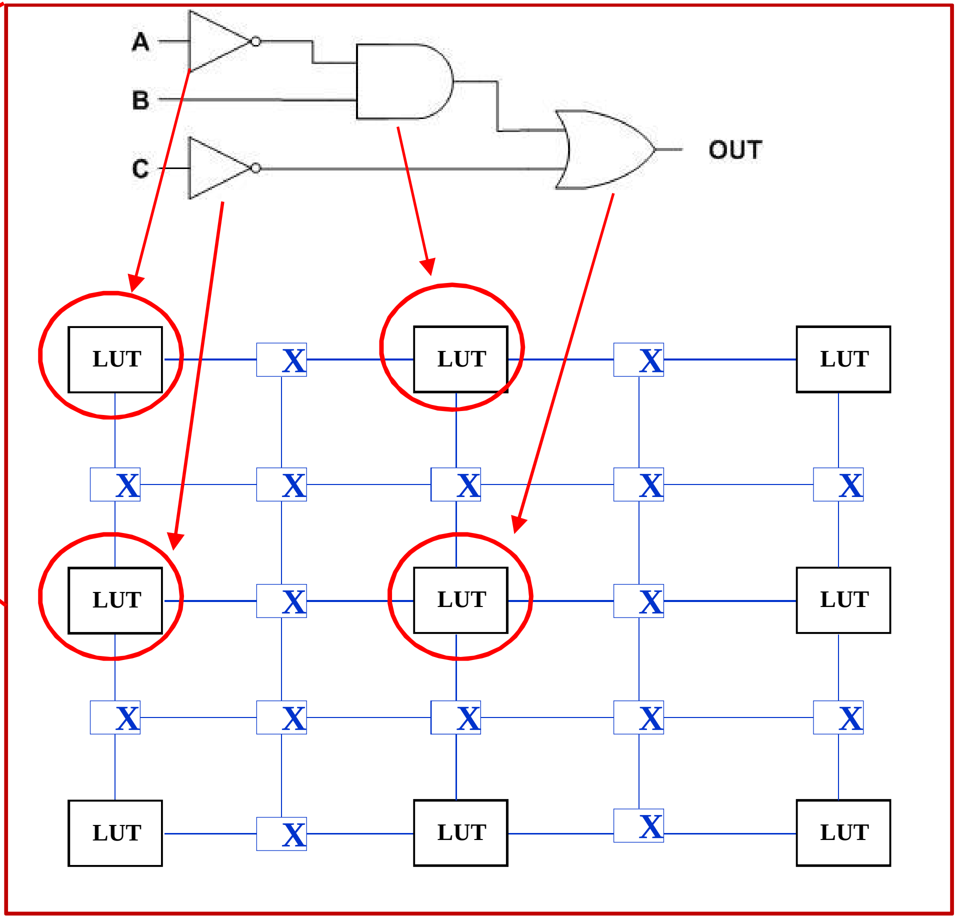
  - The flexibility of FPGAs is attractive to weight constrained Aerospace applications

    ex) Reduction of flight spares, internal spare circuitry

FPGAs as a Solution?

- **Field Programmable Gate Arrays**





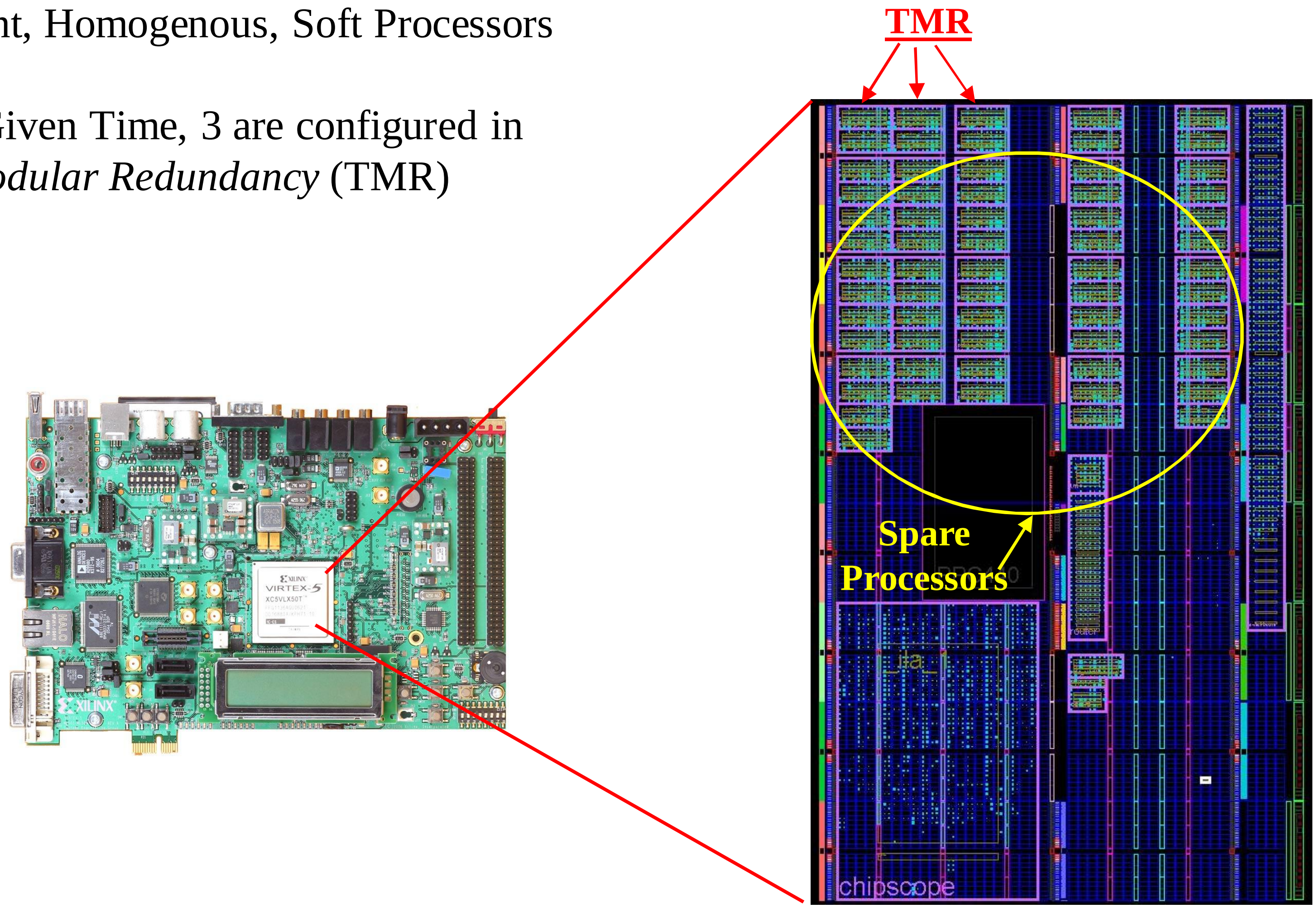
- FPGAs have followed Moore's Law and now yield comparable processing power to ASICs

Many-Core Architecture

- **Radiation Tolerance Through Architecture**

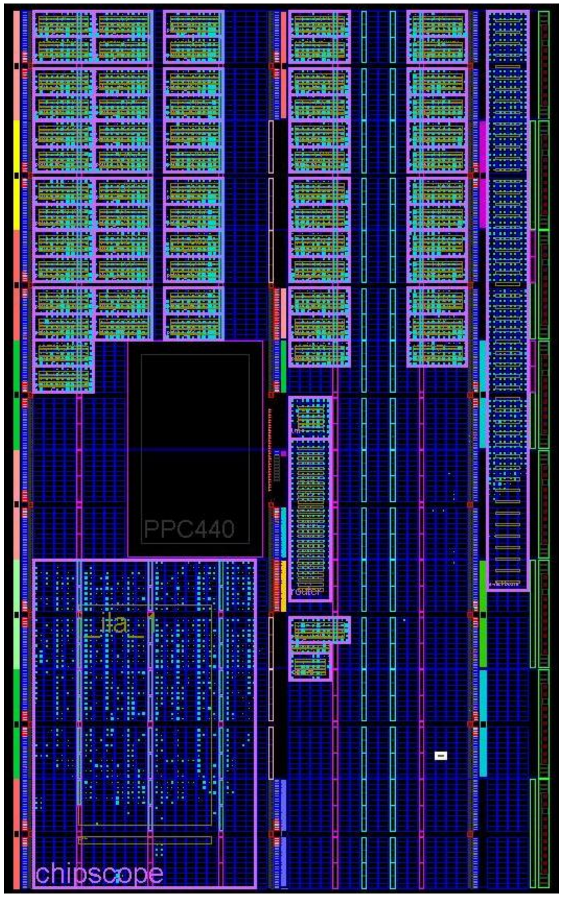
  - Redundant, Homogenous, Soft Processors

  - At Any Given Time, 3 are configured in *Triple Modular Redundancy* (TMR)



Many-Core Architecture

- **Types of Radiation Faults Seen in FPGAs**



1) Soft Faults

- *SEUs that can be recovered from using a reset*

2) Medium Severity Faults

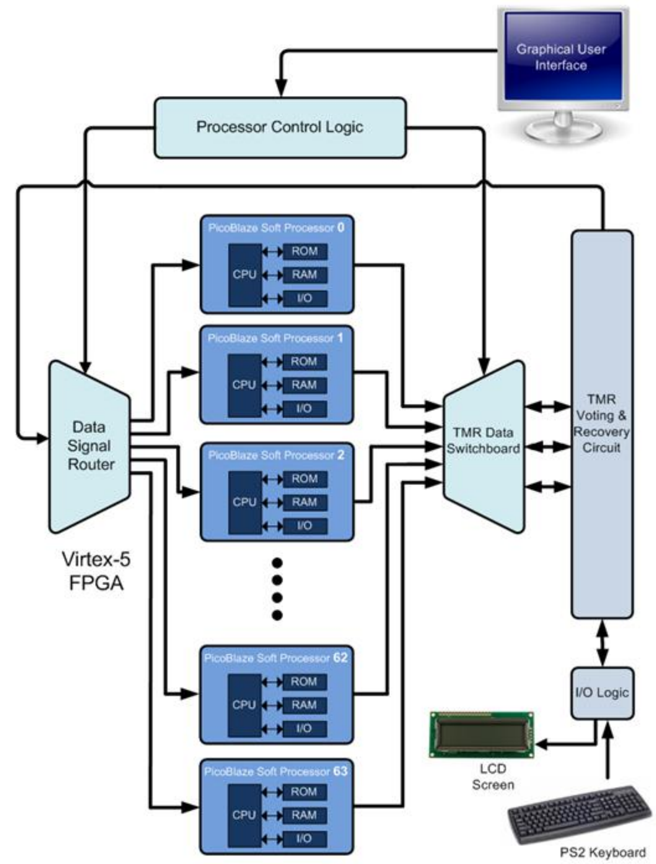
- *SEUs in reconfiguration memory, can only be recovered using reconfiguration*

3) Hard Faults

- *Damage to part of the chip due to TID or Displacement Damage*

Many-Core Architecture

- **Fault Recovery Procedures**



<u>**Fault Type**</u>	<u>**Recovery Action**</u>
Soft Faults	- TMR Voter detects fault - 2 good processors complete current task - Good 2 processors offload variable data - All 3 processors are reset - All 3 processors re-initialized with variable data - All 3 processors resume operation in TMR
Medium Faults	- Same general procedure, *except* Bad processors is **partially reconfigured** to reset configuration RAM
Hard Faults	- A spare processor is brought online to complete TMR - Bad processor is flagged as "DO NOT USE"

Many-Core Architecture

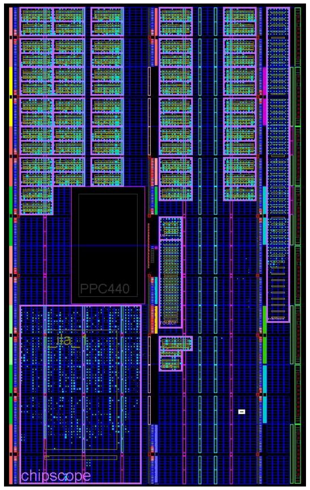
- **Advantages of this Approach**

1) SEUs mitigated using traditional TMR

2) Partial Reconfiguration technique increases *hardness* of RAM-based FPGAs

3) Spatial avoidance of damaged regions of FPGA extend system lifetime

4) Logical approach can be applied to RHBD FPGA fabrics (*SIRF*, etc…) for increased radiation immunity

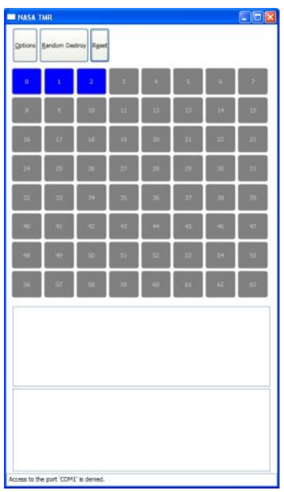


System Prototyping

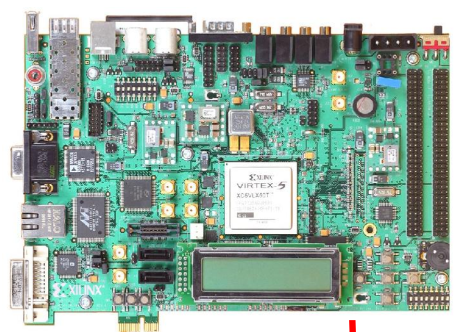
- **Many-Core Computing Architecture**

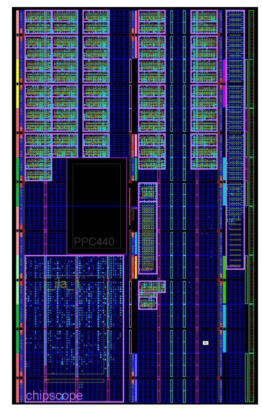
  - 64 picoBlaze Processors (3+61) implement on a Virtex-5 FX50
  - The computer system controls basic peripherals
  - A push button is used to mimic soft SEUs
  - A PC GUI is created to inject hard failures
  - HyperTerminal is used to mimic medium severity faults requiring partial reconfiguration
  - Xilinx ChipScope used to monitor processor operation on all 64 processors

PC Gui to induce Hard Failures

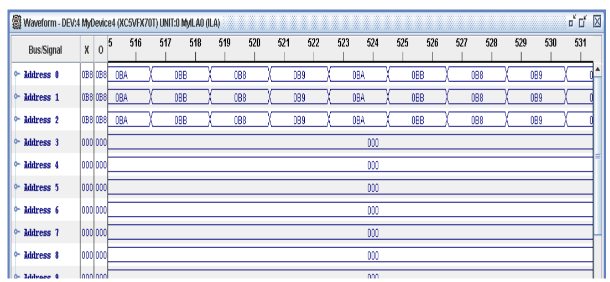


ML507 V5 Platform w 64 pBlaze uPs





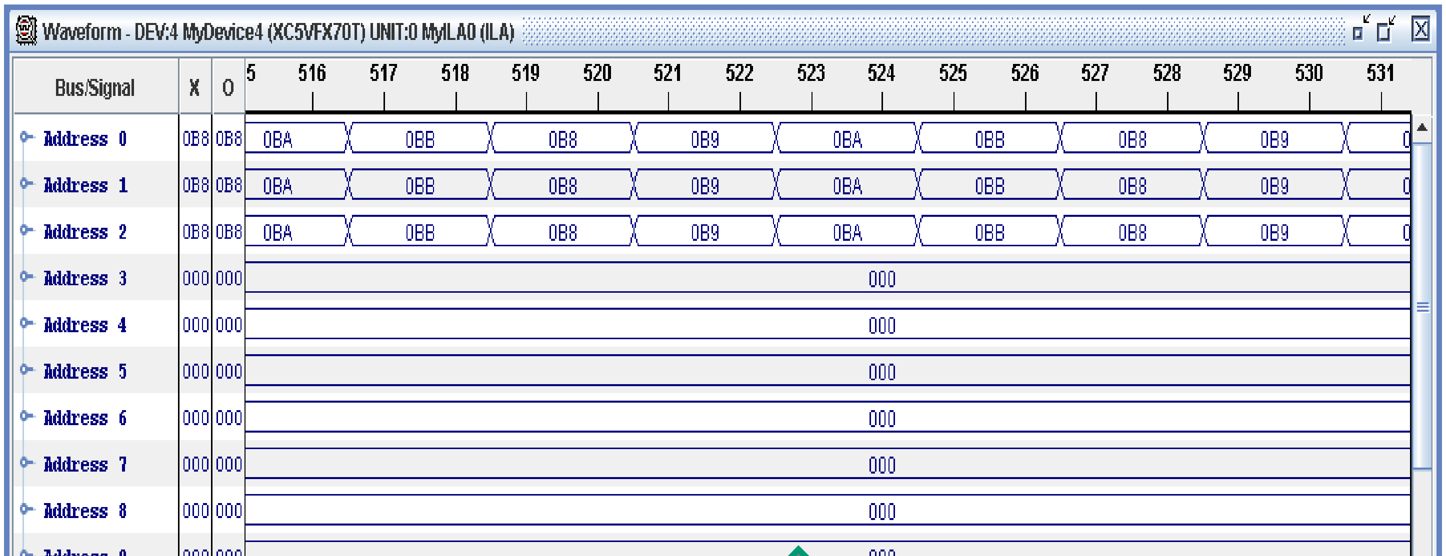
ChipScope Internal Logic Analyzer

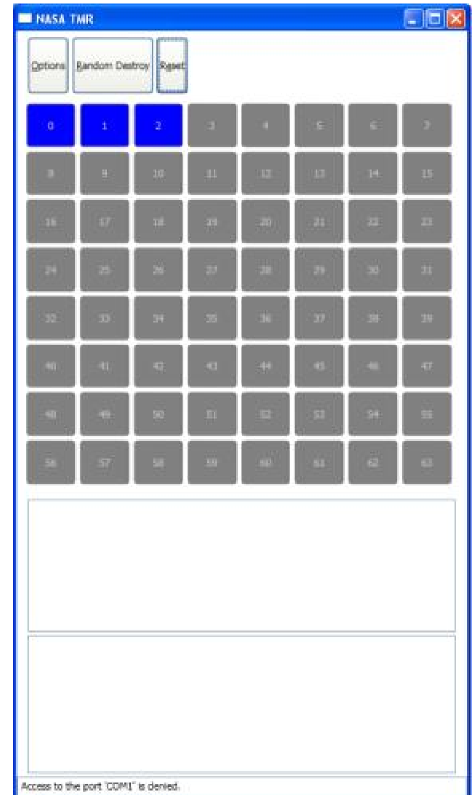


System Demonstration

- **Initial Operation**

  - Processors **0, 1, and 2** are active (blue) and operating in TMR
  - Processors **3-63** provide 61 spare *picoBlaze* processors (gray)





ChipScope shows uP 1,2,3 are running in synch with no faults

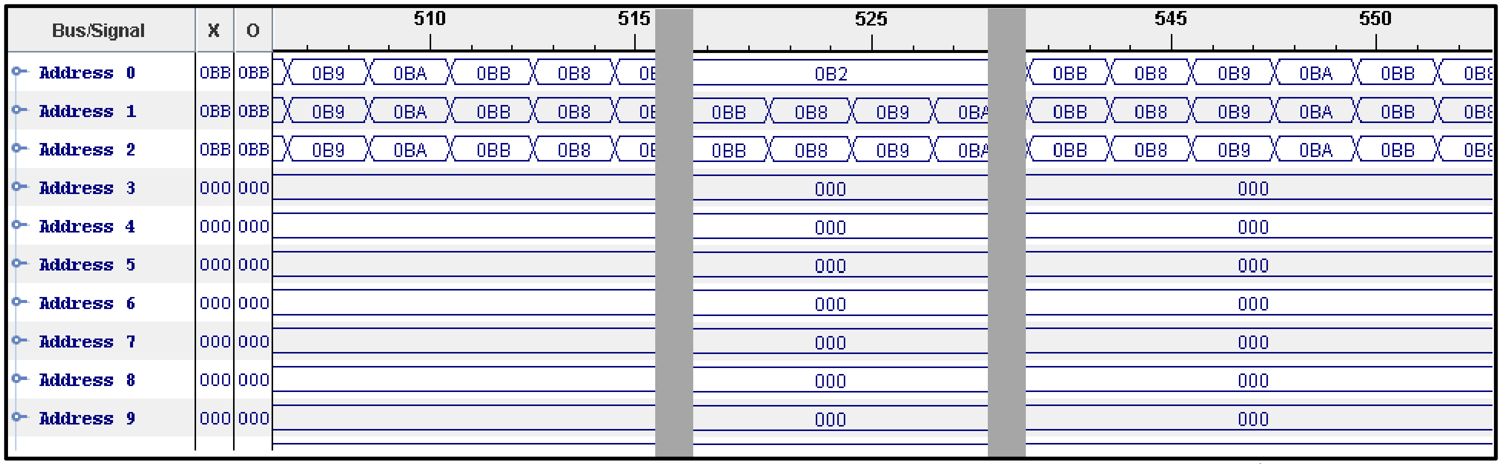
GUI indicates uP 0, 1, and 2 are active (blue)

(showing address lines between uP and memory for all 64 processors)

System Demonstration

- **Soft Fault Recovery**

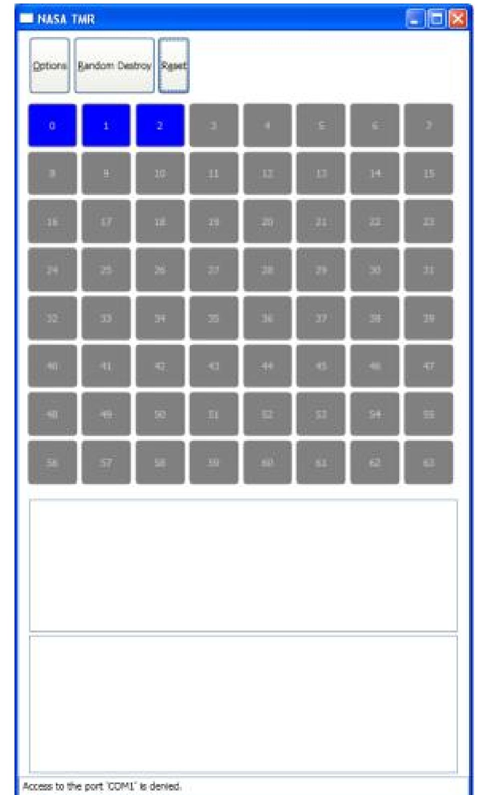
  - Processors **0, 1, and 2** are active (blue) operating in TMR
  - Processors **0** undergoes a soft fault and then recovers and resynchronizes



System initialized and running normally in TMR mode.

Processor 0 has been corrupted by an SEU. The TMR detects the failure.

Processor 0 brought back into synch with other two processors.

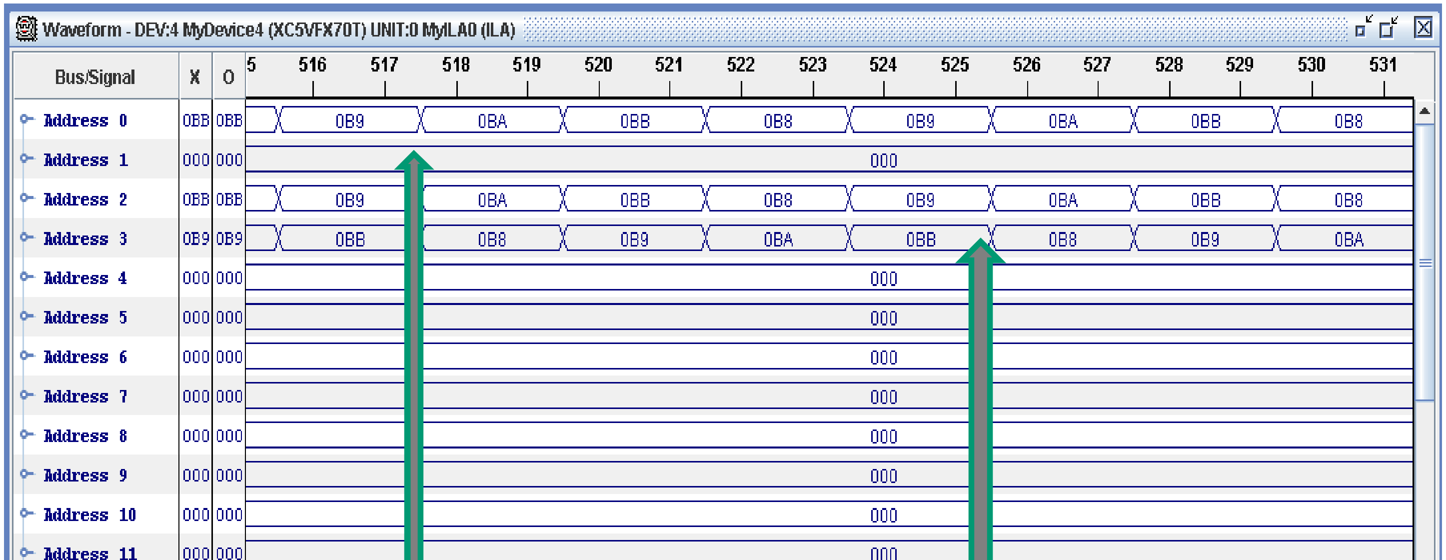


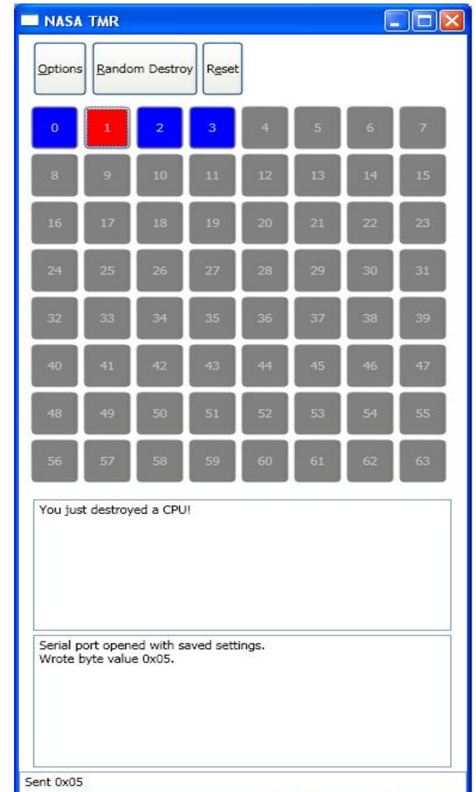
GUI indicates uP 0, 1, and 2 are active (blue)

System Demonstration

- **Hard Fault Recovery**

  - Processors **1** undergoes hard fault (induced by GUI, **red**)
  - The system shuts down uP #1 and brings on spare processor uP #3 into TMR





Processor 1 has hard fault so is shut down

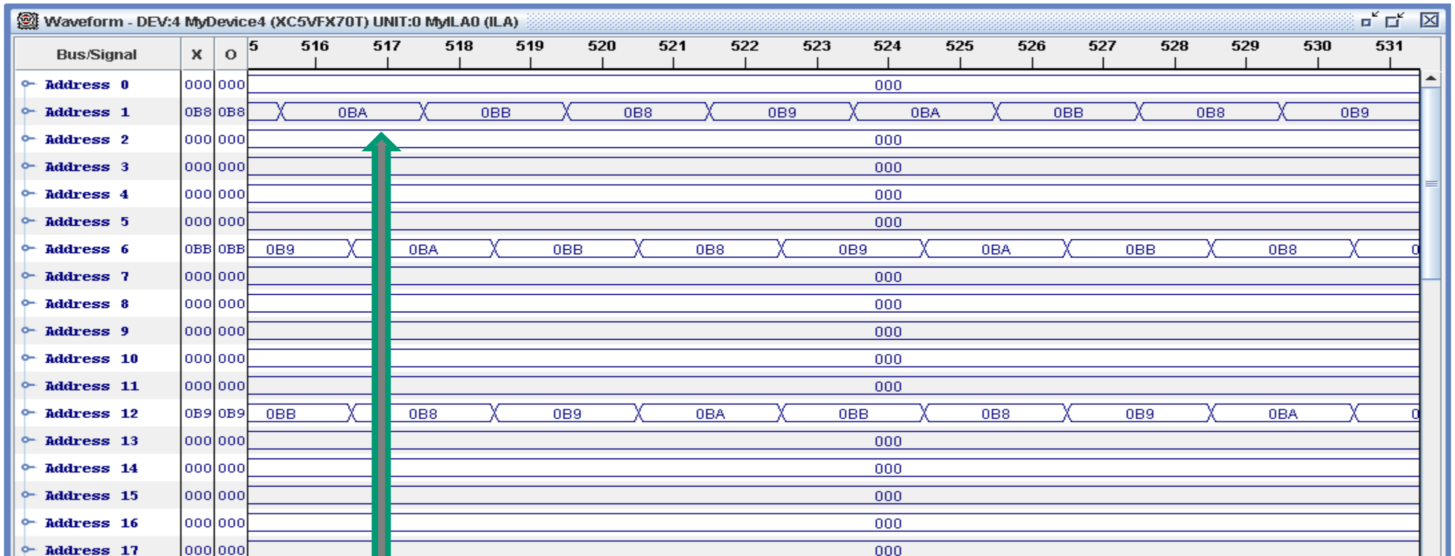
Spare processor 3 is brought online, resynchronized, and reinitialized to form TMR

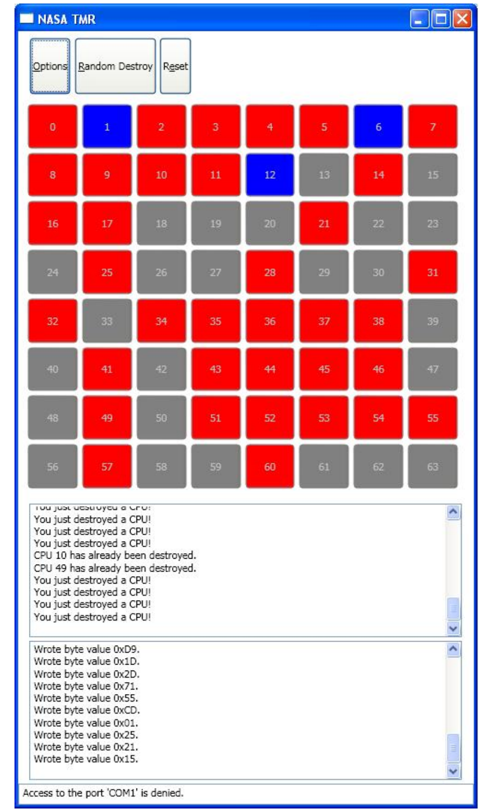
GUI indicates uP 1 is in hard fault (red). uP 0,2,3 form TMR (blue).

System Demonstration

- **Multiple Hard Faults**

  - Multiple hard faults are present
  - uPs 1, 6, and 12 form TMR





Processor 1, 6, & 12 are active

GUI indicates uP 1 , 6, & 12 are active. Multiple hard faults are present

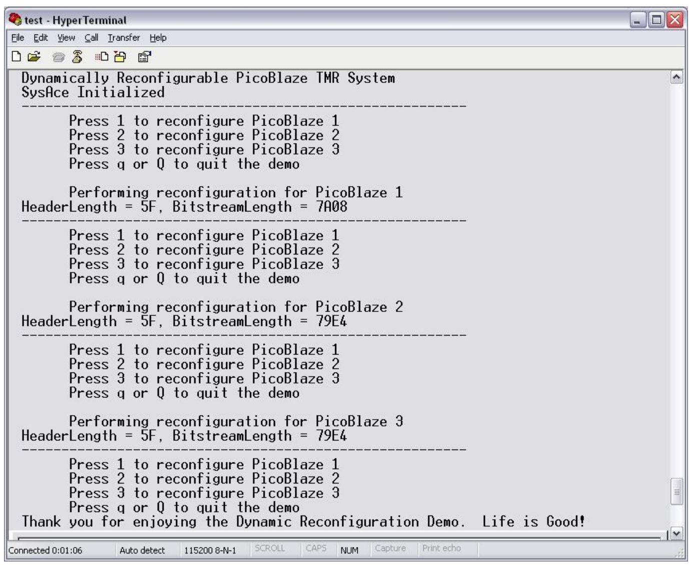
System Demonstration

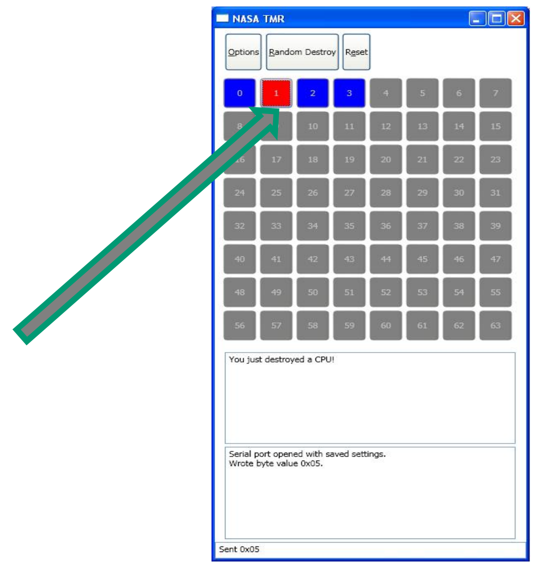
• Medium Severity Fault Recovery (PR)

- An initial hard failure can be *repaired* by going back to the effected processor and reconfiguring it.
- This handles the situation where an SEU occurred in the configuration RAM
- For this type of fault, a simple reset will not recover the processor

BUT

the processor hardware is still usable.





- Logistics: a MicroBlaze soft processor is used to read the PR bit streams through the SystemACE and write to the ICAP port of the Virtex-5.

Timing/Area Impact

- **Soft Fault Recovery** (reset, reload variable information)

Timing Overhead

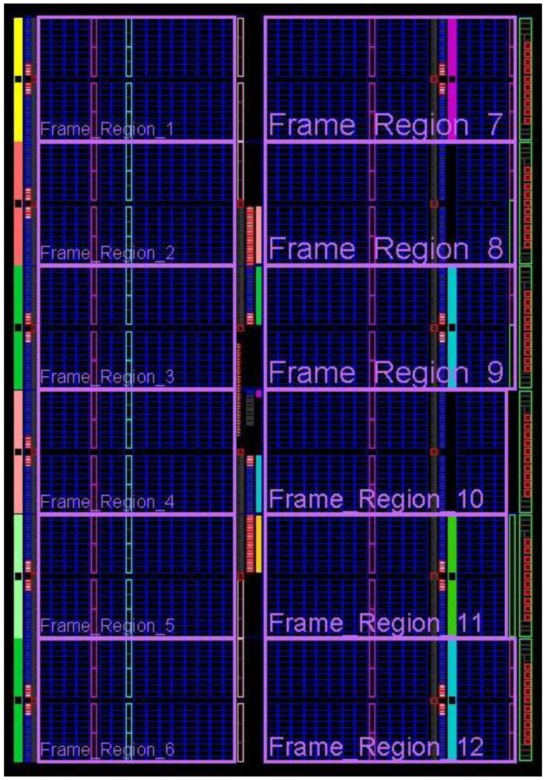
- TMR interrupt	2 clocks	
- Reset	2 clocks	
- Read variable data from good processors:	128 clocks	(2 clks/inst, 64 bytes of RAM)
- Write variable data to reset processor:	128 clocks	(2 clks/inst, 64 bytes of RAM)
Total	**260 clocks = 2.6 us**	(100 MHz V5 Clock)

Partial Reconfiguration Constraints

- **For our V5, the smallest quantum that can be partially reconfigured is 20 CLBs**

  - 1 CLB contains: *2 Slices*

  - 1 Slice contains: *- four LUTs*
    - four storage elements
    - wide-function multiplexers
    - carry logic



- **If you use BRAM in your design, 4 BRAMs must be partially reconfigured together**

- **Care must be given to placing circuitry within the smallest partially reconfigured tile**

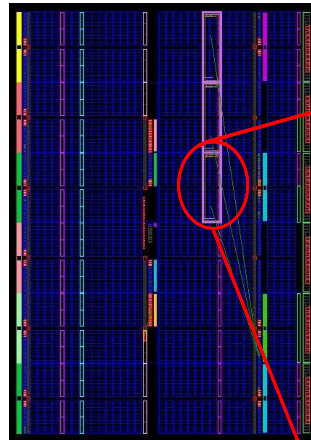
- **Bus Macros are used to provided fixed routing channels between tiles.**

PR of a *picoBlaze* Core

Physical *picoBlaze* resource estimation:

Site Type	Available	Required	% Util
LUT	320	163	50.94
FF	320	76	23.75
SLICEL	60	35	58.33
SLICEM	20	12	60.00
RAMBFIFO36	4	1	25.00

- 24 CLBs, 1 BRAM



PR <u>region</u> resource use:

- 2 columns of 20 CLBs
- 1 column of BRAM

Smallest picoBlaze PR Tile = 40 CLB + 4BRAM

Bitstream file size(LX50T):

- Partial bitstream for one PicoBlaze: 31.2 KB
- Full bitstream: 1,716 KB

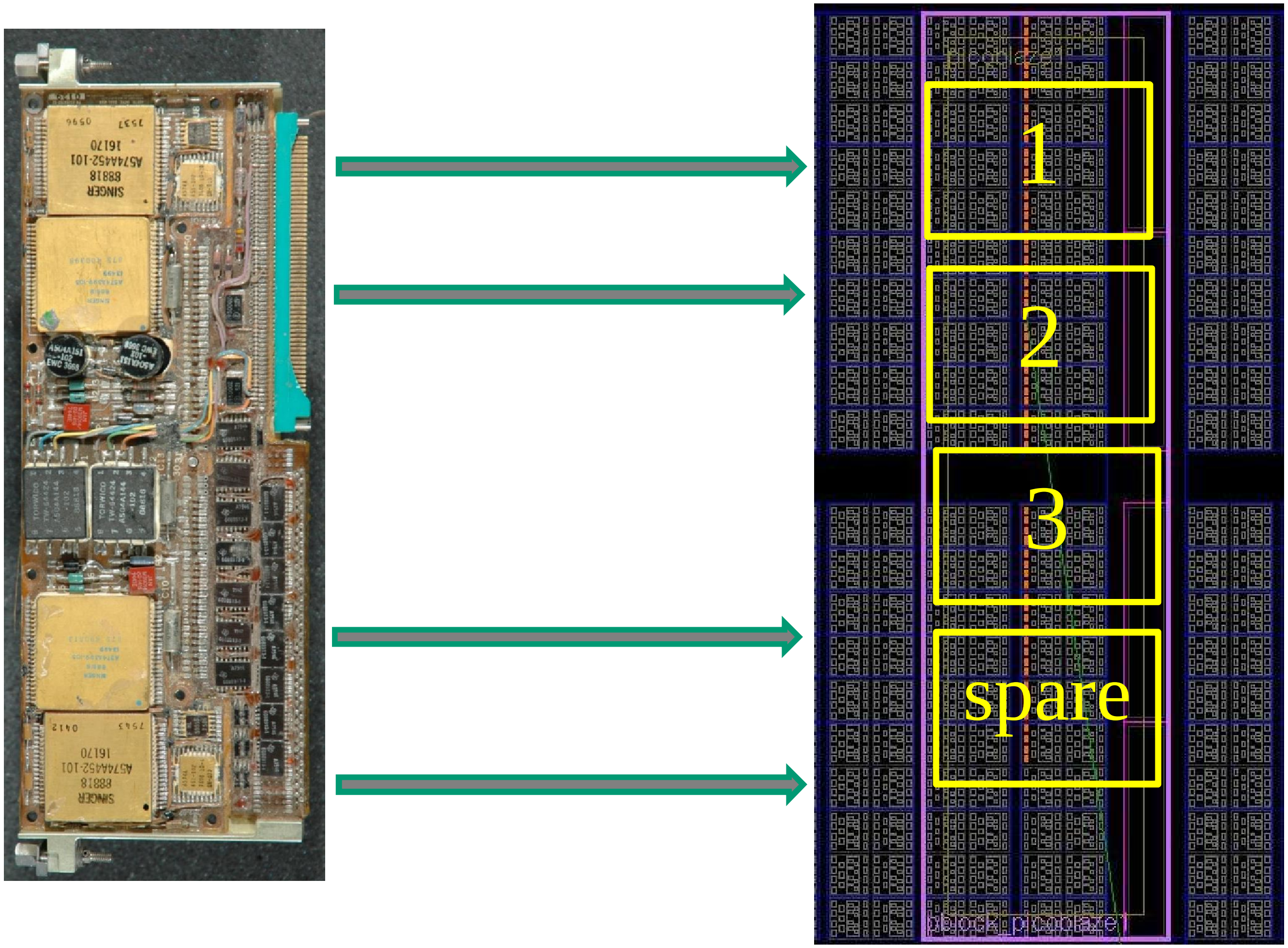
Reconfiguration time:

- Roughly 200 clks/Byte (measured)
- Measured time: **66ms** (100 MHz clk)
- Using MicroBlaze driven ICAP processor

A single PicoBlaze PR region

Future Work

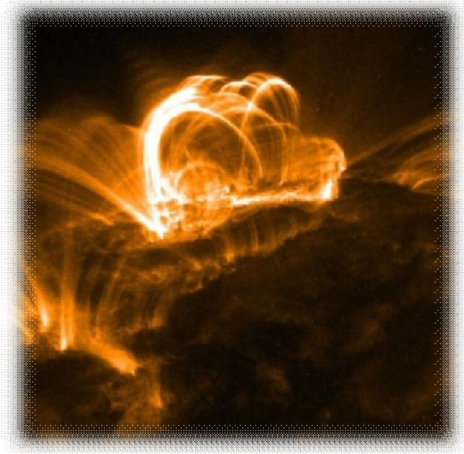
- ***microBlaze* Soft Processor**



Shuttle Processor Board

Virtex-5

Future Work



Questions?