Ionization radiation passing through the sensor creates electron hole pairs on an average energy rate of 3.6 eV per electron-hole pair. In silicon, 1 MeV of energy corresponds to 44.4 fC of charge, which is more than enough to flip the state of a logic circuit fabricated in a modern process. The integrated radiation sensor gives spatial location of radiation strikes for dynamic reconfiguration of the FPGA.

The energy of the radiation and the size of the depletion volume determine the amount of charge ultimately collected which is a function of the sensor design, materials, and bias voltage.

This sensor is a double sided strip detector (DSSD) based on a large area p-n junction. The electrodes in the radiation sensor are broken up into narrow electrically isolated strips running orthogonal to each other on opposite sides of the silicon substrate. Each strip will be monitored by a separate electronic channel. The location of the ionization particle is given by the position of the intersection of the strips receiving the signals from the front and back side electronics.

Thirty-six 1cm$^2$ individual die are created on each wafer: 16 direct contact double sided devices, 4 direct contact single sided devices, 12 capacitive coupled double sided devices, & 4 capacitive single sided devices.

There are also 3 test areas for measuring the sheet resistivity of the diffusion and metal layers on both sides of the wafer used to characterize the fabrication process.

The mask set was reduced to four individual masks by designing the mask set symmetrically such that they could be used for both surfaces of the wafer. The back side surface is rotated 90 degrees relative to front side pattern. Two different sensor designs are fabricated simultaneously with the mask set. One is a directly coupled p-n junction and the other uses capacitive coupling by creating a Metal-Oxide-Semiconductor junction.