Multi-Rate Systems
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Introduction

In this lab you will be exploring the effects of the rate changing blocks available in System Generator including the Upsample, Downsample, Serial to Parallel and Parallel to Serial blocks

Note: There is a completed example in lab5/solutions folder

Objectives

After completing this lab, you will be able to:

- Change the sample rates in a DSP System
- Convert a serial stream of data to a parallel word
- Convert a parallel word of data into a serial stream

Lab Setup

The following software is required to be installed on your system to successfully complete this lab

1. System Generator 8.2
2. ISE 8.2.01
3. ISE CORE Generator IP Update 1
4. MATLAB / Simulink R2006a
Procedure

1. Launch the MATLAB program and once invoked change directory to:
   C:\SysGen_Training_Labs\lab4

2. Open up a new Simulink diagram and create the simple diagram shown in Figure 1. Use the “Counter Limited” block from the Simulink/Sources library and set the upper limit of the counter to 10. Set the quantization of the Gateway In block to “fix [8 0]

3. Simulate the counter for 10 simulation cycles and observe the results.

4. Add a Downsampling Block form the Xilinx Blockset/Index library between the Gateway In /Gateway Out blocks and resimulate the design. What do you observe?

5. Replace the Down Sampling block with an Up Sampling block and resimulate the design. The System Generator token is going to generate an error that your sample rate is incorrect.

6. Double-click on the System Generator token and change the “Simulink System Period” to ½ as the message suggests. Resimulate the design.
Add a Sample Time probes from the Xilinx Blockset/Index library before and after the Up Sample block and connect the outputs of the probes to the Simulink/Sinks as shown in Figure 4. These probes don’t add any hardware to the design but offer a powerful debugging tool for complex multi-rate systems. Once complete, resimulate the design to observe the sample rate in the Display sinks.

![Diagram](image)

**Figure 4 – Simple counter with Up Sampling and Sample Time probes**

In the next section of the lab we will explore the rate changing effects of using the Serial to Parallel and Parallel to Serial blocks from the Xilinx Blockset.

7. Open up a new blank design and create the design shown in Figure 5.

![Diagram](image)

**Figure 5 – Serial to Parallel Example**

8. Set the limit on the “Counter Limited” block to 1. This is simply going to generate a sequence of “1010101010”.

9. Set the output of the Serial to Parallel block to “Unsigned [8 0]”.

![Property Editor](image)

**Figure 6 – Serial to Parallel Property Editor**

The Serial to Parallel block will impose a rate change on the system equal to the number of output bits / number of input bits. In this example we have 8 output bits and 2 input bits so the rate change will be set to 4.
10. OK the properties editor form and then add sample rate probes to the input and output of the Serial to Parallel Converter block. Resimulate the design and observe the sample rates

<table>
<thead>
<tr>
<th>Input Sample Rate</th>
<th>Output Sample Rate</th>
</tr>
</thead>
</table>

11. Change the output quantization of the Serial to Parallel Converter block to fix [16 0] and resimulate. What are the sample rates now?

<table>
<thead>
<tr>
<th>Input Sample Rate</th>
<th>Output Sample Rate</th>
</tr>
</thead>
</table>

12. Replace the Serial to Parallel Converter block with the Parallel to Serial block. Leave the output quantization at the default ufix [1 0].

13. Change the sample rate in the System Generator token from 1 to ½ and “OK” the form.

14. Resimulate the design and record the input and output sample rates

<table>
<thead>
<tr>
<th>Input Sample Rate</th>
<th>Output Sample Rate</th>
</tr>
</thead>
</table>

Note: You may get an error with the Sample Rate Probe connected to the output. If this occurs just temporarily connect the probe to the input signal, perform the simulation once, then reconnect it to the output signal again and resimulate.