CMOS LAB MANUAL

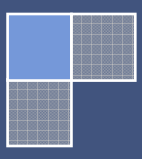
2009

CMOS LAB MANUAL

This manual was designed for use with the Montana Microfabrication Facility at MSU. The intention of the manual is to provide lab users and MSU students with a complete description of the methods used to fabricate CMOS devices on 4-inch silicon substrates.

Special Thanks to:
Andy Lingley
Phil Himmer

Author: Matthew Leone
Todd Kaiser
Montana State University
Rev1 - December 2008



SUPPLIERS

University of Minnesota Nano Fabrication Center (NFC): Photomasks
www.nfc.unm.edu

Virginia Semiconductor: Silicon Substrates
www.virginiasemi.com

EL-CAT Inc.: Silicon Substrates
www.el-cat.com

JT Baker: Chemical Supplies
www.jtbaker.com/default.asp

Technical Glass Products Inc: Quartz-ware
www.technicalglass.com

Kurt J Lesker Company: Evaporation Filaments
www.lesker.com

MSU Chem-store: Labware/Chemical Supplies
www.chemistry.montana.edu/chemstores

Sigma-Aldrich: Chemical Supplies
www.sigmaaldrich.com

SPI Supplies: Wafer Tweezers
http://www.2spi.com/spihome.html

Gases Plus: Pressurized Gas Tanks
www.gasesplus.com (406)388-9109

RECOMMENDATIONS FROM THE TEACHING ASSISTANT 2008:

The suggested high temperature process steps for future use in EE 407 labs are listed here.

wet oxidation	1000°C	180 min
N-well diffusion	900°C	20 min
drive-in	1000°C	600 min
wet oxidation	1000°C	90 min
N+ diffusion	900°C	60 min
wet oxidation	1000°C	90 min
P+ diffusion	1000°C	120 min
drive-in	1000°C	60 min
wet oxidation	1000°C	30 min
dry oxidation	1000°C	60 min

Brian Peterson
Montana State University
2008

NOTES/RECOMMENDATIONS FROM THE AUTHOR:

Previous fabrication attempts have been met with mixed success. In most cases the large-channeled NMOS transistors, resistors and diodes functioned properly. However, in some cases the threshold voltage was negative, indicating a depletion mode device and perhaps inappropriate dopant levels, but the diffusion times and temperatures showed no association. In many cases, the smaller channel devices failed to function and exhibited short circuit behavior.

The PMOS devices, including resistors, transistors and diodes nearly always failed. Numerous reasons were thought to explain for the failure but none have been proven as the cause. The most obvious reason for failure may just be an inappropriate doping level of either the N-well or P+ devices. The dopant concentrations may have been shifted due to segregation effects during oxide growth or thermal cycles. Or the failure may be caused from poor electrical contact to the diffused regions, perhaps a thin film of BSG or oxide was acting as a barrier between the aluminum and diffused silicon. Typically after Boron deposition, the resulting BSG film needs to be etched longer than necessary to remove thermal SiO_2. If insufficiently etched, the Boron-doped regions will appear blue-ish and if tested with the Nanospec or 4-proint probe will indicate oxide is present. This situation has been encountered in previous fabrication attempts.

From my experience and readings I would recommend trying the following modified fabrication sequence. If the process cannot be made successful by modifying etch times or diffusion schedules, I would recommend shifting the process from an N-well on P-type substrate to a P-well on N-type substrate. Other universities have incorporated this type of CMOS fabrication with successful results.

Matthew Leone
Montana State University
2007

Recommended CMOS Process:

Oxidation (wet):	1000°C	90 min
N-well Pre-deposition:	800°C	20 min
Oxidation (wet)	1050°C	60 min
N-well Drive-in:	1050°C	300 min
N+ S/D Pre-deposition:	850°C	20 min
Oxidation (wet):	1000°C	60 min
P+ S/D Pre-deposition:	950°C	20 min
Oxidation (dry):	1050°C	45 min

Long Oxide Etch in 6:1 BOE to remove BSG and SiO_2 from vias.

How to use this manual…

The manual is broken up into weekly segments containing multiple sections: *Goals, Equipment*, *Parameters*, *Methods* and *Results*. Each week a set of process goals is presented to the user along with a list of equipment and the methods used to achieve those goals. The parameters segment is devoted to process dependent parameters specific to the fabrication methods used that week. The parameters are color coded to correspond to a specific process method. The methods section describes the processes used within that week to achieve the desired goals. The methods are numbered to correspond to a process goal. The result section is left blank for users to record the results of that week's processes.

14-week Overview

Introduction & Oxidation	Week 1
Photolithography & Etching (N-well)	Week 2
Cleaning & Diffusion (N-)	Week 3
Documenting, Cleaning & Oxidation	Week 4
Photolithography & Etching (N+ Source/Drain)	Week 5
Cleaning & Diffusion (N+)	Week 6
Documenting, Cleaning & Oxidation	Week 7
Photolithography & Etching (P+ Source/Drain)	Week 8
Cleaning & Diffusion (P+)	Week 9
Documenting, Cleaning & Oxidation	Week 10
Photolithography & Etching (Vias)	Week 11
Cleaning & Aluminum Evaporation	Week 12
Photolithography, Etching (Pads) & Documenting	Week 13
Probing & Testing	Week 14

Introduction& Oxidation Week 1

GOALS:

1. Familiarize students with the cleanroom layout, equipment, safety and procedure.
2. Present an overview of the MEMS fabrication process and various processing techniques (i.e. photolithography, etching, etc)
3. Characterize the wafer substrates and ID individual wafers
4. RCA clean (Optional for new wafers)
5. Oxidation (Field oxide)

EQUIPMENT:

- Wafer Scribe
- JANDEL 4-point Probe Station
- RCA tanks (Optional)
- MODULAB Oxidation Furnace

PARAMETERS

Oxidation Parameters				
Temperature (°C)	Time (minutes)	Type (wet or dry)	N_2/O_2 Flow	Bubbler Setting
1000	180	Wet	7/9	40

Methods:

1. Clean Room Etiquette

The lab employs many hazardous chemicals and processes. The safety of the lab students and users is the number one priority when participating in the lab. Follow all gowning and safety procedures outlined by the lab TA.

To maintain the integrity of the wafers and the equipment, adhere to the process descriptions and details provided by the lab TA.

The most common reason a wafer will not make it to the end of the fabrication sequence, is poor handling. The wafer should be handled with the wafer-tweezers and with great attention. Limit the handling of the wafer with gloved hands to the edges and only during necessary circumstances. Never touch the wafer with a bare hand and never touch the center of the wafer, even with gloved hands.

When processing in the cleanroom, sources of contamination are another factor which may inhibit the success of the fabrication. Therefore, do not talk next to the wafers, keep the lid to the wafer box closed and lastly, do not hastily move about the clean room and do not get in a hurry to finish a process. When a lab student gets in a hurry it creates a situation with a greater likely hood of breaking a wafer or damaging a piece of equipment.

Methods:

2. Process Overview:

The CMOS devices are fabricated using common bulk silicon processing techniques. The sequence is a simple set of repeating steps including oxidation, etching, diffusion, cleaning and patterning. An overview of the sequence is shown to the right (**Figure 1**). The fabrication portion of the lab should take roughly thirteen weeks to complete, with the final week devoted to testing.

A layout of the die is shown in the bottom-right (**Figure 2**). A more complete description of the devices found on the die is found at the end of the document under the *Die Layout* section.

Document everything seen and done in a clean room lab notebook. Record all measureable quantities and procedures and any deviations. It is important to record every detail which may help explain device failures or anomalies.

3. Wafer Characterization and ID:

Semiconductor substrates, referred to as wafers, can easily be ordered through retailers and customized for specific applications. The wafers used for the lab are *100mm in diameter, 525±25 µm thick, <100>, single-side polished, single-crystal silicon, doped with boron (P-type) to a resistivity of 1-20 Ω/cm*.

A simple test to determine if the substrate is P-type or N-type silicon is known as the "Hot Probe Test." Using a DMM and a soldering iron, heat the positive probe of the DMM for several minutes with the soldering iron. Make sure the DMM is set to measure "mV." Place both probe tips, positive and negative(ground) to the wafer surface. If the DMM indicates a positive voltage the substrate is N-type, if the voltage is negative the substrate is P-type. This test should be accurate up to a resistivity of 1000 Ω/cm.

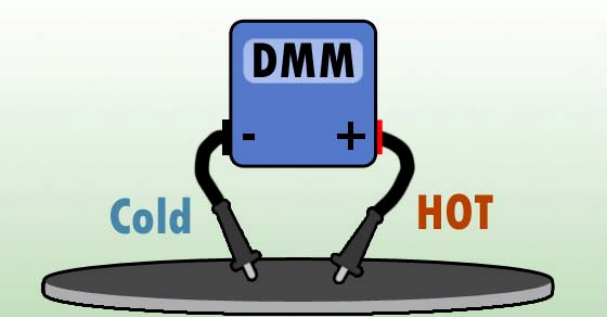


Figure 1 Overview of the fabrication sequence.

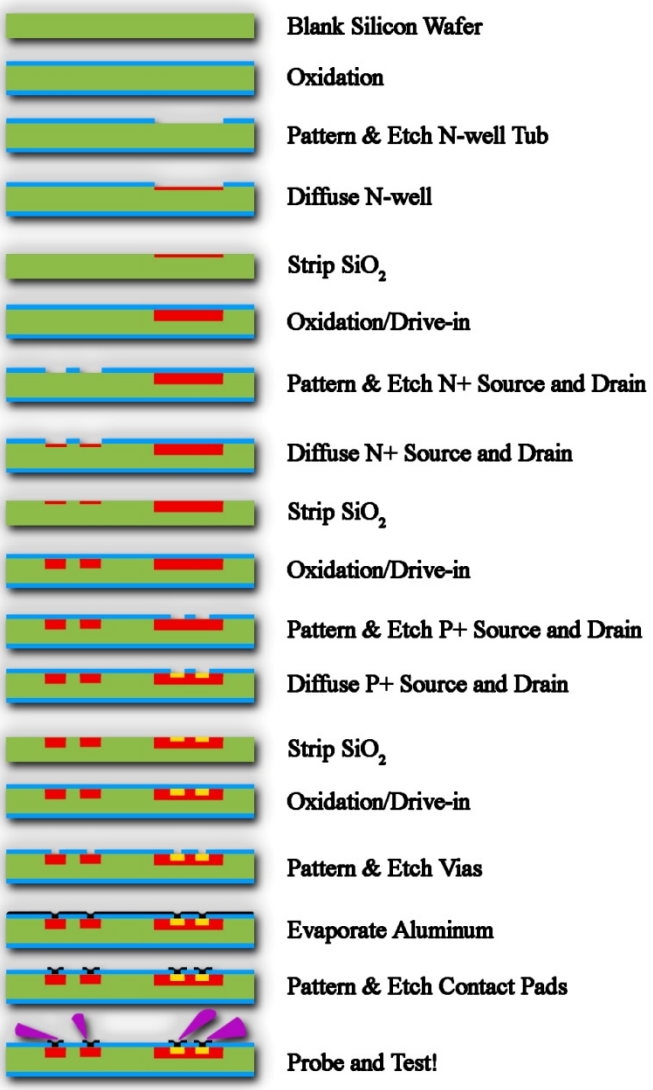
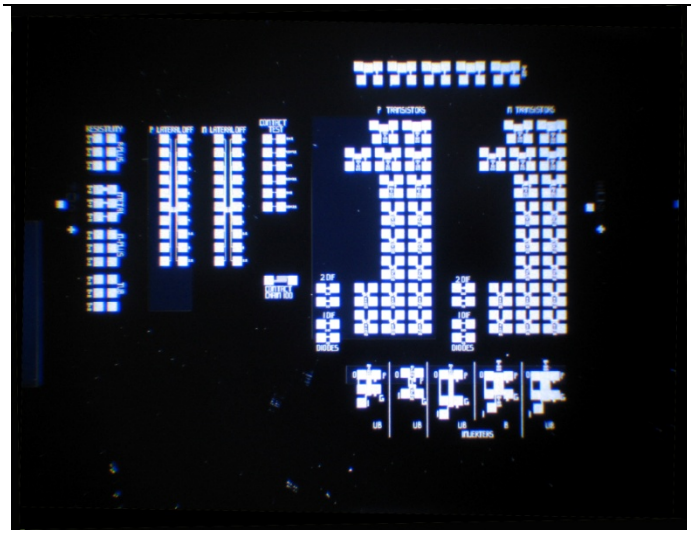


Figure 2 Microscope picture of the die layout. A more detailed description of the layout is found at the end of this document.



Methods:

3. Wafer Characterization and ID:

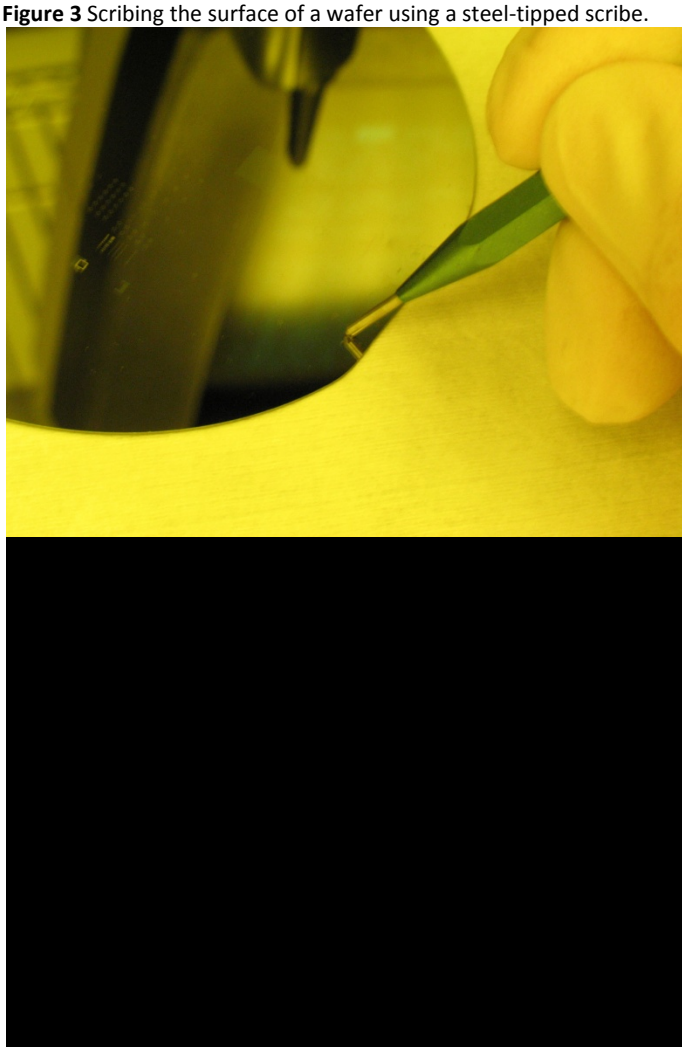
Continued…

The bulk resistivity (Ω-cm) is determined by first acquiring the sheet resistivity (Ω/□) of the wafers using the *JANDEL 4-point Probe Station* and then multiplying this value by the wafer thickness and a correction factor. See the JANDEL manual for details on using the 4-point probe.

To keep track of individual wafers, a scribe can be used to mark the **back** of the wafer with an identification mark, typically a number or letter.

Proceed by lightly pressing the tip of the scribe against the surface of the wafer and with as few strokes as possible 'scribe' a section number and wafer number. Scribing should be done as close to the edge as possible to limit the effect on fabricated devices.

Figure 3 Scribing the surface of a wafer using a steel-tipped scribe.



5. Oxidation: Growing SiO_2

(Check *Parameters* section for details)

The goal of the first oxidation run is to grow enough silicon dioxide (SiO_2) roughly a 0.5µm thick film, to mask the subsequent diffusion.

To oxidize, insert the wafers into the *MODULAB oxidation furnace* using the quartz rod and quartz boat (**see Figure 4**). There should be two dummy wafers, one at the front of the boat and another at the rear, to maintain uniformity across the boat. Ramp the furnace to 600°C before the removing the quartz boat and loading the wafers. Prior to the temperature reaching 400°C, turn on the nitrogen to purge the furnace. Also, set the potentiometer on the bubbler if performing a wet oxidation (which we are). Once the wafers are loaded and in place at the center of the furnace, ramp the furnace to the desired temperature. When the desired temperature is reached start the timer, stop the nitrogen flow and turn on the oxygen. After the allotted time, ramp the furnace down to 600°C, pull the boat, remove the wafers, and set them aside to cool. When finished, turn the furnace to 0°C and turn off the nitrogen when the temperature drops below 400°C.

Figure 4 A student using a quartz rod to insert wafers into the oxidation furnace.

RESULTS: Week 1

Sheet Resistance (Ω/□) & Resistivity (Ω-cm):

NOTES/CHANGES:

Photolithography & Etching (N-well) Week 2

GOALS:

1. Measure the thickness of the SiO_2 with the Nanospec.
2. Photolithography (Mask #1 N-well)
3. Hard-bake
4. Etch SiO_2

EQUIPMENT:

- Nanospec
- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- Teflon Cassette
- 6:1 BOE

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5250	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #1)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm^2)	UV Dose (J/cm^2)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Hard-bake Parameters

Hardbake Program	Temperature (°C)	Time (minutes)
#2	115	2

SiO_2 Etch Parameters ** for 4,200-4,500Å thick SiO_2 layer*

BOE concentration	SiO_2 Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5*	Shipley 1813 Photoresist

Methods:

1. Measuring the SiO_2 thickness:

The thickness of the freshly grown silicon dioxide layer is measured with the *Nanospec*. Choose the appropriate film type during the prompts and use a blank wafer as reference. Measure the thickness at several different points on the wafer to monitor uniformity and determine a maximum film thickness. Also note that the thickness of the SiO_2 determines the color of the wafer, therefore, color can be used to approximate film thicknesses and identify anomalies in film. For reference, the *Nanospec* prompts for measuring SiO_2 thickness are:

Is wavelength 480nm?	***Y*** ***(if not, type N and value)***
Data bank option?	***N***
Refr index option?	***N***
Switch to printer?	***N***
Enter film type:	***1-SiO2***
Enter obj lens:	***1 = 10x***

2. Photolithography with Mask #1 (N-well): Spin-coating & Soft-baking

(Check *Parameters* section for details)

The goal of the photolithography step is to transfer patterns from the mask set to the wafer surface. Photoresist, which is a UV sensitive chemical, is patterned by selectively exposing certain regions with UV light. Photoresist is also chemically resistant to the SiO_2 etchant, hydrofluoric acid (also referred to as BOE); therefore it is used to mask, or block, select portions of the SiO_2 from being etched. The first patterns transferred to the wafer are the N-wells, which will act as a substrate for the PMOS devices.

Begin by using the *BREWER spin-coater* to spin a thin film (~1um) of *SHIPLEY 1813* photoresist onto the topside of the wafer. Next, transfer the wafer to the adjacent hotplate and soft-bake to remove solvents and harden the resist. A good coating of photoresist will be barely visible to the naked eye and have a minimal number of streaks or blotches (**see Figure 7**). If there are a large number of defects, solvent clean, dehydrate, and try re-spinning more photoresist.

Figure 5 Students using the Nanospec to measure the SiO_2 thickness.

Figure 6 View from the Nanospec eyepiece, the edge of the octagon should be in focus for proper measurement.

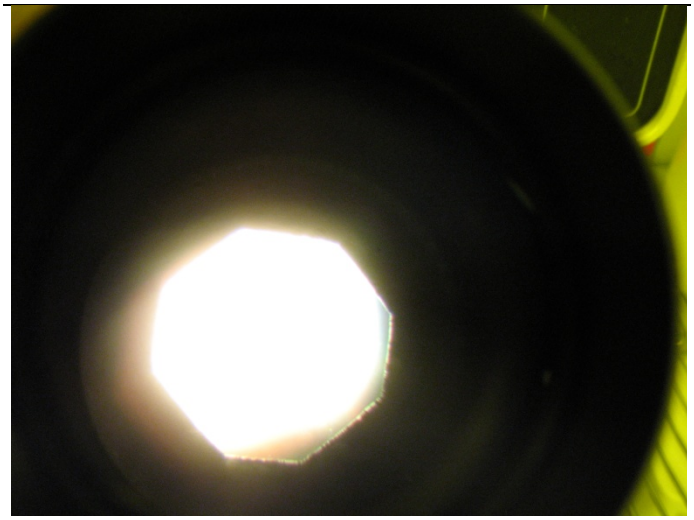
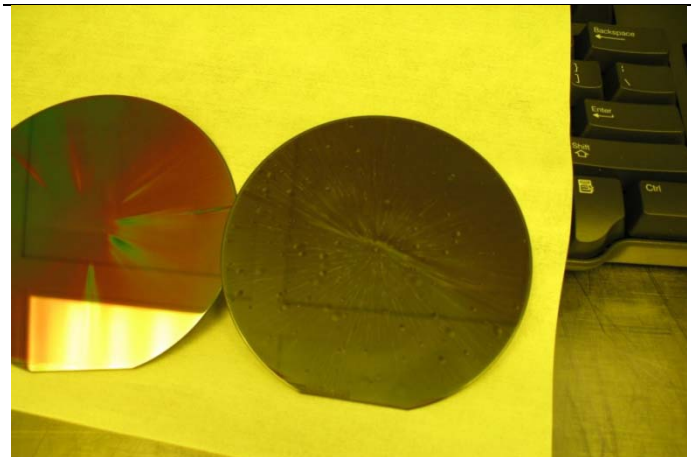


Figure 7 Wafers that have been spun with photoresist and exhibit signs of a poor coating i.e. streaking, blotchiness and color gradients



Methods:

2. Photolithography with Mask #1 (N-well): Exposure & Development

(Check *Parameters* section for details)

Proceed by patterning the photoresist with Mask #1. Start by loading the mask onto the *ABM contact-aligner* mask stage. Turn the mask-vac on and raise the mask stage. Carefully, load the wafer onto the substrate chuck and orient it such that the <110> plane (wafer flat) is to the left and running straight up and down. Turn on the substrate-vac to lock the wafer in place and lower the chuck to avoid hitting the contact mask. Next, lower the mask stage and raise the substrate chuck up to meet the mask, fringe lines will become visible as the wafer and mask come into contact. Align the mask to the wafer using the markers on the sides of the wafer (no alignment for the first photolithography step). Turn on the contact-vac to remove any air gap between mask and wafer. Adjust the exposure time and channel setting then expose. Remove the wafer by turning off the contact-vac, lowering the substrate chuck, raising the mask frame, and turning off the substrate-vac. Transfer the wafer to a dish of *MF319 developer* (a faint outline of the features can be seen at this point), submerge the wafer in MF319 and gently swirl for 30-60 seconds until the exposed resist is completely dissolved. If done correctly there should be no photoresist left in the n-well regions. If there is (**see Figure 8**), resubmerge the wafer in the MF319 developer for additional time. If unsuccessful, use a solvent clean to strip the photoresist, dehydrate and re-spin again. When finished, pour the used MF319 into the MF319 waste container located under the solvent bench next to the photoresist.

3. Hard-baking:

(Check *Parameters* section for details)

Hard-baking is the final step in the photolithography sequence, but to emphasize its importance it gets its own heading. The goal of the hard-bake is to remove any remaining solvents and/or water from the resist. It has been observed, that without hard-baking, the photoresist exhibits adhesion problems and frequently delaminates from the surface during etching. Hard-baking is very similar to soft-baking and follows the same procedure. Load a wafer onto a *hotplate* for a set time at the appropriate temperature.

Figure 8 A microscope picture of a patterned feature after development in MF319. The color gradient indicates that the photoresist was not completely removed during the development. The wafer should be developed for longer or redone with a longer exposure.

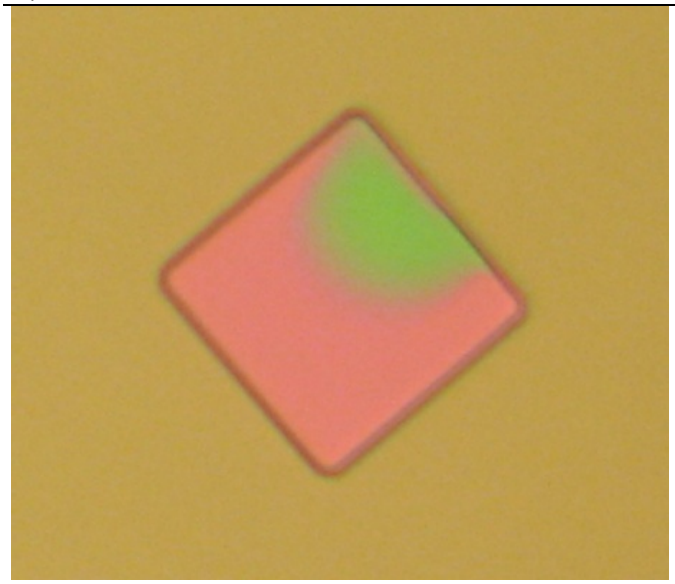
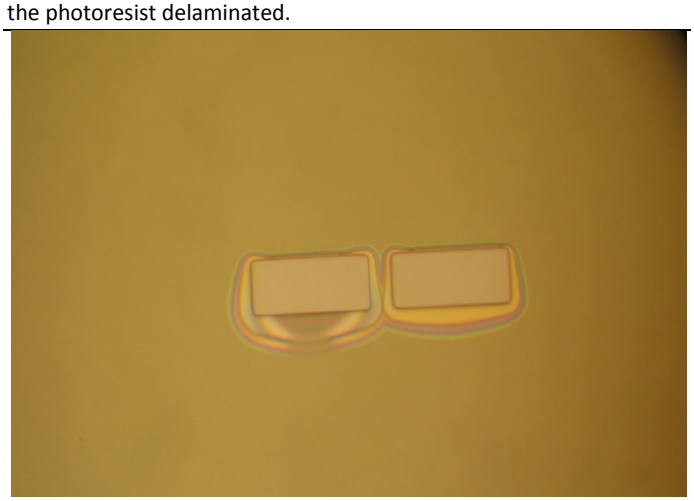


Figure 9 Several features indicating photoresist adhesion problems after etching SiO_2. The color gradient shows a tapered SiO_2 etch after the photoresist delaminated.



Methods:

4. Etching the SiO_2:

(Check *Parameters* section for details)

The goal of the SiO_2 etch is to remove the silicon dioxide from the exposed regions in the photoresist. Silicon dioxide is etched with BOE (Buffered Oxide Etch) which is a combination of hydrofluoric acid and buffering chemicals to stabilize the reaction. BOE is highly selective to silicon dioxide so the photoresist will not be etched.

This step should be carried out by the lab TA for safety reasons. Begin by loading the wafers into a *Teflon cassette* with equal spacing between wafers. Using the handle, submerge the cassette in *6:1 BOE* for the appropriate amount of time or until the exposed SiO_2 is completely removed. To determine if the SiO_2 is completely removed, check the regions for color (**see Figure 10**) and hydrophobicity. When the etch is complete, remove the cassette and rinse the wafers in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers with DI water and nitrogen gun.

Figure 10 An example of micromasking with features that were etched but had undeveloped photoresist masking the etch. The blue color indicates that SiO_2 still remains over those features. The white color is bare silicon. Micromasking can usually be solved with a descum etch (dry O_2 plasma etch) before etching in BOE.

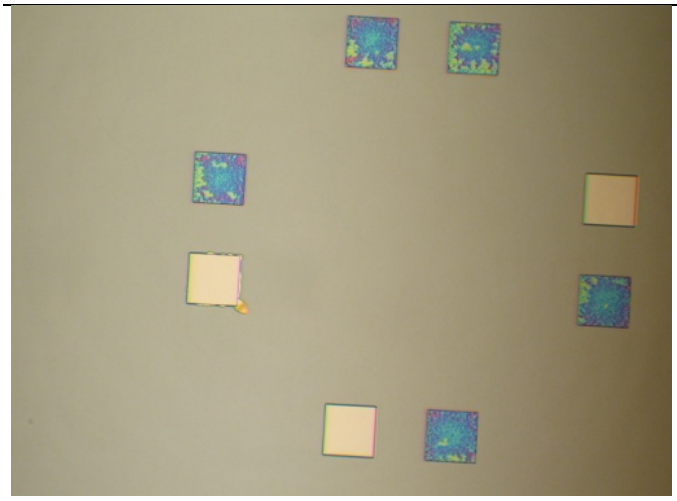
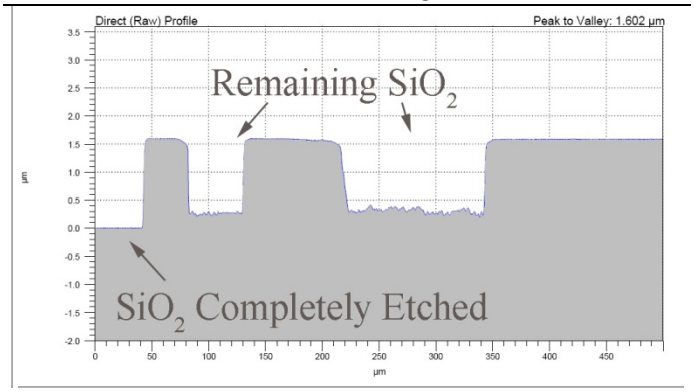


Figure 11 A profilometer measurement in reference to Figure 10. The data indicates that a small amount (250nm) of SiO_2 remains in etched windows. This SiO_2 will inhibit the following diffusion.



RESULTS: Week 2

SiO_2 Thickness (Å):

NOTES/CHANGES:

Cleaning & Diffusion (N-) Week 3

GOALS:

1. Full Wafer Clean (Solvent & RCA)
2. Phosphorus Diffusion

EQUIPMENT:

- Acetone, Methanol, Isopropyl
- MODULAB Phosphorous Diffusion Furnace
- PHOSPLUS TP-250 Phosphorous Sources
- RCA Clean Tanks

PARAMETERS:

RCA Clean Parameters					
Piranha Solution	Piranha Etch Time (minutes)	BOE solution	BOE Etch Time (seconds)	Ionic Clean	Ionic Clean Etch Time (minutes)
3:1 H_2O_2:H_2SO_4	10	6:1	10	6:1:1 H_2O:H_2O_2:HCl	10

Phosphorous Diffusion Parameters (N-well)			
Boron Source	Temperature (°C)	Time (minutes)	N_2 Flow
PHOSPLUS TP-250	900	20	7

Drive-in Parameters (N-well)			
Boron Source	Temperature (°C)	Time (minutes)	N_2 Flow
None	1000	600	7

Methods:

1. Wafer Cleaning:

(Check *Parameters* section for details)

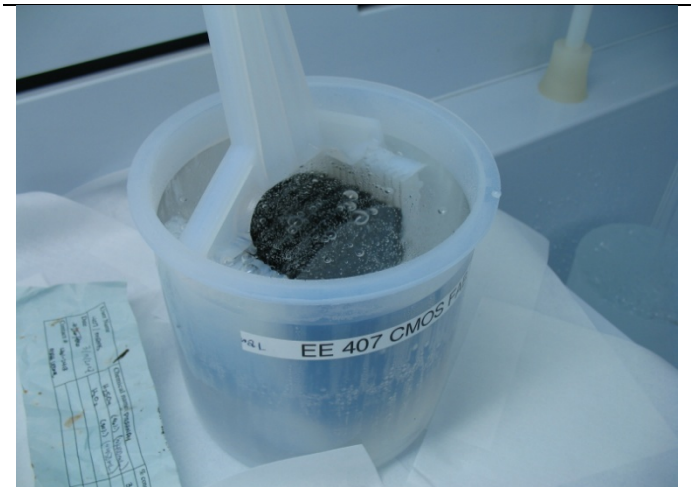
The wafers need to be cleaned to remove photoresist, and any possible sources of contamination before being placed in a high temperature furnace.

To remove the photoresist a solvent clean is performed. Begin by placing an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with *acetone* using the squirt bottle, and follow with *methanol* and *isopropyl.* The acetone will remove the photoresist and the methanol and isopropyl with remove any acetone residue. Rinse the wafers in DI water and dry with a nitrogen gun. When finished pour the solvent waste into the *Solvent Waste Container*.

To remove possible sources of contamination a modified RCA clean is performed. The RCA clean consists of rinsing the wafers in three chemical solutions. The first is a mixture of sulfuric acid and hydrogen peroxide known as Piranha etch. The piranha etch will remove any organic material. The second mixture is a simple BOE solution which will strip any native oxide that has accumulated on the wafer surface. The third and final solution is designed to remove any heavy metal ions, it is a mixture of hydrochloric acid, water and hydrogen peroxide. This solution is referred to as *ionic clean*

This step should also be carried out by the lab TA. Load the wafers into a *Teflon cassette* transfer the cassette between the RCA solutions until the cleaning is complete. Rinse the wafers and cassette in a bucket of DI water then pull each wafer and rinse and dry by hand.

Figure 12 Wafers submerged in Piranha Etch to remove organic contaminates.



6. Phosphorous Diffusion:

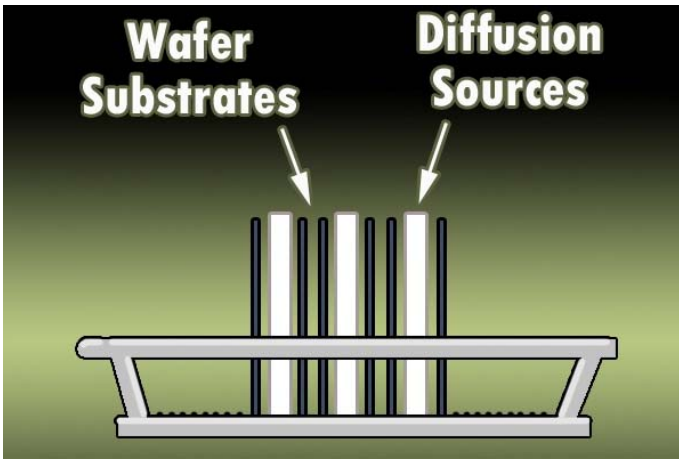
(Check *Parameters* section for details)

The goal of the phosphorous diffusion is to flip the polarity of the P-type substrate in the N-wells. In other words, the diffusion will create N-type silicon areas on the wafer. These N-wells or TUBS will act as the substrate for the PMOS devices.

The diffusion is modeled as a solid-solubility-limited diffusion followed by several drive-in steps. The expected resistivity can be derived from this model and verified with the PHOSPLUS data sheet.

To diffuse N-type (Phosphorous) material, ramp the *MODULAB Phosphorous Diffusion Furnace* to 600°C and set the nitrogen flow. Remove the quartz boat with the solid, white, *PHOSPLUS TP-250 sources* already in place. Load the silicon wafers next to the sources with the patterned side facing a source (**see Figure B**). Insert the quartz boat to the center of the furnace and ramp the furnace to the desired temperature. When the desired temperature is reached start the timer. After the allotted time, ramp the furnace down to 600°C, pull the quartz boat and remove the wafers and set them aside to cool. When finished, turn the furnace to 0°C and turn off the nitrogen when the temperature drops below 400°C.

Figure B An illustration of how the wafers are loaded into the quartz boat next to the diffusion sources.



RESULTS: Week 3

RESULTS:

NOTES/CHANGES:

Documenting, Cleaning & Oxidation Week 4

GOALS:

1. Take pictures using the microscope and digital camera.
2. Strip the SiO_2 & PSG
3. Obtain 4-point probe measurements of the diffusion
4. RCA clean
5. Oxidation

EQUIPMENT:

- Optical Microscope
- 6:1 BOE
- Teflon cassette
- JANDEL 4-point Probe Station
- RCA Clean tanks
- MODULAB Oxidation Furnace
- CANON Digital Camera

PARAMETERS:

SiO_2 Etch Parameters ** for 4,200-4,500Å thick SiO_2 layer*			
BOE concentration	SiO_2 Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5*	none

RCA Clean Parameters					
Piranha Solution	Piranha Etch Time (minutes)	BOE solution	BOE Etch Time (seconds)	Ionic Clean	Ionic Clean Etch Time (minutes)
3:1 H_2O_2:H_2SO_4	10	6:1	10	6:1:1 H_2O:H_2O_2:HCl	10

Oxidation Parameters				
Temperature (°C)	Time (minutes)	Type (wet or dry)	N_2/O_2 Flow	Bubbler Setting
1000	90	Wet	7/9	40

Methods:

1. Taking Pictures:

With the first diffusion completed, the wafers now have observable features. From this point, one goal of the lab is to document the fabrication progress by taking pictures of the surface of the wafer as it moves through the sequence. Begin by using the *optical microscope* and *CANON digital camera* to take a picture of the diffused N-well (**shown in Figure 13**)

Figure 13 A diffused N-well. The added dopants create the different color.

4. Stripping the SiO_2 and PSG:

(Check *Parameters* section for details)

Prepare the wafer surface for the next oxidation by completely removing all the SiO_2 and PSG.

REPEAT: This step should be carried out by the lab TA for safety reasons. Begin by loading the wafers into a *Teflon cassette* with equal spacing between wafers. Using the handle, submerge the cassette in *6:1 BOE* for the appropriate amount of time or until the exposed SiO_2 is completely removed. To determine if the SiO_2 is completely removed, check the regions for color (**see Figure 9**) and hydrophobicity. When the etch is complete, remove the cassette and rinse the wafers in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers with DI water and nitrogen gun.

Figure 14 A lab TA handling acids at the rinse sink with full acid protection clothing. Note the facemask, apron, and chemical gloves.

3. Diffusion Measurements:

There is a large diffused rectangle/square test region. This region is used to measure the sheet-resistivity associated with the phosphorus N-well diffusion (**see Figure 16 next page**). Use the *JANDEL 4-point probe* to measure the sheet resistivity of the diffusion. Start by raising the probe arm, uncapping the tip and placing the wafer on the stage. Align the probes over the test region and lower the arm into contact. Start the test by using a small current, roughly 100nA, and increment the current until the sheet resistivity stabilizes. Consult the JANDEL 4-point probe manual for further assistance. The measured sheet resistivity should correspond to the value found on this PHOSPLUS data sheet for the appropriate time and temperature (**see Figure 17 next page**).

Figure 15 A student using the JANDEL 4-point probe to document the sheet resistivity of the diffusion.

Methods:

Figure 16 An outline of the wafer diffusion test regions. The area in pink is diffused as N- and should be tested with the 4-point probe.

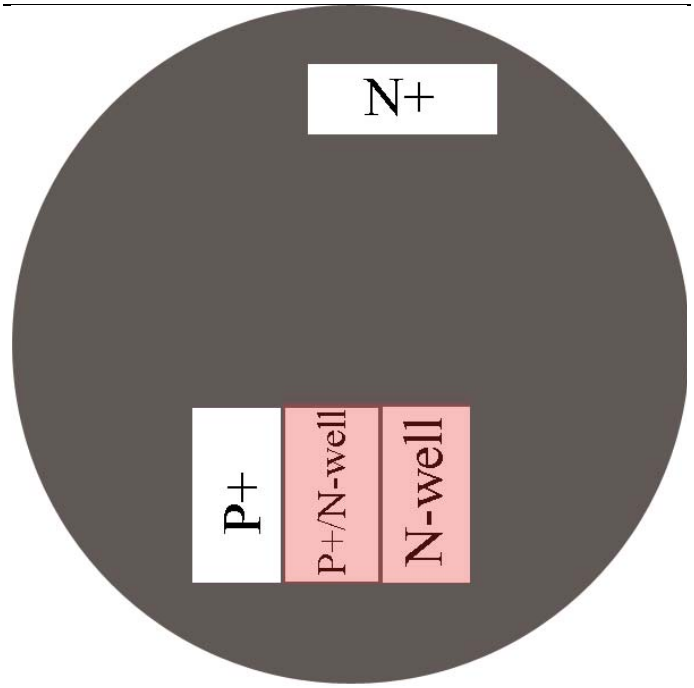
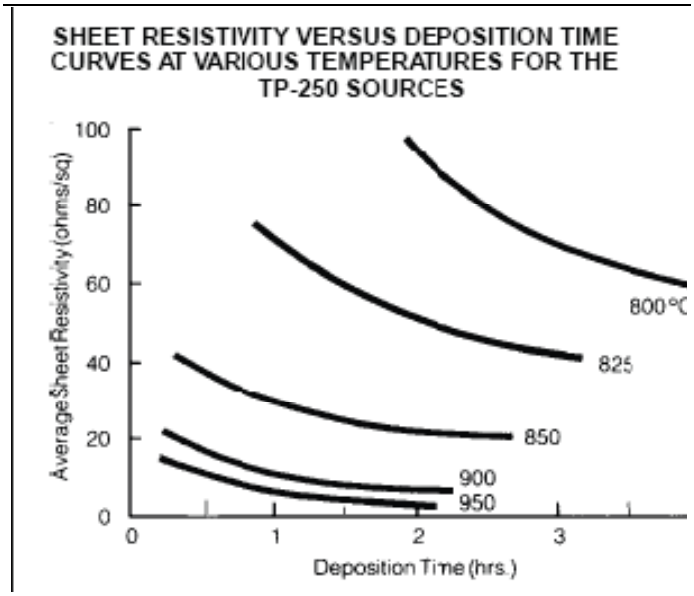


Figure 17 A graph from the PhosPlus datasheet illustrating the relationship between diffusion time, temperature and sheet resistivity. The graph should be used to verify sheet-resistivity measurements.



4. RCA Cleaning:

(Check *Parameters* section for details)

REPEAT: To remove possible sources of contamination a modified RCA clean is performed. The RCA clean consists of rinsing the wafers in three chemical solutions: Piranha etch, BOE, Ionic clean.

This step should be carried out by the lab TA for safety. Load the wafers into a *Teflon cassette* transfer the cassette between the RCA solutions until the cleaning is complete. Rinse the wafers and cassette in a bucket of DI water then pull each wafer and rinse and dry by hand.

5. Oxidation: Growing SiO_2

(Check *Parameters* section for details)

The goal of the second oxidation run is the same as the first: grow enough silicon dioxide (SiO_2) roughly a 0.5µm thick film, to mask the subsequent diffusion.

REPEAT: To oxidize, insert the wafers into the *MODULAB oxidation furnace* using the quartz rod and quartz boat (**see Figure 4**). There should be two dummy wafers, one at the front of the boat and another at the rear, to maintain uniformity across the boat. Ramp the furnace to 600°C before the removing the quartz boat and loading the wafers. Prior to the temperature reaching 400°C, turn on the nitrogen to purge the furnace. Also, set the potentiometer on the bubbler if performing a wet oxidation (which we are). Once the wafers are loaded and in place at the center of the furnace, ramp the furnace to the desired temperature. When the desired temperature is reached start the timer, stop the nitrogen flow and turn on the oxygen. After the allotted time, ramp the furnace down to 600°C (or 0°C if finished with furnace), pull the boat, remove the wafers, and set them aside to cool. When the temperature drops below 400°C the nitrogen can be turned off.

RESULTS: Week 4

Sheet Resistance (Ω/□) & Resistivity (Ω-cm):

NOTES/CHANGES:

Photolitho & Etching(N+ Source/Drain) Week 5

GOALS:

1. Measure the thickness of the SiO_2 layer with the Nanospec.
2. Photolithography
   (Mask #2 N+ Source/Drain)
3. Hard-bake
4. Etch SiO_2

EQUIPMENT:

- Nanospec
- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- Teflon Cassette
- 6:1 BOE

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5250	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #2)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm^2)	UV Dose (J/cm^2)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Hard-bake Parameters

Hardbake Program	Temperature (°C)	Time (minutes)
#2	115	2

SiO_2 Etch Parameters ** for 4,200-4,500Å thick SiO_2 layer*

BOE concentration	SiO_2 Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5*	Shipley 1813 Photoresist

Methods:

1. Measuring the SiO_2 thickness:

Measure the thickness of the silicon dioxide at several different points on the wafer using the *Nanospec*. For reference, the Nanospec prompts for measuring SiO_2 thickness are:

Is wavelength 480nm?	***Y (if not, type N and value)***
Data bank option?	***N***
Refr index option?	***N***
Switch to printer?	***N***
Enter film type:	***1-SiO2***
Enter obj lens:	***1 = 10x***

2. Photolithography with Mask #2 (N+ S/D): Spin-coating & Soft-baking

(Check *Parameters* section for details)

The second mask contains the features for the NMOS sources and drains.

REPEAT: Begin by using the *BREWER spin-coater* to spin a thin film of *SHIPLEY 1813* photoresist onto the topside of the wafer. Next, transfer the wafer to the adjacent hotplate and soft-bake to remove solvents and harden the resist. A good coating of photoresist will be barely visible to the naked eye and have a minimal number of streaks or blotches (**see Figure 7**). If there are a large number of defects, solvent clean, dehydrate, and try re-spinning more photoresist.

Figure 18 Students and professor looking on as a wafer is aligned and exposed at the ABM contact aligner.

2. Photolithography with Mask #2 (N+ S/D): Exposure & Development

(Check *Parameters* section for details)

Proceed by patterning the photoresist with Mask #2.

REPEAT: Load the mask onto the *ABM contact-aligner* mask stage. Turn the mask-vac on and raise the mask stage. Carefully, load the wafer onto the substrate chuck and orient it such that the <110> plane (wafer flat) is to the left and running straight up and down. Turn on the substrate-vac to lock the wafer in place and lower the chuck to avoid hitting the contact mask. Next, lower the mask stage and raise the substrate chuck up to meet the mask, fringe lines will become visible as the wafer and mask come into contact. Align the mask to the wafer using the markers on the sides of the wafer. Turn on the contact-vac to remove any air gap between mask and wafer. Adjust the exposure time and channel setting then expose. Remove the wafer by turning off the contact-vac, lowering the substrate chuck, raising the mask frame, and turning off the substrate-vac. Transfer the wafer to a dish of *MF319 developer* (a faint outline of the features can be seen at this point), submerge the wafer in MF319 and gently swirl for 30-60 seconds until the exposed resist is completely dissolved. If done correctly there should be no photoresist left in the diffusion contact regions (**see Figure 8**). If there is, resubmerge the wafer in the MF319 developer for additional time. If unsuccessful, use a solvent clean to strip the photoresist, dehydrate and re-spin again. When finished, pour the used MF319 into the MF319 waste container located under the solvent bench next to the photoresist.

Methods:

3. Hard-baking:

(Check *Parameters* section for details)

REPEAT: It has been observed, that without hard-baking, the photoresist exhibits adhesion problems and frequently delaminates from the surface during etching. Hard-baking is very similar to soft-baking and follows the same procedure. Load a wafer onto a *hotplate* for a set time at the appropriate temperature.

4. Etching the SiO_2:

(Check *Parameters* section for details)

REPEAT: This step should be carried out by the lab TA for safety reasons. Begin by loading the wafers into a *Teflon cassette* with equal spacing between wafers. Using the handle, submerge the cassette in *6:1 BOE* for the appropriate amount of time or until the exposed SiO_2 is completely removed. To determine if the SiO_2 is completely removed, check the regions for color (**see Figure 9**) and hydrophobicity. When the etch is complete, remove the cassette and rinse the wafers in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers with DI water and nitrogen gun.

RESULTS: Week 5

SiO_2 Thickness (Å):

NOTES/CHANGES:

Cleaning & Diffusion (N+) Week 6

GOALS:

1. Full Wafer Clean (Solvent & RCA)
2. Phosphorous Diffusion

EQUIPMENT:

- RCA Tanks
- Acetone, Methanol, Isopropyl
- Phosphorous Diffusion Furnace
- PHOSPLUS TP-250 Phosphorous Sources
- Teflon Cassette

PARAMETERS:

RCA Clean Parameters					
Piranha Solution	Piranha Etch Time (minutes)	BOE solution	BOE Etch Time (seconds)	Ionic Clean	Ionic Clean Etch Time (minutes)
3:1 H_2O_2:H_2SO_4	10	6:1	10	6:1:1 H_2O:H_2O_2:HCl	10

Boron Diffusion Parameters (N+)			
Boron Source	Temperature (°C)	Time (minutes)	N_2 Flow
PHOSPLUS TP-250	900	60	7

Methods:

1. Wafer Cleaning:

(Check *Parameters* section for details)

The wafers need to be cleaned to remove photoresist, and any possible sources of contamination before being placed in a high temperature furnace.

REPEAT: To remove the photoresist a solvent clean is performed. Begin by placing an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with *acetone* using the squirt bottle, and follow with *methanol* and *isopropyl*. The acetone will remove the photoresist and the methanol and isopropyl with remove any acetone residue. Rinse the wafers in DI water and dry with a nitrogen gun. When finished pour the solvent waste into the *Solvent Waste Container*.

REPEAT: To remove possible sources of contamination a modified RCA clean is performed. This step should be carried out by the lab TA. Load the wafers into a *Teflon cassette* transfer the cassette between the RCA solutions until the cleaning is complete. Rinse the wafers and cassette in a bucket of DI water then pull each wafer and rinse and dry by hand,

6. Phosphorous Diffusion:

(Check *Parameters* section for details)

The goal of the phosphorous diffusion is to create highly doped N-type silicon to act as the sources and drains of the NMOS transistors.

REPEAT: To diffuse N-type (Phosphorous) material, ramp the *MODULAB Phosphorous Diffusion Furnace* to 600°C and set the nitrogen flow. Remove the quartz boat with the solid, white, *PHOSPLUS TP-250 sources* already in place. Load the silicon wafers next to the sources with the patterned side facing a source. Insert the quartz boat to the center of the furnace and ramp the furnace to the desired temperature. When the desired temperature is reached start the timer. After the allotted time, ramp the furnace down to 600°C (or 0°C if finished with furnace), pull the quartz boat and remove the wafers and set them aside to cool. When the temperature drops below 400°C the nitrogen can be turned off.

RESULTS: Week 6

RESULTS:

NOTES/CHANGES:

Documenting, Cleaning & Oxidation Week 7

GOALS:

1. Take pictures using the microscope and digital camera
2. Strip the SiO_2 and PSG
3. Obtain 4-point probe measurements of the diffusion
4. RCA clean
5. Oxidation

EQUIPMENT:

- Optical Microscope
- CANON Digital Camera
- 6:1 BOE
- Teflon Cassette
- JANDEL 4-point Probe Station
- RCA Tanks
- MODULAB Oxidation Furnace

PARAMETERS:

SiO_2 Etch Parameters ** for 4,200-4,500Å thick SiO_2 layer*			
BOE concentration	SiO_2 Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5*	none

RCA Clean Parameters					
Piranha Solution	Piranha Etch Time (minutes)	BOE solution	BOE Etch Time (seconds)	Ionic Clean	Ionic Clean Etch Time (minutes)
3:1 H_2O_2:H_2SO_4	10	6:1	10	6:1:1 H_2O:H_2O_2:HCl	10

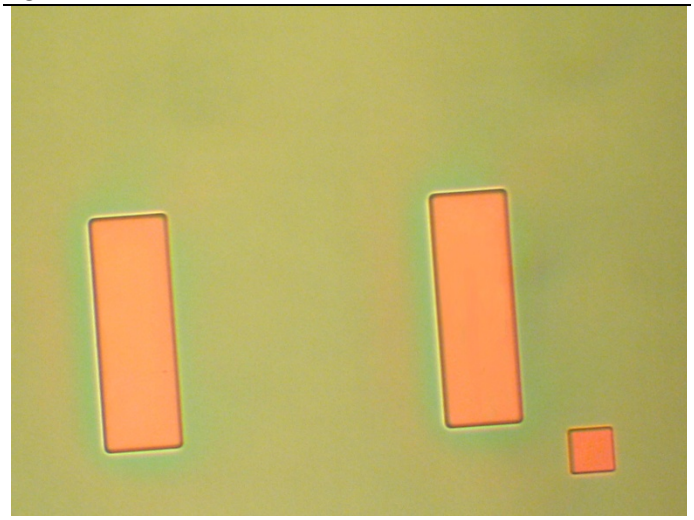
Oxidation Parameters				
Temperature (°C)	Time (minutes)	Type (wet or dry)	N_2/O_2 Flow	Bubbler Setting
1000	90	Wet	7/9	40

Methods:

1. Taking Pictures:

Use the *Optical Microscope* and *CANON Digital Camera* to take pictures of the diffused NMOS sources and drains.

Figure 19 Diffused NMOS sources and drains.



2. Stripping the SiO_2 and PSG:

(Check *Parameters* section for details)

Prepare the wafer surface for the next oxidation by completely removing all the SiO_2 and PSG.

REPEAT: This step should be carried out by the lab TA for safety reasons. Begin by loading the wafers into a *Teflon cassette* with equal spacing between wafers. Using the handle, submerge the cassette in *6:1 BOE* for the appropriate amount of time or until the exposed SiO_2 is completely removed. To determine if the SiO_2 is completely removed, check the regions for color (**see Figure 9**) and hydrophobicity. When the etch is complete, remove the cassette and rinse the wafers in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers with DI water and nitrogen gun.

3. Diffusion Measurements:

Use the *JANDEL 4-point probe* to measure the sheet resistivity of the N+ and N-well diffusions (Refer to **Figure 21** for the location of the diffused areas). Consult the JANDEL 4-point probe manual for further assistance. The measured sheet resistivity of the N+ region should correspond to the value found on the PhosPlus data sheet (**see Figure 20**).

Figure 20 A graph from the PhosPlus datasheet illustrating the relationship between diffusion time, temperature and sheet resistivity.

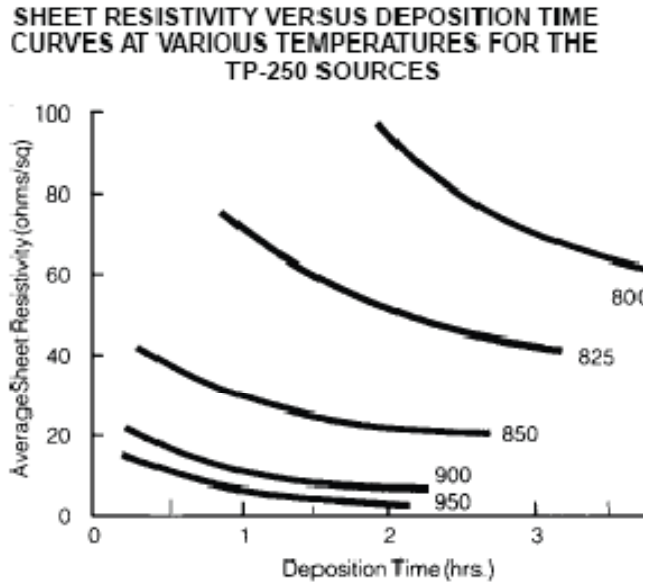
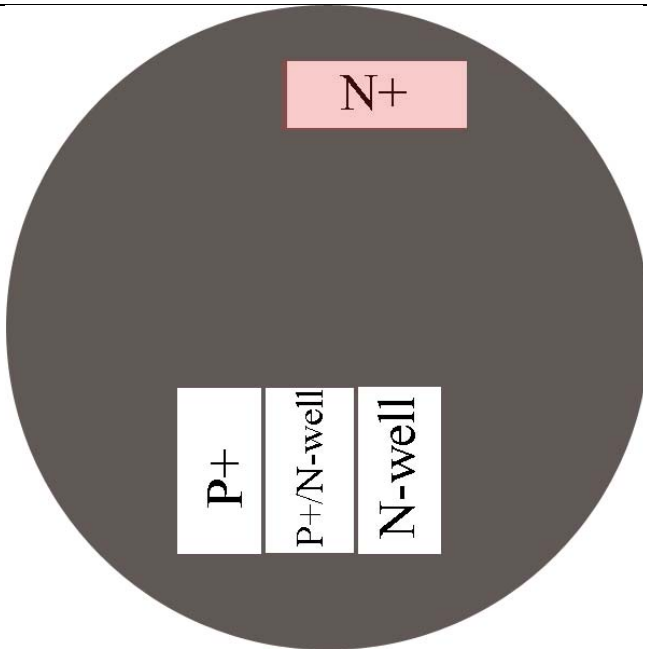


Figure 21 An outline of the wafer diffusion test regions. The area in pink is the freshly diffused N+ region and should be tested with the 4-point probe.



Methods:

4. RCA Cleaning:

(Check *Parameters* section for details)

REPEAT: To remove possible sources of contamination a modified RCA clean is performed. The RCA clean consists of rinsing the wafers in three chemical solutions: Piranha etch, BOE, Ionic clean.

This step should be carried out by the lab TA for safety. Load the wafers into a Teflon cassette transfer the cassette between the RCA solutions until the cleaning is complete. Rinse the wafers and cassette in a bucket of DI water then pull each wafer and rinse and dry by hand.

5. Oxidation: Growing SiO_2

(Check *Parameters* section for details)

The goal of the oxidation run is to grow enough silicon dioxide (SiO_2) roughly a 0.5µm thick film, to mask the subsequent diffusion.

REPEAT: To oxidize, insert the wafers into the *MODULAB oxidation furnace* using the quartz rod and quartz boat (**see Figure 4**). There should be two dummy wafers, one at the front of the boat and another at the rear, to maintain uniformity across the boat. Ramp the furnace to 600°C before the removing the quartz boat and loading the wafers. Prior to the temperature reaching 400°C, turn on the nitrogen to purge the furnace. Also, set the potentiometer on the bubbler if performing a wet oxidation (which we are). Once the wafers are loaded and in place at the center of the furnace, ramp the furnace to the desired temperature. When the desired temperature is reached start the timer, stop the nitrogen flow and turn on the oxygen. After the allotted time, ramp the furnace down to 600°C (or 0°C if finished with furnace), pull the boat, remove the wafers, and set them aside to cool. When the temperature drops below 400°C the nitrogen can be turned off.

RESULTS: Week 7

Sheet Resistance (Ω/□) & Resistivity (Ω-cm):

NOTES/CHANGES:

Photolitho & Etching (P+ Source/Drain) Week 8

GOALS:

1. Measure the thickness of the SiO_2 layer with the Nanospec
2. Photolithography
   (Mask #3 P+ Source/Drain)
3. Hardbake
4. SiO_2 Etch

EQUIPMENT:

- Nanospec
- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- 6:1 BOE
- Teflon Cassette

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5250	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #3)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm^2)	UV Dose (J/cm^2)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Hard-bake Parameters

Hardbake Program	Temperature (°C)	Time (minutes)
#2	115	2

SiO_2 Etch Parameters ** for 4,200-4,500Å thick SiO_2 layer*

BOE concentration	SiO_2 Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5*	Shipley 1813 Photoresist

Methods:

1. Measuring the SiO_2 thickness:

Measure the thickness of the silicon dioxide at several different points on the wafer using the *Nanospec*. For reference, the Nanospec prompts for measuring SiO_2 thickness are:

Is wavelength 480nm?	***Y (if not, type N and value)***
Data bank option?	***N***
Refr index option?	***N***
Switch to printer?	***N***
Enter film type:	***1-SiO2***
Enter obj lens:	***1 = 10x***

2. Photolithography with Mask #3 (P+ S/D): Spin-coating & Soft-baking

(Check *Parameters* section for details)

The third mask contains the features for the PMOS sources and drains.

REPEAT: Begin by using the *BREWER spin-coater* to spin a thin film of *SHIPLEY 1813* photoresist onto the topside of the wafer. Next, transfer the wafer to the adjacent hotplate and soft-bake to remove solvents and harden the resist. A good coating of photoresist will be barely visible to the naked eye and have a minimal number of streaks or blotches (**see Figure 7**). If there are a large number of defects, solvent clean, dehydrate, and try re-spinning more photoresist.

Figure 22 A student using the ABM mask aligner to align Mask #3.

2. Photolithography with Mask #3 (P+ S/D): Exposure & Development

(Check *Parameters* section for details)

Proceed by patterning the photoresist with Mask #3.

REPEAT: Load the mask onto the *ABM contact-aligner* mask stage. Turn the mask-vac on and raise the mask stage. Carefully, load the wafer onto the substrate chuck and orient it such that the <110> plane (wafer flat) is to the left and running straight up and down. Turn on the substrate-vac to lock the wafer in place and lower the chuck to avoid hitting the contact mask. Next, lower the mask stage and raise the substrate chuck up to meet the mask, fringe lines will become visible as the wafer and mask come into contact. Align the mask to the wafer using the markers on the sides of the wafer. Turn on the contact-vac to remove any air gap between mask and wafer. Adjust the exposure time and channel setting then expose. Remove the wafer by turning off the contact-vac, lowering the substrate chuck, raising the mask frame, and turning off the substrate-vac. Transfer the wafer to a dish of *MF319 developer* (a faint outline of the features can be seen at this point), submerge the wafer in MF319 and gently swirl for 30-60 seconds until the exposed resist is completely dissolved. If done correctly there should be no photoresist left in the diffusion contact regions (**see Figure 8**). If there is, resubmerge the wafer in the MF319 developer for additional time. If unsuccessful, use a solvent clean to strip the photoresist, dehydrate and re-spin again. When finished, pour the used MF319 into the MF319 waste container located under the solvent bench next to the photoresist.

Methods:

3. Hard-baking:

(Check *Parameters* section for details)

REPEAT: It has been observed, that without hard-baking, the photoresist exhibits adhesion problems and frequently delaminates from the surface during etching. Hard-baking is very similar to soft-baking and follows the same procedure. Load a wafer onto a hotplate for a set time at the appropriate temperature.

4. Etching the SiO_2:

(Check *Parameters* section for details)

REPEAT: This step should be carried out by the lab TA for safety reasons. Begin by loading the wafers into a *Teflon cassette* with equal spacing between wafers. Using the handle, submerge the cassette in *6:1 BOE* for the appropriate amount of time or until the exposed SiO_2 is completely removed. To determine if the SiO_2 is completely removed, check the regions for color (**see Figure 9**) and hydrophobicity. When the etch is complete, remove the cassette and rinse the wafers in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers with DI water and nitrogen gun.

RESULTS: Week 8

SiO_2 Thickness (Å):

NOTES/CHANGES:

Cleaning & Diffusion (P+) Week 9

GOALS:

1. Full Wafer Clean (Solvent & RCA)
2. Boron Diffusion

EQUIPMENT:

- Acetone, Methanol, Isopropyl
- RCA Tanks
- Boron Diffusion Furnace
- BORONPLUS GS139 Boron Sources

PARAMETERS:

RCA Clean Parameters					
Piranha Solution	Piranha Etch Time (minutes)	BOE solution	BOE Etch Time (seconds)	Ionic Clean	Ionic Clean Etch Time (minutes)
3:1 H_2O_2:H_2SO_4	10	6:1	10	6:1:1 H_2O:H_2O_2:HCl	10

Boron Diffusion Parameters (DIFFUSED CONTACTS)			
Boron Source	Temperature (°C)	Time (minutes)	N_2 Flow
BORONPLUS GS-139	1000	120	7

Drive-in Parameters (DIFFUSED CONTACTS)			
Boron Source	Temperature (°C)	Time (minutes)	N_2 Flow
none	1000	60	7

Methods:

Week 9

1. Wafer Cleaning:

(Check *Parameters* section for details)

The wafers need to be cleaned to remove photoresist, and any possible sources of contamination before being placed in a high temperature furnace.

REPEAT: To remove the photoresist a solvent clean is performed. Begin by placing an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with *acetone* using the squirt bottle, and follow with *methanol* and *isopropyl*. The acetone will remove the photoresist and the methanol and isopropyl with remove any acetone residue. Rinse the wafers in DI water and dry with a nitrogen gun. When finished pour the solvent waste into the *Solvent Waste Container*.

REPEAT: To remove possible sources of contamination a modified RCA clean is performed. This step should be carried out by the lab TA. Load the wafers into a *Teflon cassette* transfer the cassette between the RCA solutions until the cleaning is complete. Rinse the wafers and cassette in a bucket of DI water then pull each wafer and rinse and dry by hand,

6. Boron Diffusion:

(Check *Parameters* section for details)

The goal of the boron diffusion is to create highly doped P-type silicon to act as the sources and drains of the PMOS transistors.

REPEAT: To diffuse P-type (Boron) material, ramp the *Lindberg Blue Boron Diffusion Furnace* to 600°C and set the nitrogen flow. Remove the quartz boat with the solid, white, *BORONPLUS GS-139 sources* already in place. Load the silicon wafers next to the sources with the patterned side facing a source. Insert the quartz boat to the center of the furnace and ramp the furnace to the desired temperature. When the desired temperature is reached start the timer. After the allotted time, ramp the furnace down to 600°C (or 0°C if finished with furnace), pull the quartz boat and remove the wafers and set them aside to cool. When the temperature drops below 400°C the nitrogen can be turned off.

RESULTS:

RESULTS:

NOTES/CHANGES:

Documenting, Cleaning & Oxidation Week 10

GOALS:

1. Take pictures with microscope and camera
2. Strip SiO_2 and BSG
3. 4-point probe
3. RCA clean
4. Dry Oxidation

EQUIPMENT:

- Optical Microscope
- CANON Digital Camera
- JANDEL 4-point probe
- RCA tanks
- MODULAB Oxidation Furnace

PARAMETERS:

SiO_2 Etch Parameters ** for 4,200-4,500Å thick SiO_2 layer*			
BOE concentration	SiO_2 Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5*	Shipley 1813 Photoresist

RCA Clean Parameters					
Piranha Solution	Piranha Etch Time (minutes)	BOE solution	BOE Etch Time (seconds)	Ionic Clean	Ionic Clean Etch Time (minutes)
3:1 H_2O_2:H_2SO_4	10	6:1	10	6:1:1 H_2O:H_2O_2:HCl	10

Oxidation Parameters				
Temperature (°C)	Time (minutes)	Type (wet or dry)	N_2/O_2 Flow	Bubbler Setting
1000	30	**Wet**	7/9	N/A

Oxidation Parameters				
Temperature (°C)	Time (minutes)	Type (wet or dry)	N_2/O_2 Flow	Bubbler Setting
1000	60	**Dry**	7/9	N/A

Methods:

1. Taking Pictures:

Use the *Optical Microscope* and *CANON Digital Camera* to take pictures of the diffused PMOS sources and drains.

Figure 23 Diffused PMOS and NMOS sources and drains.

2. Stripping the SiO_2 and PSG:

(Check *Parameters* section for details)

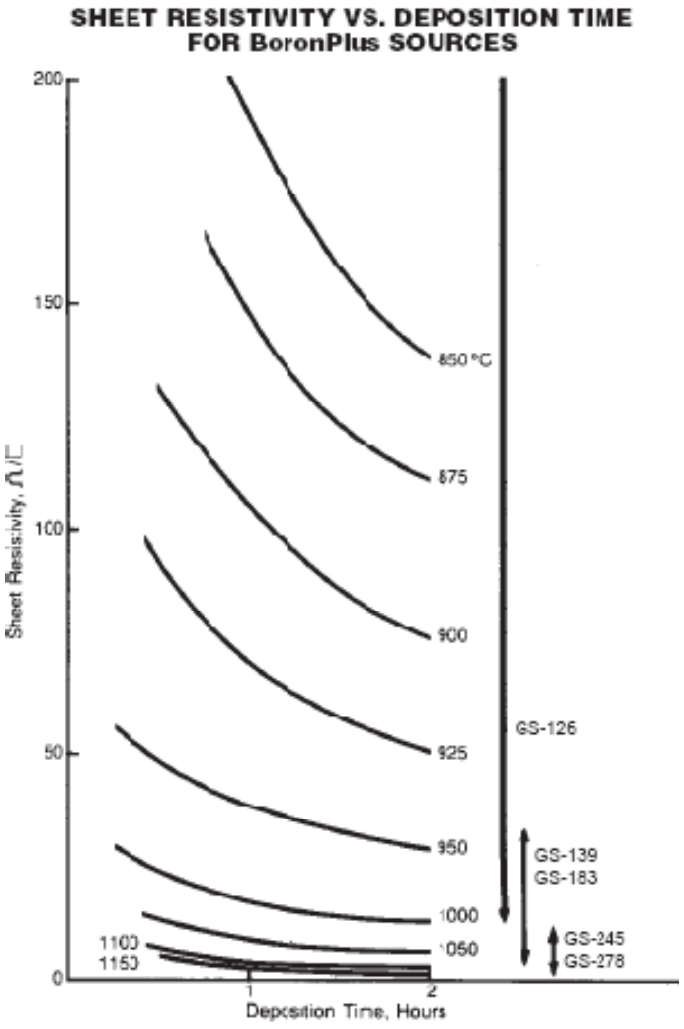
Prepare the wafer surface for the next oxidation by completely removing all the SiO_2 and PSG.

REPEAT: This step should be carried out by the lab TA for safety reasons. Begin by loading the wafers into a *Teflon cassette* with equal spacing between wafers. Using the handle, submerge the cassette in *6:1 BOE* for the appropriate amount of time or until the exposed SiO_2 is completely removed. To determine if the SiO_2 is completely removed, check the regions for color (**see Figure 9**) and hydrophobicity. When the etch is complete, remove the cassette and rinse the wafers in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers with DI water and nitrogen gun.

3. Diffusion Measurements:

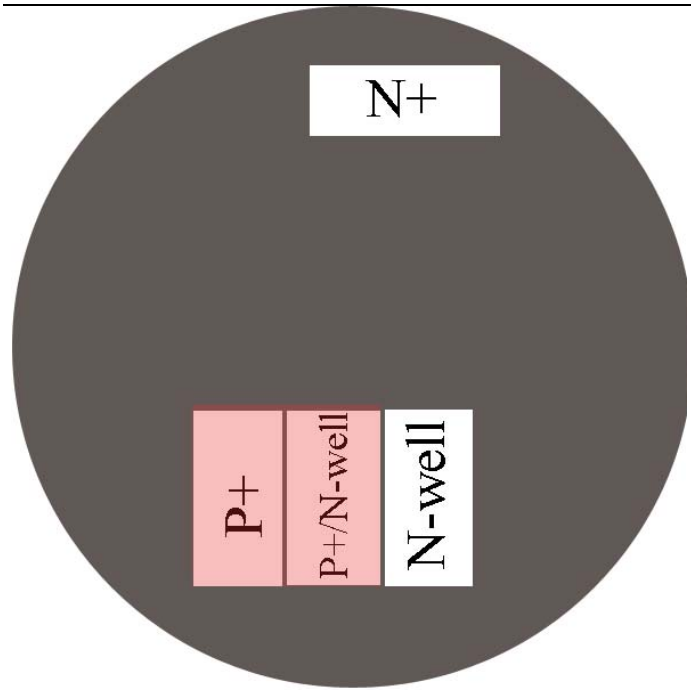
Use the 4-point probe to measure the sheet resistivity of the P+, N+ and N-well diffusions (Refer to **Figure 25** for the location of the diffused areas). Consult the JANDEL 4-point probe manual for further assistance. The measured sheet resistivity of the P+ region should correspond to the value found on the BoronPlus data sheet (**see Figure 24**).

Figure 24 Graph from the BoronPlus data sheet.



Methods:

Figure 25 An outline of the wafer diffusion test regions. The area in pink is diffused as P+. Test each area with the 4-point probe and record the final sheet resistivities.



4. RCA Cleaning:

(Check *Parameters* section for details)

REPEAT: To remove possible sources of contamination a modified RCA clean is performed. The RCA clean consists of rinsing the wafers in three chemical solutions: Piranha etch, BOE, Ionic clean.

This step should be carried out by the lab TA for safety. Load the wafers into a Teflon cassette transfer the cassette between the RCA solutions until the cleaning is complete. Rinse the wafers and cassette in a bucket of DI water then pull each wafer and rinse and dry by hand.

5. Dry Oxidation: Growing SiO_2

(Check *Parameters* section for details)

The goal of the fourth oxidation run is to grow the gate oxide. The oxide thickness should be approximately 700Å thick. The method of oxidation differs from the previous runs, the oxide will be grown with dry O_2.

REPEAT: To oxidize, insert the wafers into oxidation furnace using the quartz rod and quartz boat. There should be two dummy wafers, one at the front of the boat and another at the rear, to maintain uniformity across the boat. Ramp the furnace to 600°C before the removing the quartz boat and loading the wafers. Prior to the temperature reaching 400°C, turn on the nitrogen to purge the furnace. Load the wafers and insert the quartz boat to the center of the furnace and ramp the furnace to the desired temperature. When the desired temperature is reached start the timer, stop the nitrogen flow and turn on the oxygen. After the allotted time, ramp the furnace down to 600°C (or 0°C if finished with furnace), pull the boat, remove the wafers, and set them aside to cool.

RESULTS: Week 10

Sheet Resistance (Ω/□) & Resistivity (Ω-cm):

NOTES/CHANGES: A short wet oxidation was added along with another masking step. The gate oxide mask (GOX) removes the field oxide where the gate oxide is to be grown and generates the alignment marks for the contact mask. In the past this step was removed to expedite the process so that it could be finished by the end of the term. We now start on Week #2 with the substrates already oxidized to allow for the extra processing steps now.

Photolithography & Etching (Vias) Week 11

GOALS:

1. Measure the thickness of the SiO_2 layer with the Nanospec
2. Photolithography (Mask #4 Vias)
3. Hardbake
4. SiO_2 Etch

EQUIPMENT:

- Nanospec
- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- 6:1 BOE
- Teflon Cassette

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5250	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #4)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm^2)	UV Dose (J/cm^2)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Hard-bake Parameters

Hardbake Program	Temperature (°C)	Time (minutes)
#2	115	2

SiO_2 Etch Parameters ** for 4,200-4,500Å thick SiO_2 layer*

BOE concentration	SiO_2 Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5*	Shipley 1813 Photoresist

Methods:

1. Measuring the SiO_2 thickness:

Measure the thickness of the silicon dioxide at several different points on the wafer using the *Nanospec*. For reference, the Nanospec prompts for measuring SiO_2 thickness are:

Is wavelength 480nm?	***Y (if not, type N and value)***
Data bank option?	***N***
Refr index option?	***N***
Switch to printer?	***N***
Enter film type:	***1-SiO2***
Enter obj lens:	***1 = 10x***

2. Photolithography with Mask #4 (Vias): Spin-coating & Soft-baking

(Check *Parameters* section for details)

The fourth mask contains the features of the via etch. The vias are holes in the SiO_2 which allow the aluminum pads to contact the diffused silicon surface.

REPEAT: Begin by using the *BREWER spin-coater* to spin a thin film of *SHIPLEY 1813* photoresist onto the topside of the wafer. Next, transfer the wafer to the adjacent hotplate and soft-bake to remove solvents and harden the resist. A good coating of photoresist will be barely visible to the naked eye and have a minimal number of streaks or blotches (**see Figure 7**). If there are a large number of defects, solvent clean, dehydrate, and try re-spinning more photoresist.

2. Photolithography with Mask #4 (Vias): Exposure & Development

(Check *Parameters* section for details)

Proceed by patterning the photoresist with Mask #4.

REPEAT: Load the mask onto the *ABM contact-aligner* mask stage. Turn the mask-vac on and raise the mask stage. Carefully, load the wafer onto the substrate chuck and orient it such that the <110> plane (wafer flat) is to the left and running straight up and down. Turn on the substrate-vac to lock the wafer in place and lower the chuck to avoid hitting the contact mask. Next, lower the mask stage and raise the substrate chuck up to meet the mask, fringe lines will become visible as the wafer and mask come into contact. Align the mask to the wafer using the markers on the sides of the wafer. Turn on the contact-vac to remove any air gap between mask and wafer. Adjust the exposure time and channel setting then expose. Remove the wafer by turning off the contact-vac, lowering the substrate chuck, raising the mask frame, and turning off the substrate-vac. Transfer the wafer to a dish of *MF319 developer* (a faint outline of the features can be seen at this point), submerge the wafer in MF319 and gently swirl for 30-60 seconds until the exposed resist is completely dissolved. If done correctly there should be no photoresist left in the diffusion contact regions (**see Figure 8**). If there is, resubmerge the wafer in the MF319 developer for additional time. If unsuccessful, use a solvent clean to strip the photoresist, dehydrate and re-spin again. When finished, pour the used MF319 into the MF319 waste container located under the solvent bench next to the photoresist.

Methods:

3. Hard-baking:

(Check *Parameters* section for details)

REPEAT: It has been observed, that without hard-baking, the photoresist exhibits adhesion problems and frequently delaminates from the surface during etching. Hard-baking is very similar to soft-baking and follows the same procedure. Load a wafer onto a hotplate for a set time at the appropriate temperature.

4. Etching the SiO_2:

(Check *Parameters* section for details)

REPEAT: This step should be carried out by the lab TA for safety reasons. Begin by loading the wafers into a *Teflon cassette* with equal spacing between wafers. Using the handle, submerge the cassette in *6:1 BOE* for the appropriate amount of time or until the exposed SiO_2 is completely removed. To determine if the SiO_2 is completely removed, check the regions for color (**see Figure 9**) and hydrophobicity. When the etch is complete, remove the cassette and rinse the wafers in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers with DI water and nitrogen gun.

RESULTS: Week 11

SiO_2 Thickness (Å):

NOTES/CHANGES:

Cleaning & Aluminum Evaporation Week 12

GOALS:

1. Take pictures with microscope and camera
2. Solvent Clean
3. Aluminum PVD

EQUIPMENT:

- Acetone, Methanol, Isopropyl
- MODULAB Physical Vapor Deposition system

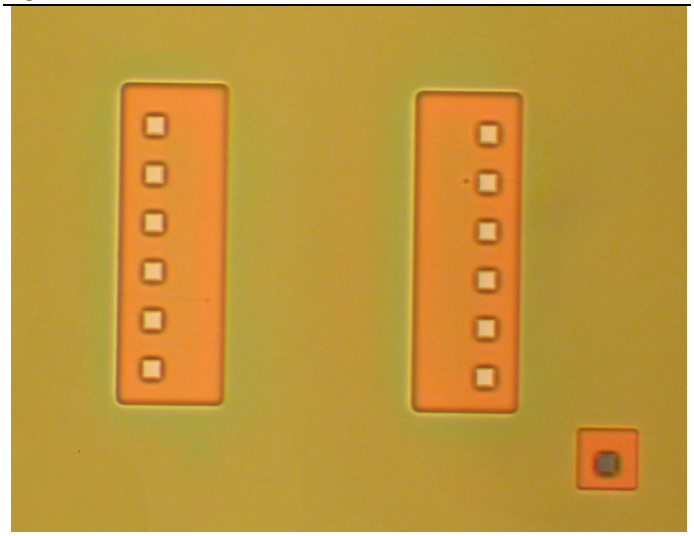
PARAMETERS:

Methods:

1. Taking Pictures:

Use the *Optical Microscope* and *CANON Digital Camera* to take pictures of the diffused PMOS sources and drains.

Figure 26 Etched vias above a NMOS source and drain.



2. Solvent Clean:

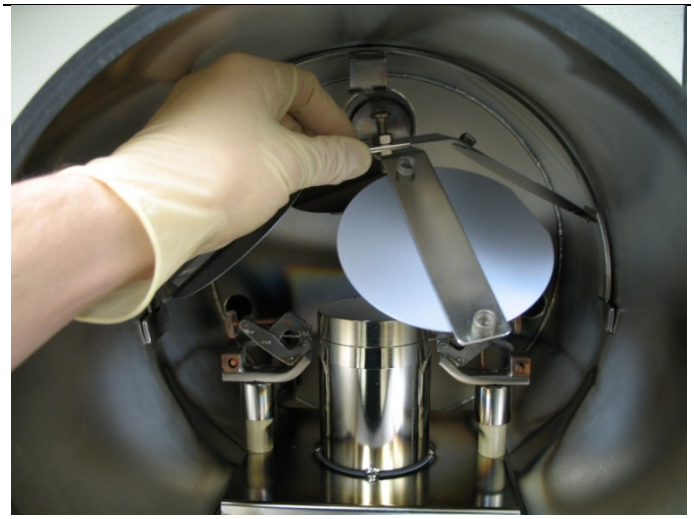
REPEAT: To remove the photoresist a solvent clean is performed. Begin by placing an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with *acetone* using the squirt bottle, and follow with *methanol* and *isopropyl.* Rinse the wafers in DI water and dry with a nitrogen gun. When finished pour the solvent waste into the *S*olvent Waste Container.

3. Aluminum PVD:

The goal of the aluminum evaporation is to create a thin film of aluminum on the topside of the wafer. The aluminum will be patterned with Mask #5 to create electrical contact pads for characterizing the finished devices. The evaporation is accomplished with the *MODULAB PVD system*. See the *MODULAB PVD* operations manual for more information.

Approximately 40-50 cm^2 of aluminum should be evaporated. This will provide roughly 0.5-0.7µm of aluminum on the wafer surface.

Figure 27 Completed Type-2 piezoresistors.



RESULTS: Week 12

Results:

NOTES/CHANGES:

Photolitho, Etch (Pads) & Document Week 13

GOALS:

1. Photolithography (Mask #5 Contact Pads)
2. Aluminum Etch
3. Solvent Clean
4. Anneal
5. Measure aluminum thickness with profilometer
6. Take pictures with microscope and camera

EQUIPMENT:

- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- PAE Etchant
- Acetone, Methanol, Isopropyl
- AMBIOS Profilometer
- Optical Microscope
- CANON Digital Camera

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5250	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #1)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm^2)	UV Dose (J/cm^2)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Hard-bake Parameters

Hardbake Program	Temperature (°C)	Time (minutes)
#2	115	2

Aluminum Etch Parameters ** for 0.5-1um thick aluminum layer*

Etchant	Approx. Etch Rate (Å /min)	Approx. Etch Time (minutes)	Etch Mask
PAE	350	15*	Shipley 1813 Photoresist

Anneal Parameters

Furnace	Temperature (°C)	N_2 Flow	Time (min)
Boron Diffusion Furnace	450	7	45

Methods:

1. Photolithography with Mask #5

(Contact Pads):

Spin-coating & Soft-baking

(Check *Parameters* section for details)

The fifth mask contains the features for the aluminum contact pads.

REPEAT: Begin by using the *BREWER spin-coater* to spin a thin film of *SHIPLEY 1813* photoresist onto the topside of the wafer. Next, transfer the wafer to the adjacent hotplate and soft-bake to remove solvents and harden the resist. A good coating of photoresist will be barely visible to the naked eye and have a minimal number of streaks or blotches (**see Figure 7**). If there are a large number of defects, solvent clean, dehydrate, and try re-spinning more photoresist.

1. Photolithography with Mask #5

(Contact Pads):

Exposure & Development

(Check *Parameters* section for details)

Proceed by patterning the photoresist with Mask #5.

REPEAT: Load the mask onto the *ABM contact-aligner* mask stage. Turn the mask-vac on and raise the mask stage. Carefully, load the wafer onto the substrate chuck and orient it such that the <110> plane (wafer flat) is to the left and running straight up and down. Turn on the substrate-vac to lock the wafer in place and lower the chuck to avoid hitting the contact mask. Next, lower the mask stage and raise the substrate chuck up to meet the mask, fringe lines will become visible as the wafer and mask come into contact. Align the mask to the wafer using the markers on the sides of the wafer. Turn on the contact-vac to remove any air gap between mask and wafer. Adjust the exposure time and channel setting then expose. Remove the wafer by turning off the contact-vac, lowering the substrate chuck, raising the mask frame, and turning off the substrate-vac. Transfer the wafer to a dish of *MF319 developer* (a faint outline of the features can be seen at this point), submerge the wafer in MF319 and gently swirl for 30-60 seconds until the exposed resist is completely dissolved. If done correctly there should be no photoresist left in the diffusion contact regions (**see Figure 8**). If there is, resubmerge the wafer in the MF319 developer for additional time. If unsuccessful, use a solvent clean to strip the photoresist, dehydrate and re-spin again. When finished, pour the used MF319 into the MF319 waste container located under the solvent bench next to the photoresist.

Methods:

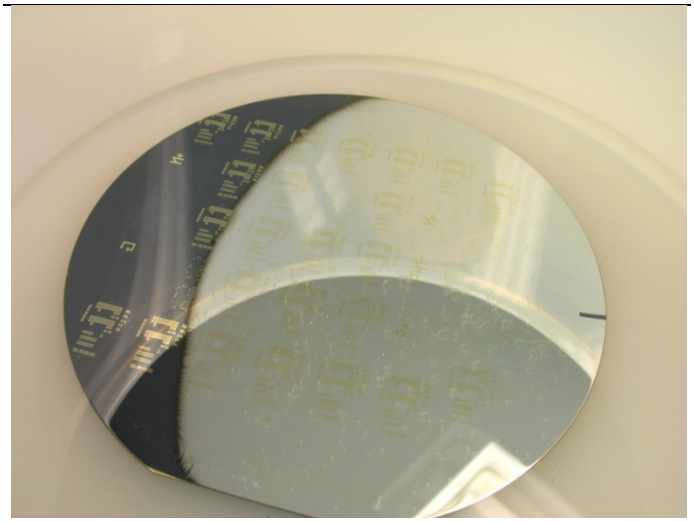
2. Etching Aluminum:

(Check *Parameters* section for details)

The exposed aluminum is removed in PAE (Phosphoric Acid Etch) one wafer at a time. The PAE contains three acids: phosphoric, acetic, and nitric. It etches aluminum at approximately 350Å/min and is highly selective to aluminum compared to photoresist.

Begin by pouring a small amount of PAE into a pyrex or Teflon evaporating dish. Submerge a wafer and gently swirl until the exposed aluminum has been etched. A visible etch front will move across the wafer as the aluminum is removed (see Figure 24). The etch will take between 10-15 minutes to complete.

Figure 28 Aluminum being etched in PAE. Note the etch front moving from left to right. This is a result of a varying thickness in the aluminum created during the evaporation.



3. Solvent Clean:

REPEAT: To remove the photoresist a solvent clean is performed. Begin by placing an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with acetone using the squirt bottle, and follow with methanol and isopropyl. Rinse the wafers in DI water and dry with a nitrogen gun. When finished pour the solvent waste into the *Solvent Waste Container*.

4. Annealing:

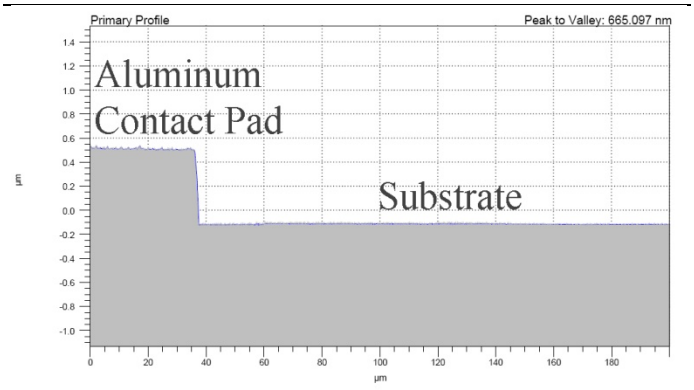
The goal of the anneal is to improve the junction between the silicon and aluminum. Before the anneal, the junction is highly resistive and inhibits the effectiveness of the devices. Afterward, the junction is more conductive and creates a more stable sensor.

To anneal, place wafers into the quartz boat (away from the diffusion sources) and insert into the heated furnace. Leave for the desired time, then remove and allow wafers to cool.

5. Aluminum Thickness Measurements:

Measure the thickness of the patterned aluminum film with the *AMBIOS Stylus Profilometer.* Begin by loading a wafer onto the stage. Using the XP2 software move the stage and wafer beneath the stylus. Adjust the stylus height and stage position over a patterned feature. Scan the feature with an appropriate scan length, speed, and force. Consult the AMBIOS operations manual for more details. The results should resemble the following figure, **Figure 29**.

Figure 29 Profilometer data of an aluminum pad. The data reveals the thickness of the aluminum film.

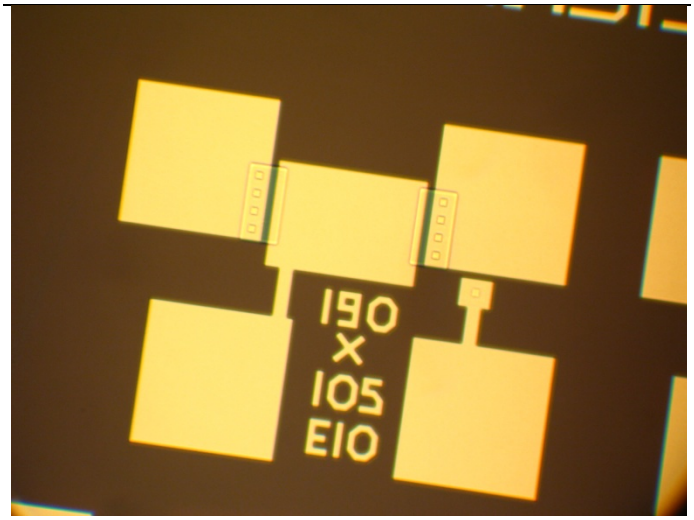


Methods:

6. Taking Pictures:

Use the *Optical Microscope* and *CANON Digital Camera* to take pictures of the finished PMOS and NMOS devices. Take pictures of the test structures as well.

Figure 30 Completed NMOS transistors with patterned aluminum contact pads.



RESULTS: Week 13

Aluminum Thickness (µm):

NOTES/CHANGES:

Probe & Test! Week 14

GOALS:

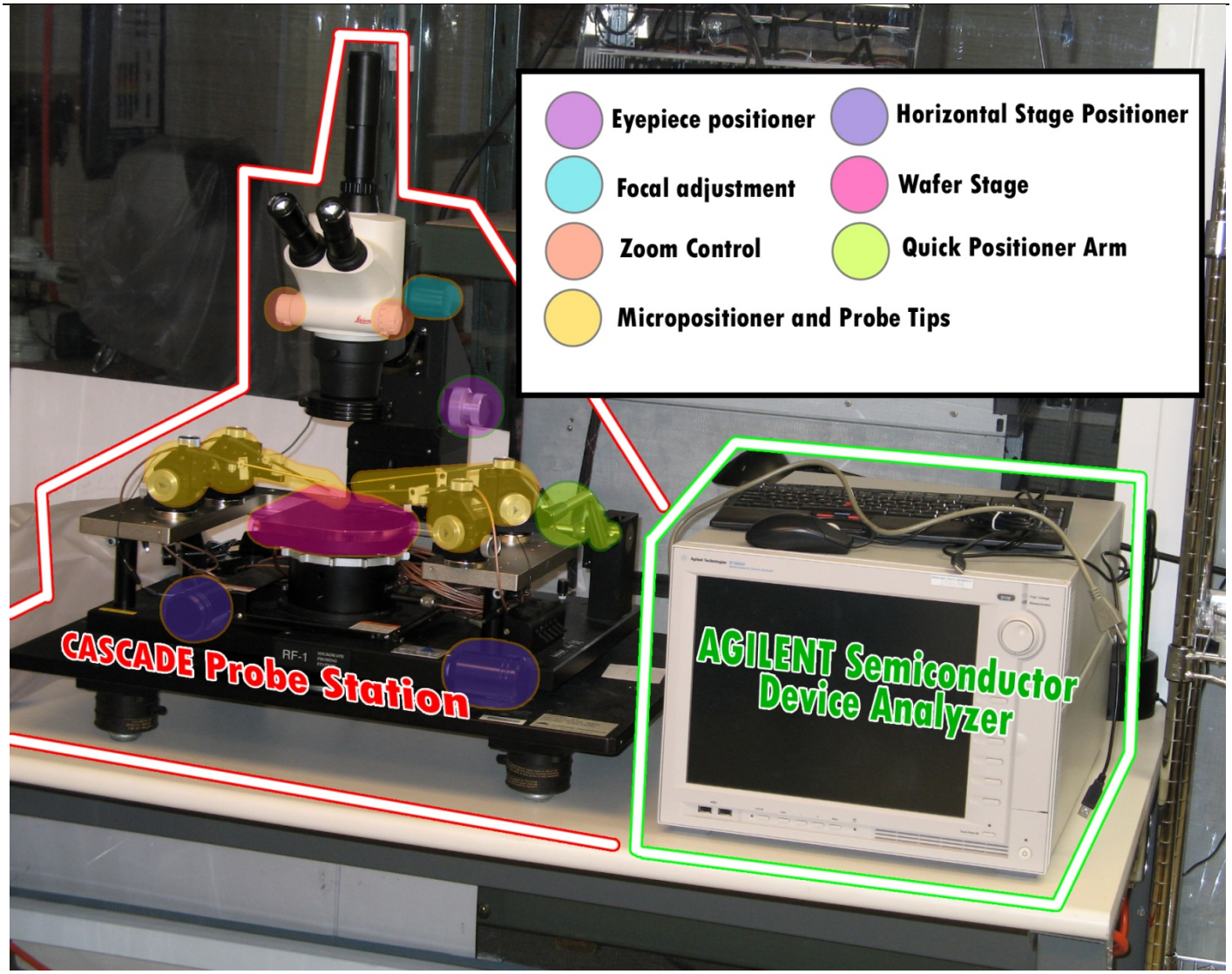
1. Characterize and test as many devices as possible

EQUIPMENT:

- Wafer Scribe
- CASCADE probe station
- DMM
- Oscilloscope
- AGILENT Semiconductor Device Analyzer

PARAMETERS:

Figure 31 Overview of the probe station.



Methods:

1. Testing:

Devices are tested and characterized with the *CASCADE probe station* and *AGILENT Semiconductor Device Analyzer* (**see Figure 31**). The first devices to be tested should be the resistors. (Refer to the *Die Layout* Section at the end of the document for details on where the devices are located) Setup the Resistor Test program on the device analyzer (**see Figure 37**). Place the wafer on the wafer stage and adjust the probe and stage position so that the probe tips are aligned over the two aluminum pads of a resistor (**see Figure 36**). Ensure the probes correspond to the correct ports numbers on the device analyzer and press the "run" button. The results should resemble the following graph (**Figure 38**). If the results are poor or indicate the device is not functioning properly, re-test other devices on different dies around the wafer.

After all varieties of resistors are tested, continue by characterizing the diodes, NMOS and PMOS devices. The appropriate testing interfaces need to be recalled from the device analyzer, and in the case of the transistors all four probes need to be used for the source, drain, gate, and substrate (optional). The following figures (**Figure 39-43**) show the testing interface and results from functional devices. The tests should be performed on devices through the wafer. The transistor tests should also be performed on various NMOS and PMOS devices with different channel lengths and widths to determine the smallest functional device.

Figure 34 Completed wafer.

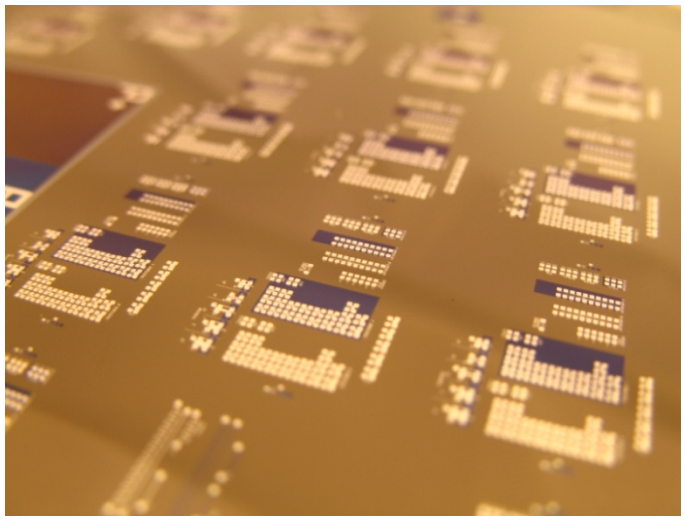


Figure 32 A student using the CASCADE probe station and AGILENT device analyzer to test CMOS devices,

Figure 33 Microprobes at the CASCADE probe station.

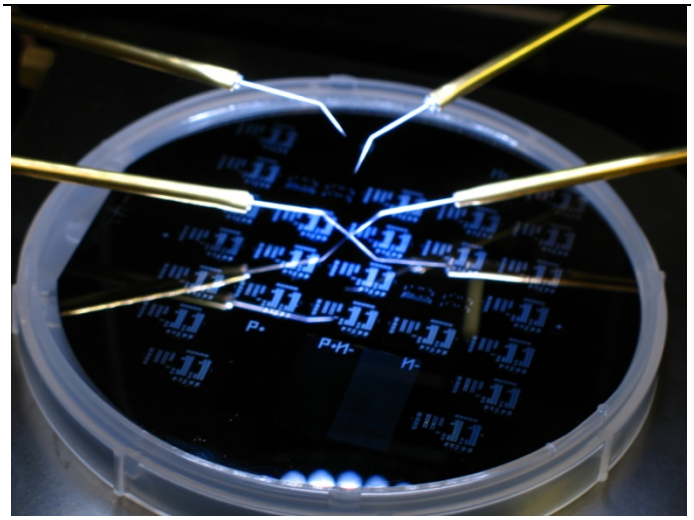
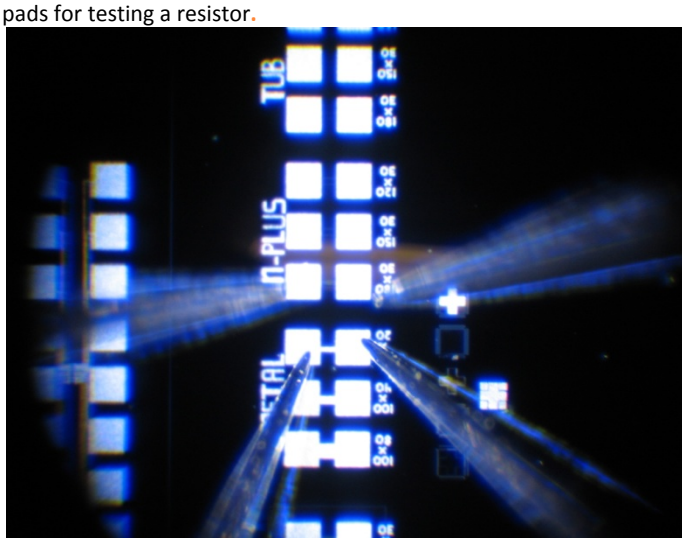


Figure 36 Camera image from the CASCADE probe station. The bottom two probe tips are positioned onto the aluminum contact pads for testing a resistor.



Methods:

Figure 37 Screen capture from the AGILENT Semiconductor Device Analyzer showing the resistor test setup.

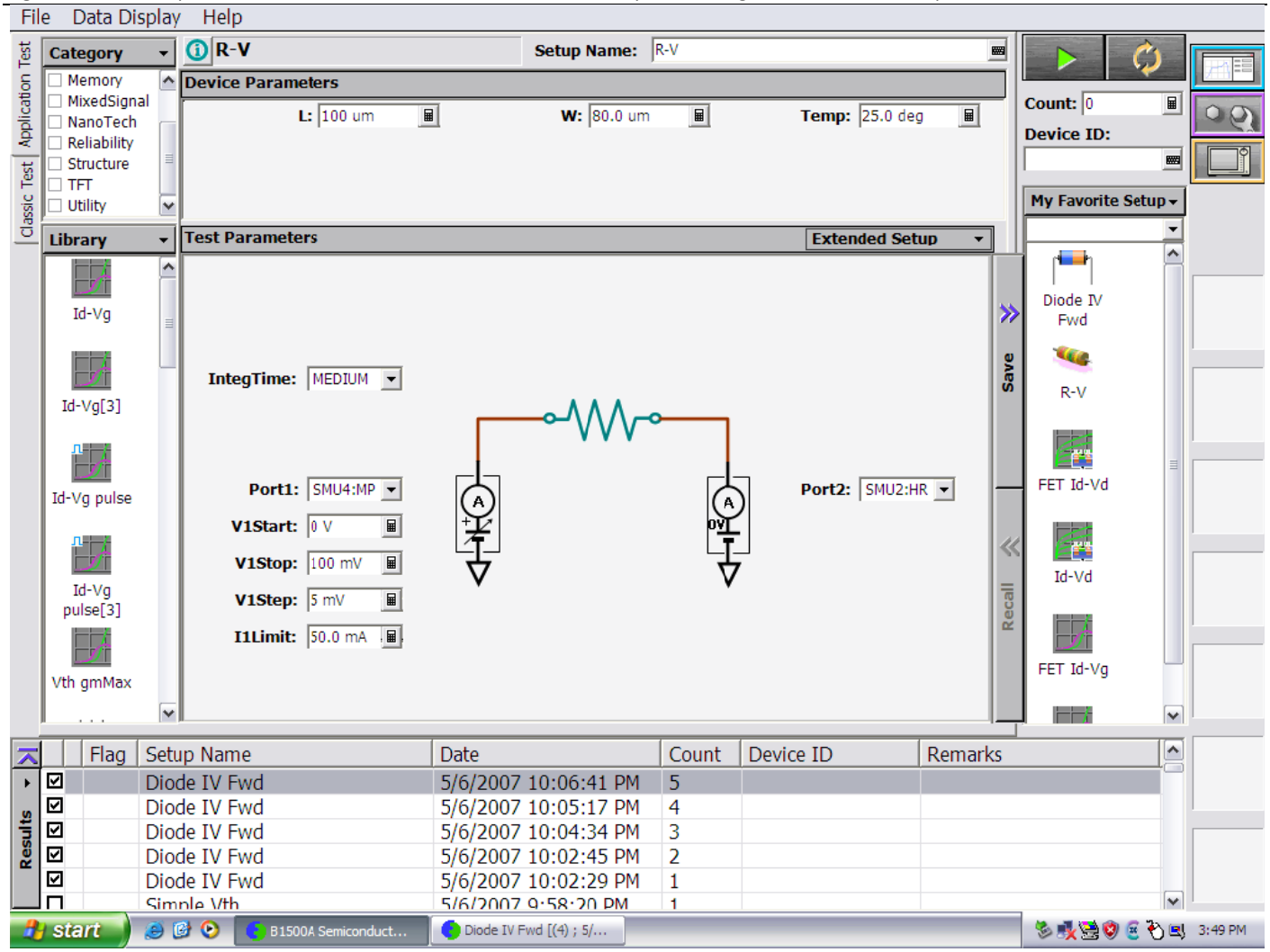
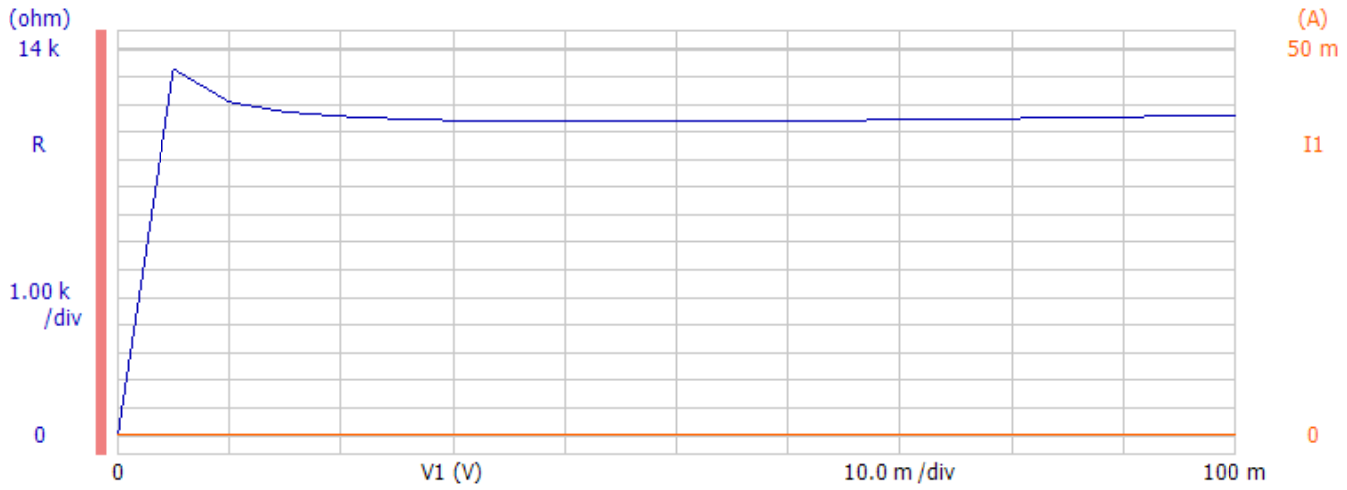


Figure 38 Result from testing a diffused resistor. The program ramps the voltage across the probes and measures the current. The graph displays the resistance as a function of voltage, the approximate resistance is 11.5kΩ.



Methods:

Figure 39 Screen capture from the AGILENT Semiconductor Device Analyzer showing the diode test setup.

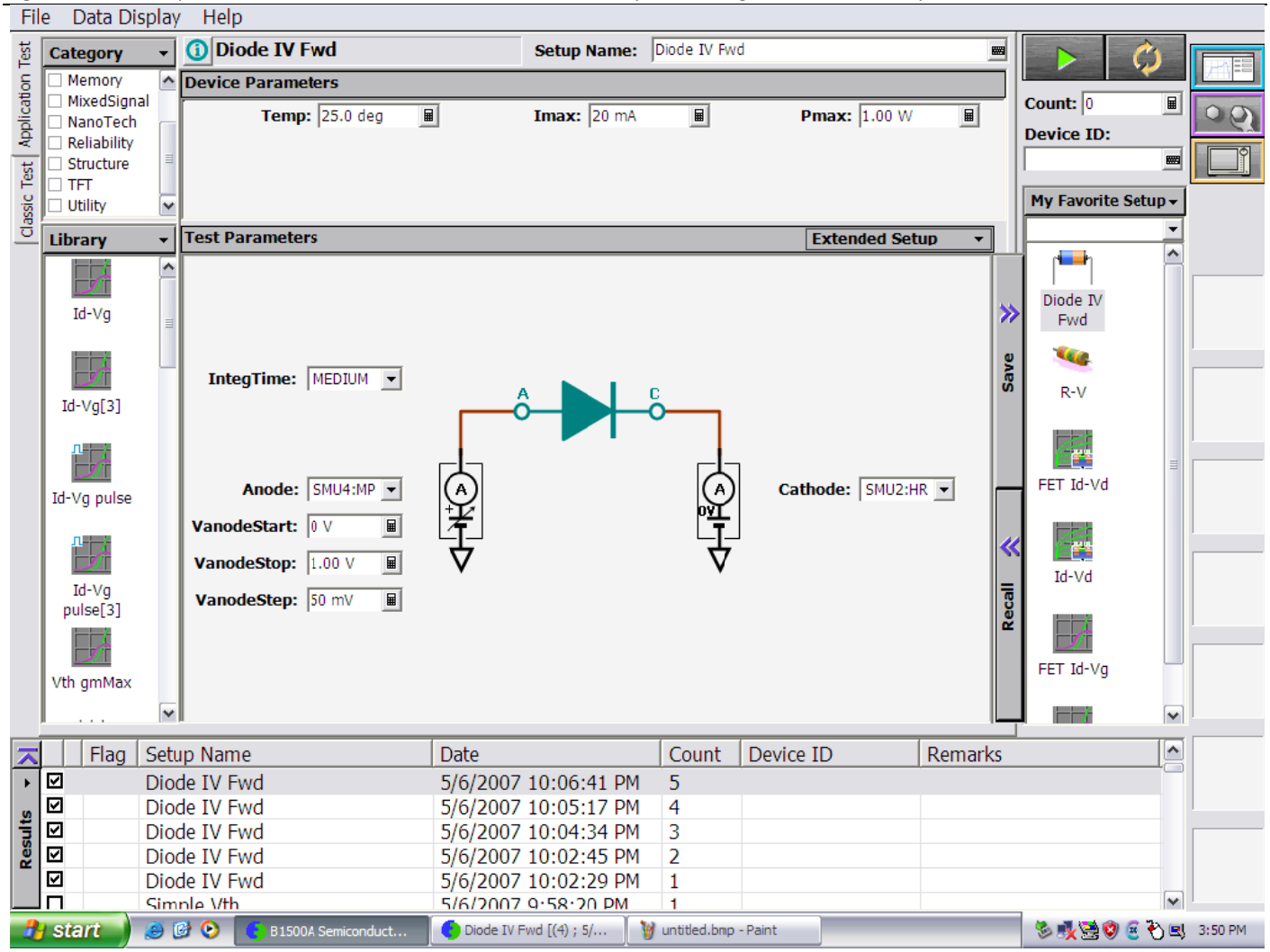
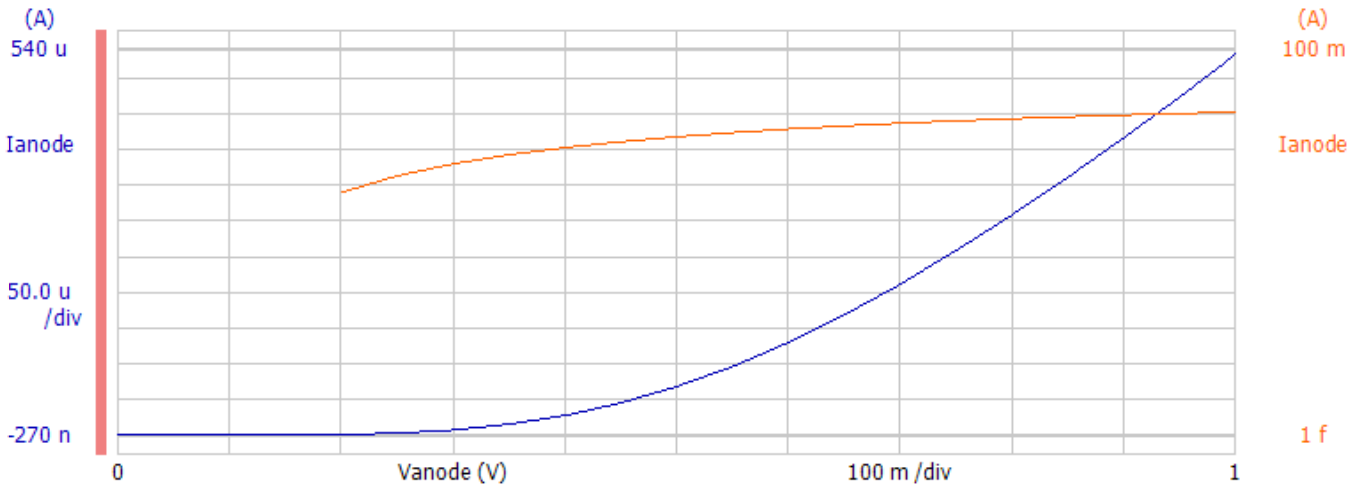


Figure 40 Result from testing a diffused PN diode. The graph illustrates the exponential behavior of the current through a diode.



Methods:

Figure 41 Screen capture from the AGILENT Semiconductor Device Analyzer showing the transistor test setup to achieve an Id vs Vd curve. Note the "FET Id-Vd" test setup uses only three probes. Also note that under the *Device Parameters* section the "Polarity" is labeled as Nch for a NMOS transistor.

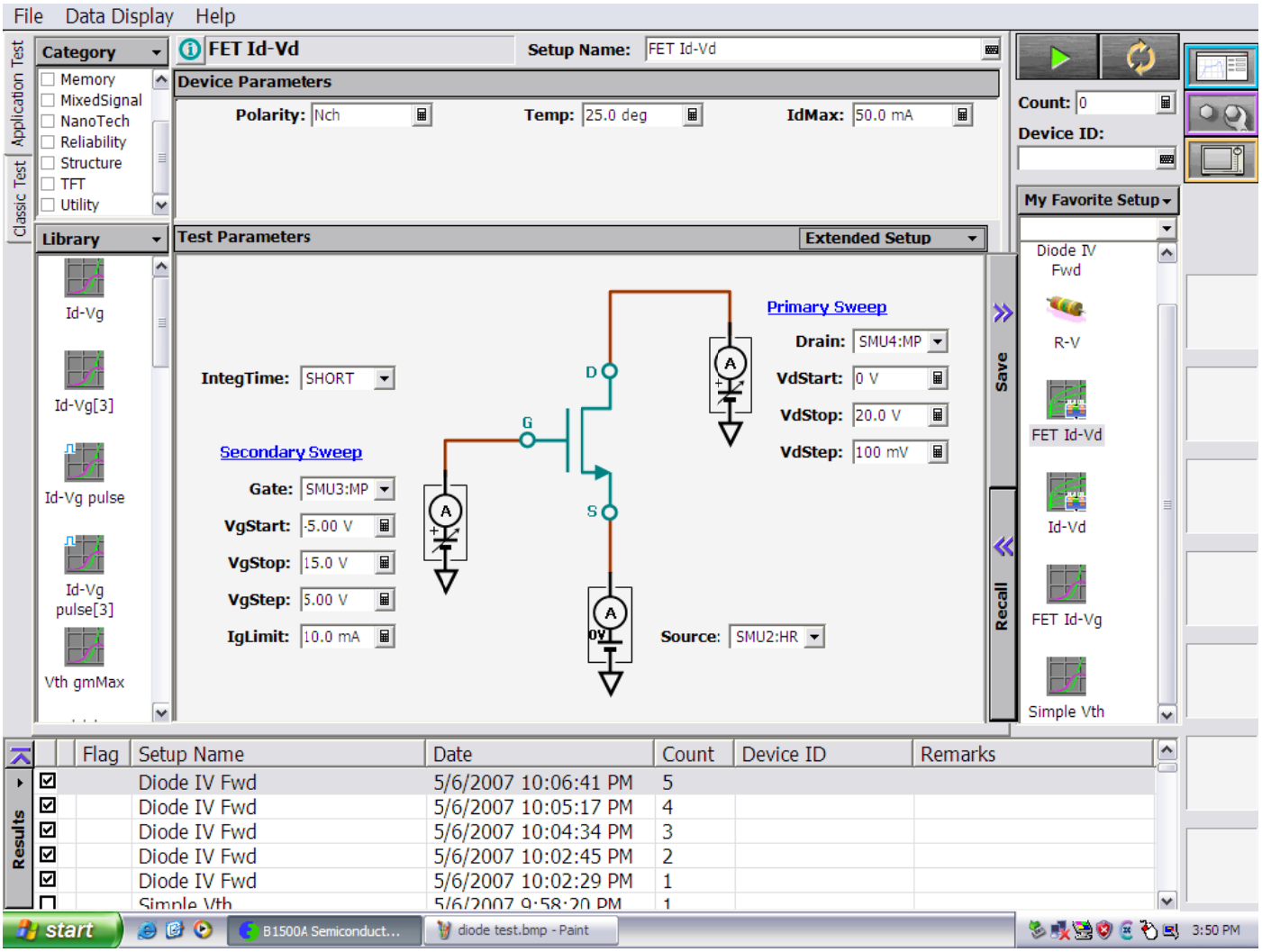
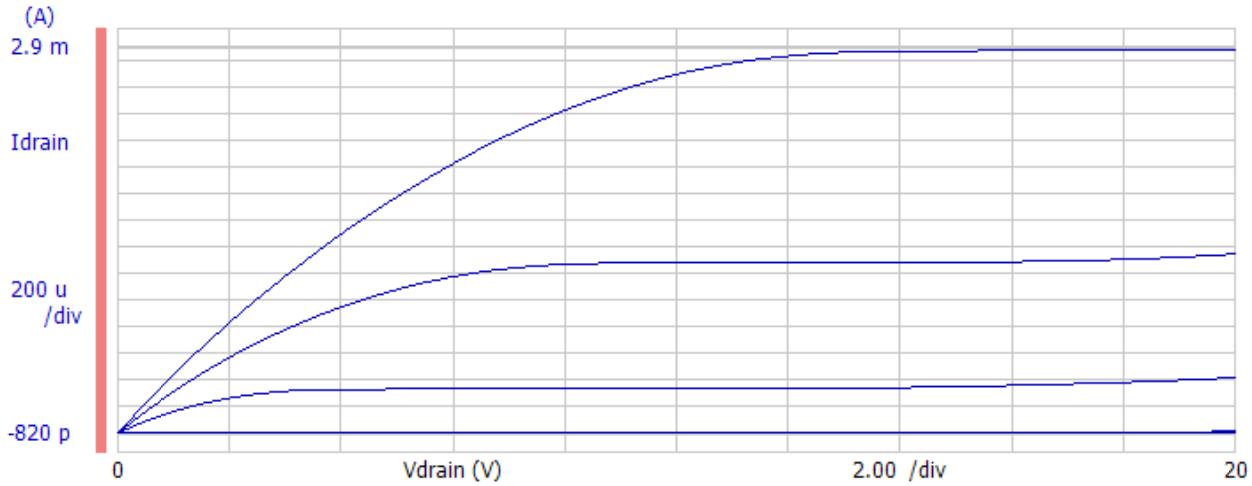
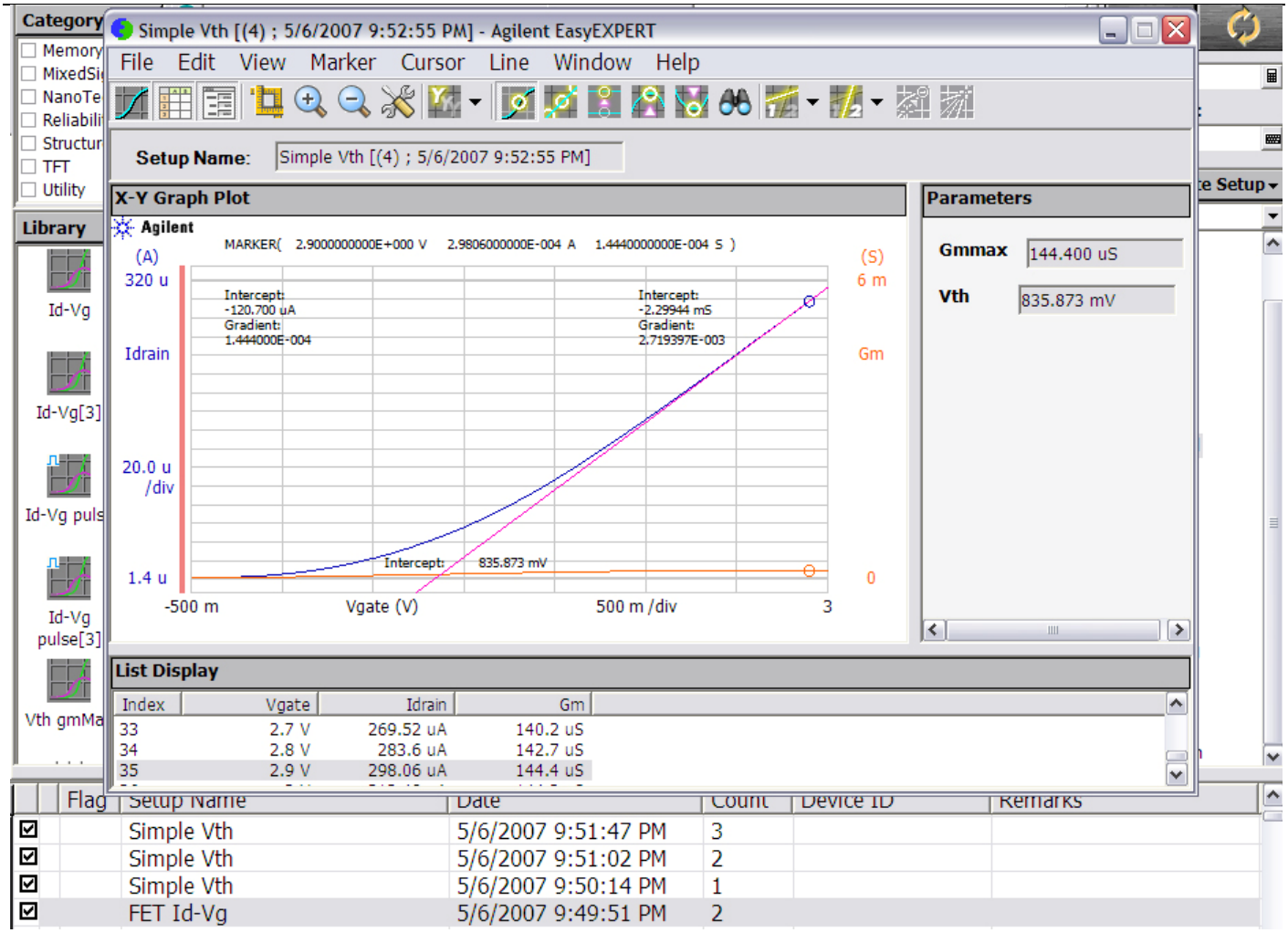


Figure 42 The result of the FET Id-Vd test. Note the characteristic triode-saturation shape of the curves as drain and gate voltages are ramped. A breakdown of the in the saturation region can also be seen from the graph by the upward curve at the large drain voltages.



Methods:

Figure 43 Screen capture from the AGILENT Semiconductor Device Analyzer showing the results of a "Simple Vth" test. While there is another similar test labeled "FET Id-Vg," the Simple Vth test will reveal an approximate value of the threshold voltage for the transistor. In this case the results indicate the device has a threshold voltage of 0.836V.



RESULTS: Week 14

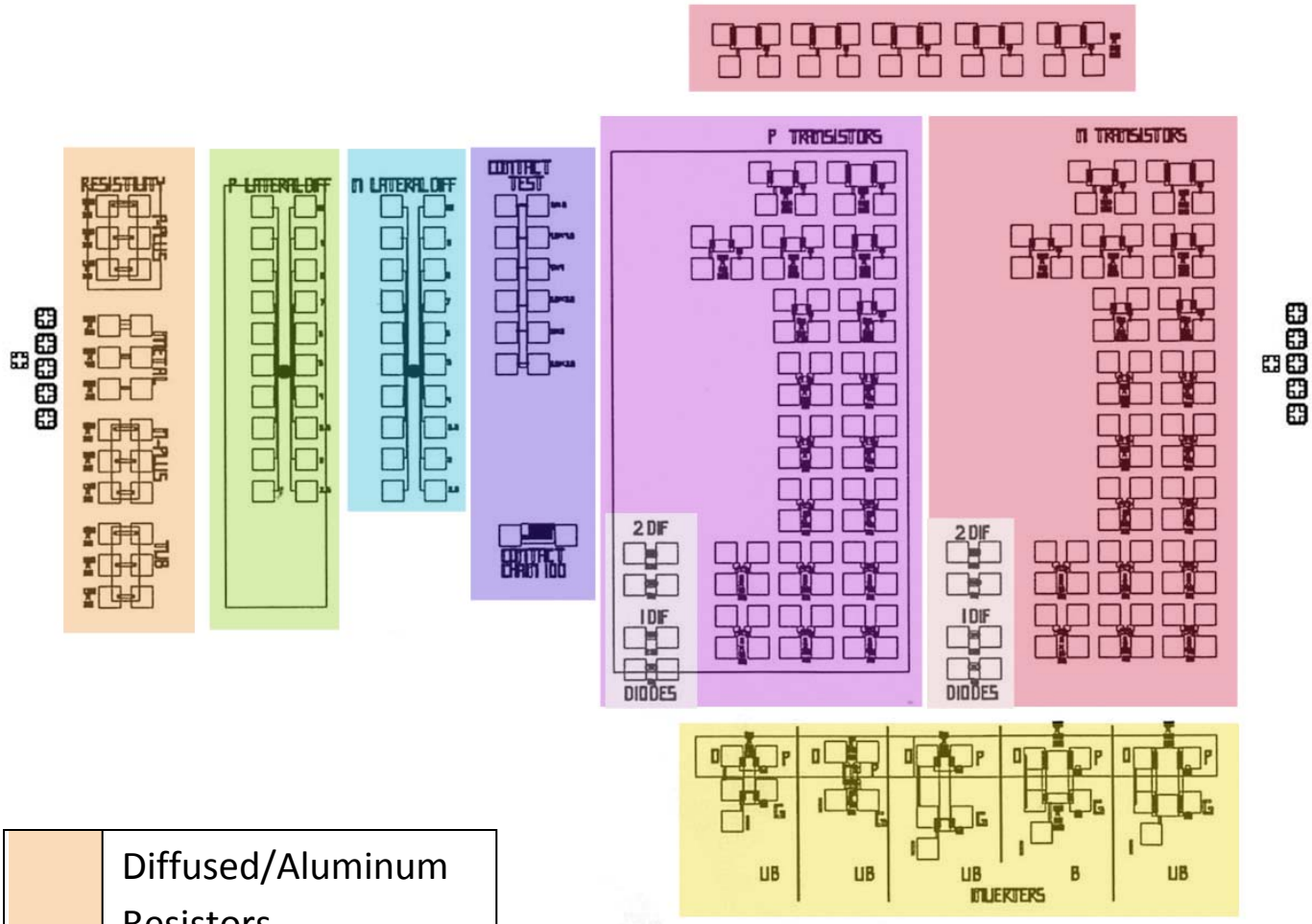
Results:

NOTES/CHANGES:

Die Layout

The following image is of a single die. Each die contains both NMOS and PMOS devices as well as a number of test structures. The NMOS and PMOS transistors are oriented such that the larger channels (both length and width) are at the top of the segment. At the bottom, near the diodes are the smaller channel transistor devices.

Layout:



	Diffused/Aluminum Resistors		
	Test structure: Lateral Diffusion P+		PMOS Transistors/Diodes: Varying channel lengths and widths.
	Test structure: Lateral Diffusion N+		NMOS Transistors/Diodes: Varying channel lengths and widths.
	Test structure: Contacts/Contact chain		CMOS Inverters: Includes NMOS and PMOS devices with different W/L ratios.