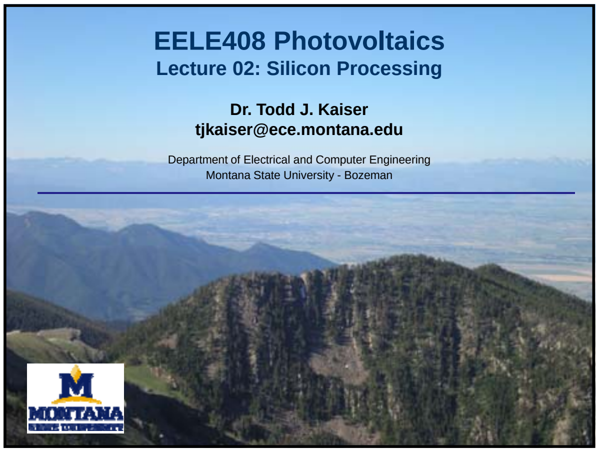

EELE408 Photovoltaics

Lecture 02: Silicon Processing

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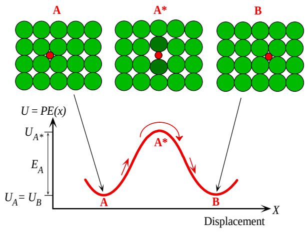
The Fabrication Process

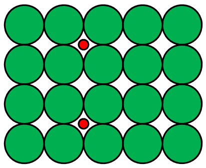
- Thermally Activated Processes
  - Diffusion
    - Dopes the silicon to make it more conductive
    - $2B_2O_3 + 3Si \rightarrow 4B + 3SiO_2$
    - $2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2$
  - Oxidation
    - Forms a glass insulating layer that can be used as a masking layer
- Photolithography
  - Transfers pattern to layers
    - Photoresist
    - Mask Alignment
    - Development
- Etching
  - Removes material that is not protected by masking layer
- Physical Vapor Deposition (PVD)
  - Deposits a thin layer of metal

Thermally Activated Processes

- Thermal energy required to initiate process.
- Diffusion
  - Interstitial impurity atoms move in lattice



Thermally Activated Process

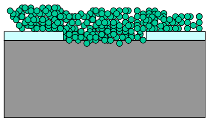


Energy below the activation energy

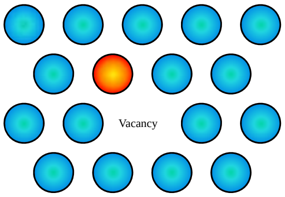
Energy above the activation energy

Diffusion

- Movement of particles from high concentration to low concentration
- Mass transport within solids by step-wise atomic motion
- Thermal energy drives reaction

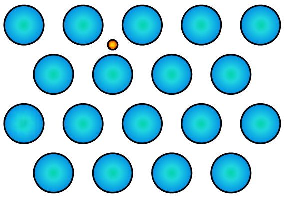


Vacancy Diffusion



- Requires vacancies (defects)
- Rate a function of the number of defects present

Interstitial Diffusion



- More rapid than vacancy diffusion
- More empty interstitial positions than vacancies

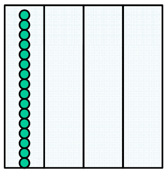
Diffusion Model

Process where particles tend to spread out or redistribute due to random thermal motion from high concentration to low concentration

Ex: spill a beer and eventually the whole room smells like a brewery

Or perfume

1-D system particles have an equally chance of jumping left or right due to thermal energy, if hit a wall bounce back to original bin



Diffusion – (doping Si)

- Activation energy-energy required to get over potential barrier (change location)

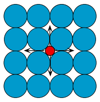
$$D = D_0 \exp\left(-\frac{E_A}{kT}\right)$$

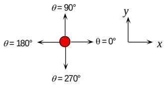
Arrhenius Rate Equation

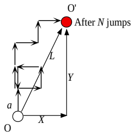
- How far does the impurity move- root mean displacement

$$L = \sqrt{2[D(T)t]_{total}}$$

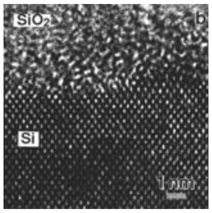
$$L = \sqrt{2\left(\sum_i D_i t_i\right)}$$

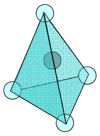






Silicon Oxide

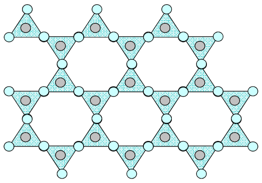




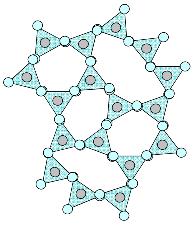
$(SiO_4)^{4-}$ tetrahedron

Silicon and four closest oxygen atoms

Quartz vs fused silica



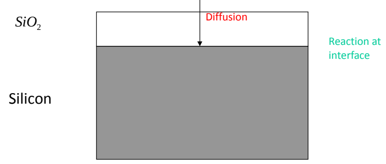
Crystalline Quartz



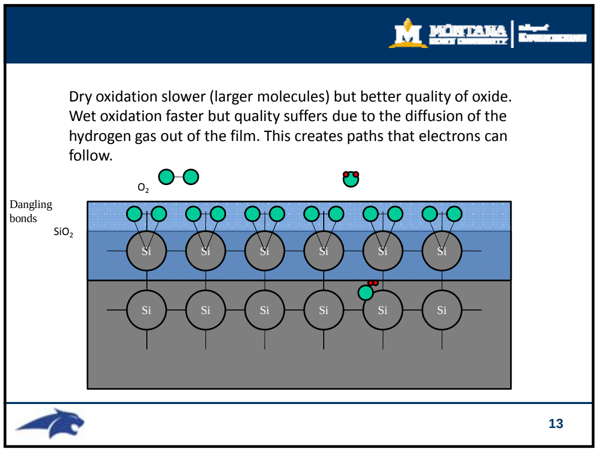
Amorphous fused silica

Thermal Oxidation of Silicon

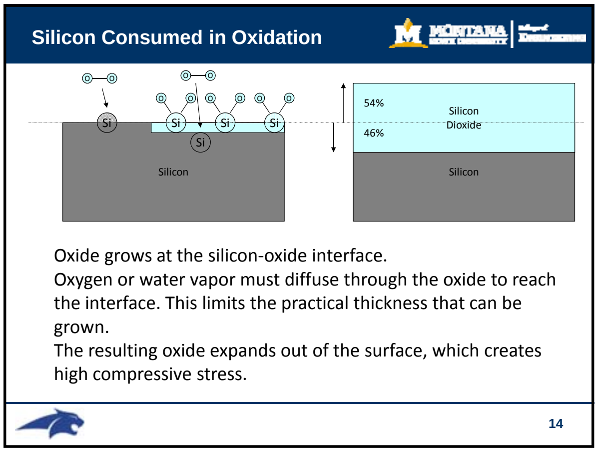
Ambient	Dry	Wet
	O_2	H_2O
	$Si + O_2 \rightarrow SiO_2$	$Si + 2H_2O \rightarrow SiO_2 + 2H_2$



Which method gives the better quality insulator Wet or Dry oxidation? Why?
Which method is faster? Why?



Dry oxidation slower (larger molecules) but better quality of oxide. Wet oxidation faster but quality suffers due to the diffusion of the hydrogen gas out of the film. This creates paths that electrons can follow.

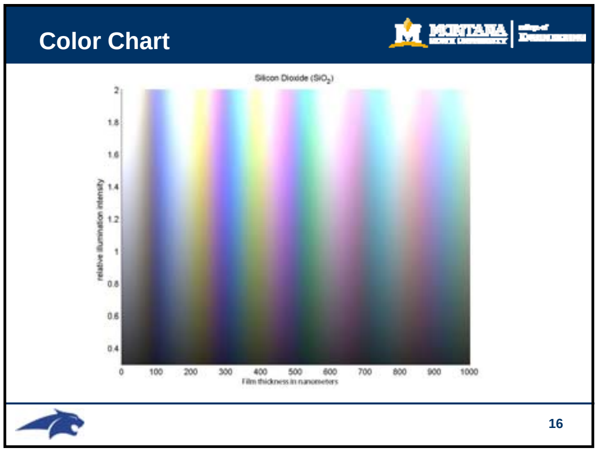


Silicon Consumed in Oxidation

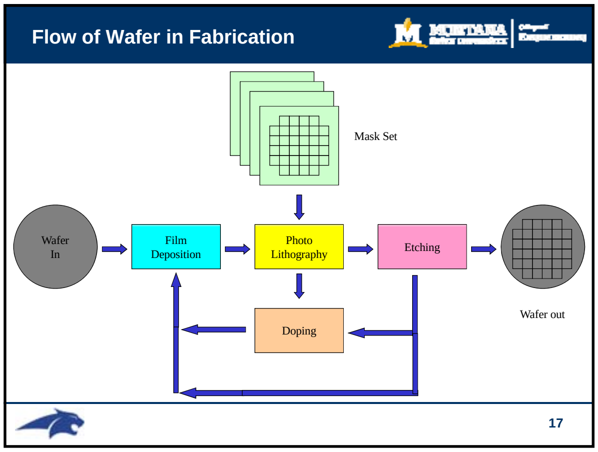
Oxide grows at the silicon-oxide interface.
Oxygen or water vapor must diffuse through the oxide to reach the interface. This limits the practical thickness that can be grown.
The resulting oxide expands out of the surface, which creates high compressive stress.

Thermal Oxidation of Silicon

- Silicon oxidizes on exposure to oxygen
  - "Dry": $Si + O_2 \rightarrow SiO_2$
  - "Wet": $Si + 2H_2O \rightarrow SiO_2 + 2H_2$
- Room temperature in air creates "Native Oxide"
  - Very Thin - ~1nm – poor insulator, but can impede surface processing of Si
- Dry Oxide: 900-1200°C in O_2
  - Thin 0.05-0.5μm : Excellent insulator: gate oxides
- Wet Oxide: 900-1200°C in H_2O
  - Thick <2.5μm : Good Insulator: field oxides, Masking



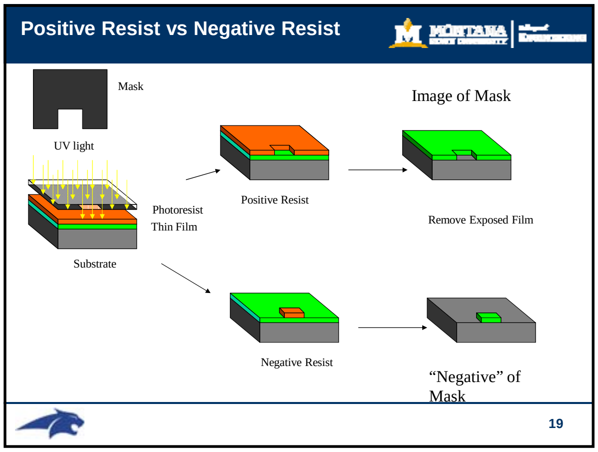
Color Chart



Flow of Wafer in Fabrication

Lithography

- Lithography is the basic technique to define and transfer patterns in most microfabrication procedures
- Photolithography uses UV light through a mask onto a photosensitive organic (photoresist, PR)
- Positive resist→exposed resist is removed in developer→"What shows goes" (image of mask)
  - Shipley 1813
- Negative resist→UV light cross-links polymer and developer rinses away non-cross-linked chains→exposed remains (negative of mask)
- PR protects region for the next process step



Positive Resist vs Negative Resist

Mask

UV light

Photoresist
Thin Film

Substrate

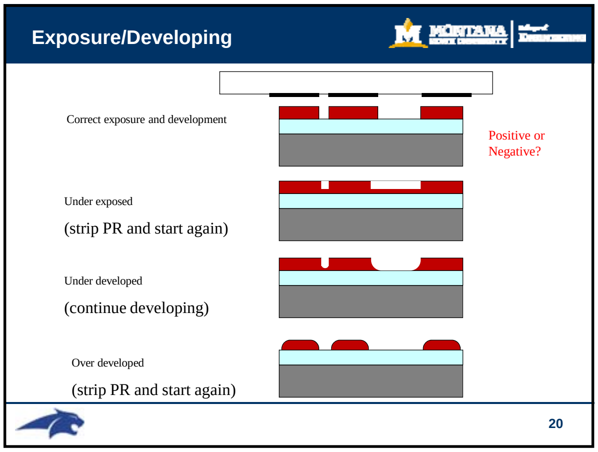
Positive Resist

Image of Mask

Remove Exposed Film

Negative Resist

"Negative" of Mask



Exposure/Developing

Correct exposure and development

Positive or Negative?

Under exposed

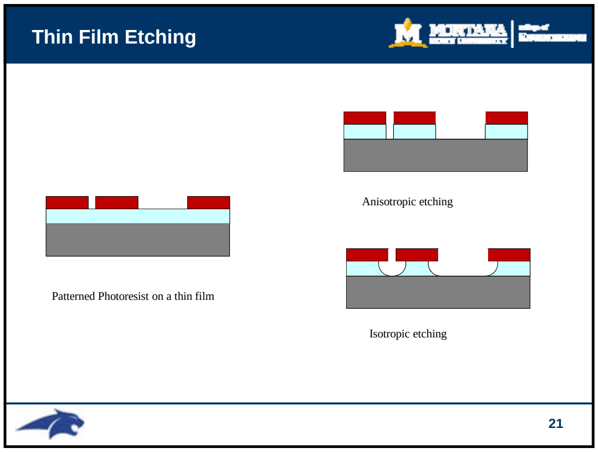
(strip PR and start again)

Under developed

(continue developing)

Over developed

(strip PR and start again)

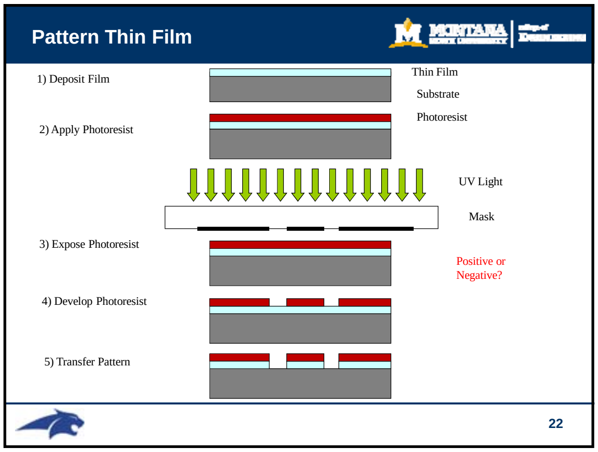


Thin Film Etching

Patterned Photoresist on a thin film

Anisotropic etching

Isotropic etching



Pattern Thin Film

1) Deposit Film

Thin Film

Substrate

Photoresist

2) Apply Photoresist

UV Light

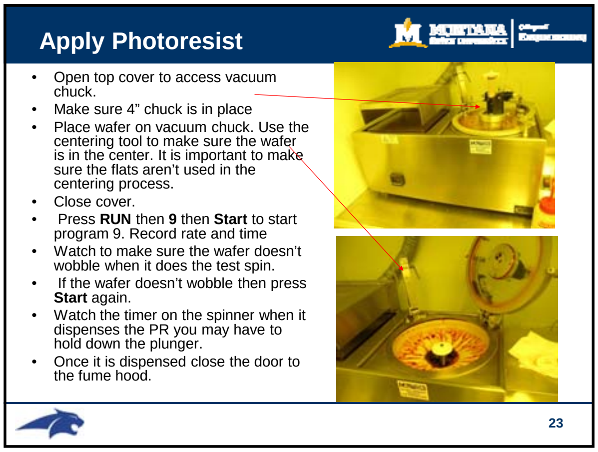
Mask

3) Expose Photoresist

Positive or Negative?

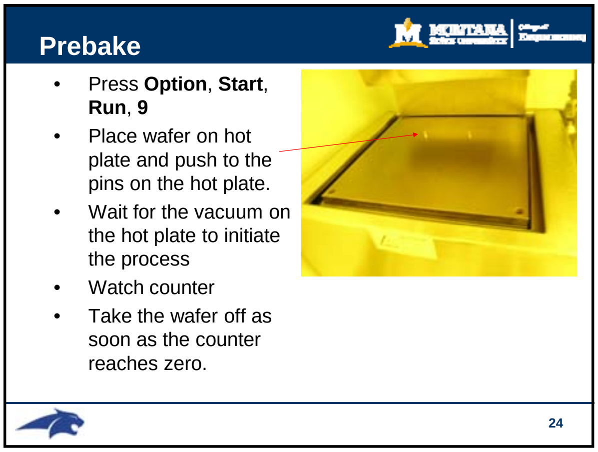
4) Develop Photoresist

5) Transfer Pattern



Apply Photoresist

- Open top cover to access vacuum chuck.
- Make sure 4" chuck is in place
- Place wafer on vacuum chuck. Use the centering tool to make sure the wafer is in the center. It is important to make sure the flats aren't used in the centering process.
- Close cover.
- Press **RUN** then **9** then **Start** to start program 9. Record rate and time
- Watch to make sure the wafer doesn't wobble when it does the test spin.
- If the wafer doesn't wobble then press **Start** again.
- Watch the timer on the spinner when it dispenses the PR you may have to hold down the plunger.
- Once it is dispensed close the door to the fume hood.



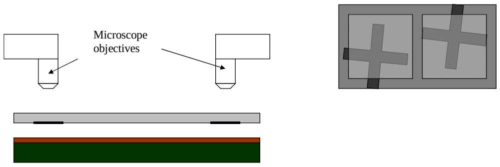
Prebake

- Press **Option**, **Start**, **Run**, **9**
- Place wafer on hot plate and push to the pins on the hot plate.
- Wait for the vacuum on the hot plate to initiate the process
- Watch counter
- Take the wafer off as soon as the counter reaches zero.

ABM Contact Aligner

Alignment position

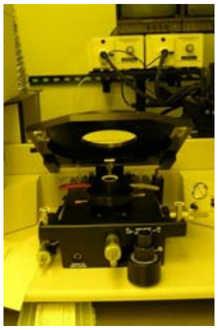
- Groups of alignment marks should be placed near the perimeter of the mask sets



- Makes rotational alignment easier
- Alignment is iterative process x-y then theta, x-y then theta…

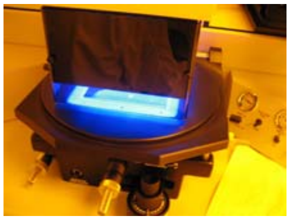
Exposure

- Turn on vacuum pump.
- Put mask on the mask holder and turn on the vacuum. (Insert mask with chrome side down)
- Raise the wafer stage (switch on the right)
- Load wafer onto vacuum chuck. Turn on vacuum chuck. Beware of flat position
- Lower stage.
- Raise wafer until it comes is contact with the mask. You will feel the micrometer knob slip.



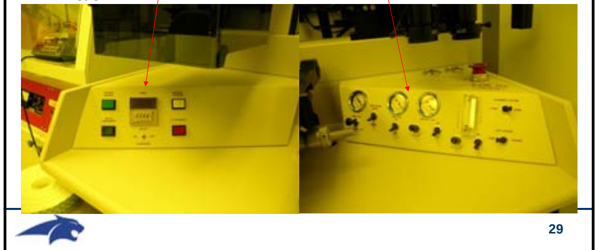
Aligner Mask Holder

- Lower wafer 100 µm
- Calculate the exposure time
- Auto expose. Don’t look at the light.
- Remove mask and wafer.
- Leave the machine on.



Aligner controls

- UV intensity: 30 mW/cm^2
- Set exposure time (~4.5 sec)
- Exposure dose 135 mJ/cm^2
- Vacuum controls
- Nitrogen flow

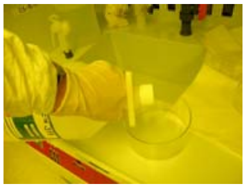


Development

- PR comes with corresponding developer.
- Typically a KOH dissolved in water that reacts with PR to form amines and metallic salts
- Very temperature sensitive chemical reaction, therefore need to monitor or set temperature.
- After development a hard bake is used to further set the PR and drive off absorbed water and solvent.

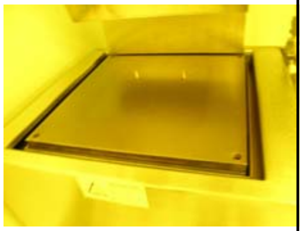
Develop

- MF 319 or AZ726
- Pour developer into crystallization dish
- Time the development
- Record time and developer concentration
- Rinse and inspect
- If PR is not entirely removed in exposed areas, return to developer
- Record additional time



Postbake

- If patterns are well defined post bake
- This drives off the remaining solvent
- Record time and temperature



Wet Etching Silicon Dioxide

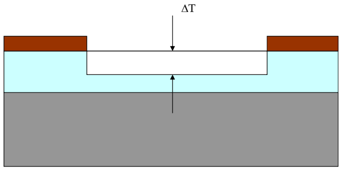
- HF supplied by vendor is 49%
  - Etch rate too fast

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

- Reaction consumes HF → rate will be function of time
- Buffering agent added to maintain HF concentration
  - Ammonium Fluoride: NH_4F
- 6:1 Buffered Oxide Etch
  - 6:1→NH_4F:HF (40%:49%)

Etch Rate

- The rate at which the material is removed



$$\text{etch rate} = \frac{\Delta T}{\Delta t} = \frac{\text{change in thickness}}{\text{change in time}}$$

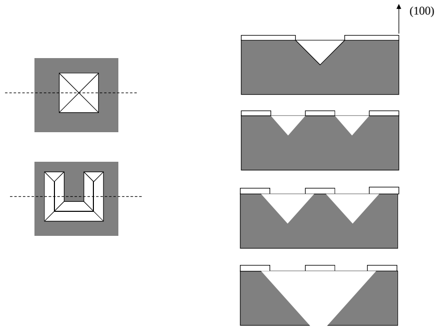
Etch Oxide (HF solution)

- BOE 6:1
- Etch rate 900nm/min
- Calculate required time for your oxide thickness
- Approx. 5-6 minutes
- Rinse and dry
- It is better to over etch at this step than under etch.
- Record time and concentration used

Solvent Clean

- Acetone-Red
- Isopropyl Alcohol-Blue
- Methanol -Green
- DI water
- Dry with nitrogen gun
- Store wafer in dry box

Anisotropic Wet Etch



Mechanism of Wet Silicon Etches

- Injection of holes into silicon to form Si^+
- Attachment of OH^- to the Si^+
- Reaction of hydrated Si with complexing agent in solution
- Dissolution of reacting products into solution

$$Si + 2OH^- + 4h^+ \Rightarrow Si(OH)_2^{\ 2+}$$

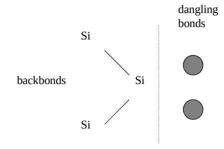
$$4H_2O + 4e^- \Rightarrow 4OH^- + 2H_2$$

$$Si(OH)_2^{\ 2+} + 4OH^- \Rightarrow SiO_2(OH)_2^{\ 2-} + 2H_2O$$

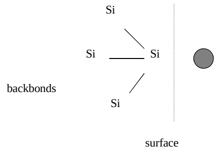
$$Si + 2OH^- + 2H_2O \Rightarrow SiO_2(OH)_2^{\ 2-} + 2H_2$$

Hydrogen gas bubbles

Why crystal Selectivity in Si



Si atoms on (100) plane have 2 dangling bonds/surface atom, OH^- reduces strength of backbonds



Si atoms on (111) plane have 1 dangling bonds/surface atom, breaking the three backbonds is the rate limiting step

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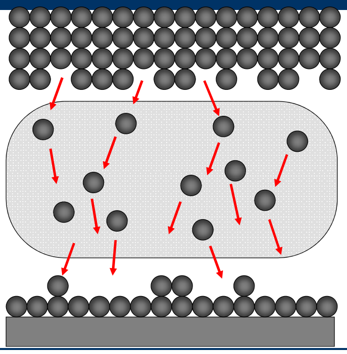
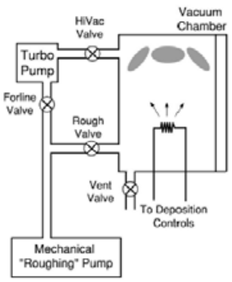
3 Basics Steps of Evaporation

- Atoms from a solid are vaporized
- Vaporized atoms are transported through a reduced pressure region
- Atoms condense on a solid surface to form a thin film



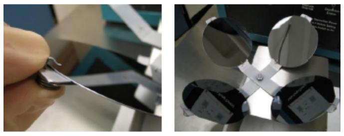
Our Physical Vapor Deposition (PVD)



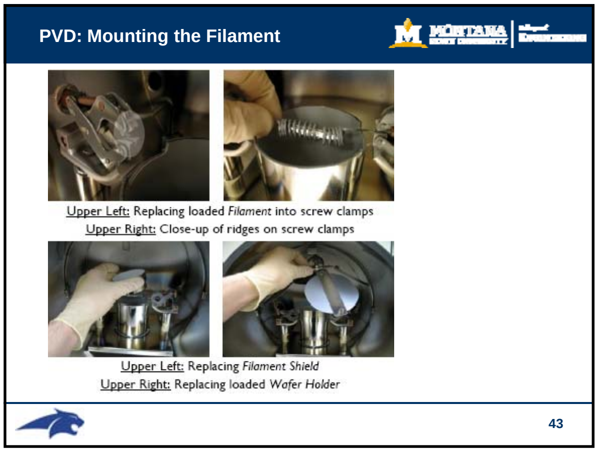
Above: Schematic of Modu-Lab thermal PVD

PVD: Loading the Wafers

Upper Left: Aluminum evaporation sample loaded into *Filament*
Upper Right: Loading a wafer into *Wafer Holder*



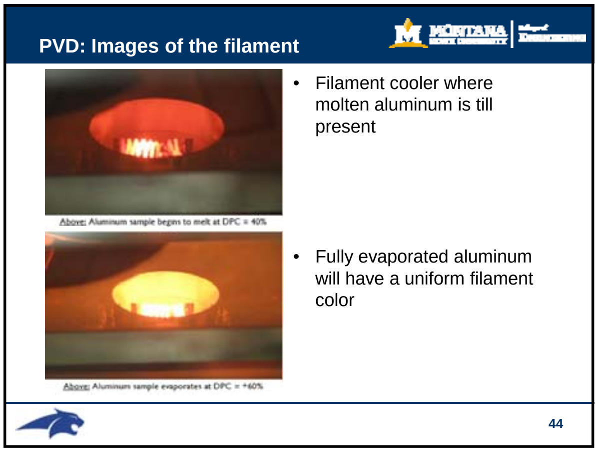
Upper Left: Close-up of a spring clip
Upper Right: Fully-loaded *Wafer Holder*



PVD: Mounting the Filament

Upper Left: Replacing loaded *Filament* into screw clamps
Upper Right: Close-up of ridges on screw clamps

Upper Left: Replacing *Filament Shield*
Upper Right: Replacing loaded *Wafer Holder*



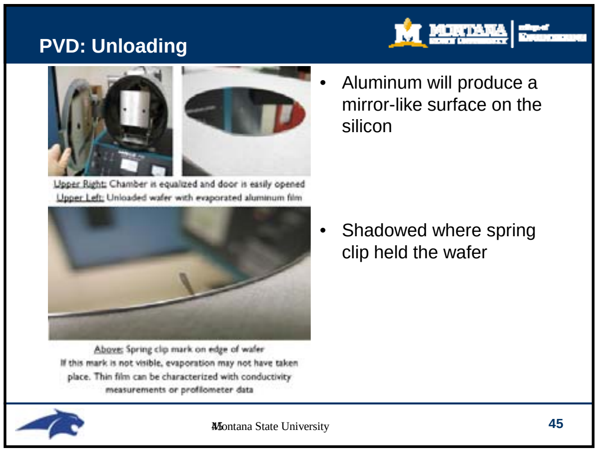
PVD: Images of the filament

- Filament cooler where molten aluminum is till present

Above: Aluminum sample begins to melt at DPC = 40%

- Fully evaporated aluminum will have a uniform filament color

Above: Aluminum sample evaporates at DPC = +60%



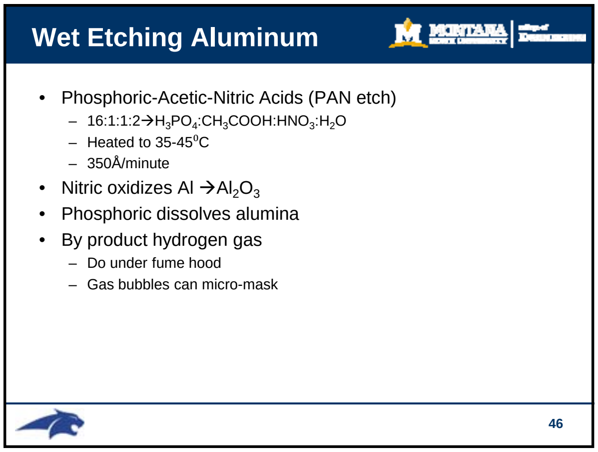
PVD: Unloading

- Aluminum will produce a mirror-like surface on the silicon

Upper Right: Chamber is equalized and door is easily opened
Upper Left: Unloaded wafer with evaporated aluminum film

- Shadowed where spring clip held the wafer

Above: Spring clip mark on edge of wafer
If this mark is not visible, evaporation may not have taken place. Thin film can be characterized with conductivity measurements or profilometer data



Wet Etching Aluminum

- Phosphoric-Acetic-Nitric Acids (PAN etch)
  - 16:1:1:2→H_3PO_4:CH_3COOH:HNO_3:H_2O
  - Heated to 35-45^{0}C
  - 350Å/minute
- Nitric oxidizes Al →Al_2O_3
- Phosphoric dissolves alumina
- By product hydrogen gas
  - Do under fume hood
  - Gas bubbles can micro-mask