

MEMS LAB MANUAL

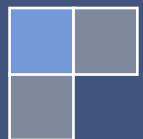
2007

MEMS LAB MANUAL

A complete description of the fabrication sequence for piezoresistive MEMS sensors. This manual was designed for use with the Montana Microfabrication Facility at MSU.

Special Thanks to:
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SUPPLIERS

University of Minnesota Nano Fabrication Center (NFC): Photomasks
www.nfc.com

Virginia Semiconductor: Silicon Substrates
www.virginiasemi.com

JT Baker: Chemical Supplies
www.jtbaker.com

Technical Glass Products Inc: Quartz-ware
www.technicalglass.com

Kurt J Lesker Company: Evaporation Filaments
www.lesker.com

MSU Chem-store: Labware/Chemical Supplies
www.chemistry.montana.edu/chemstores

Sigma-Aldrich: Chemical Supplies
www.sigmaaldrich.com

SPI Supplies: Wafer Tweezers
<http://www.2spi.com/spihome.html>

How to use this manual...

The manual is broken up into weekly segments containing multiple sections: *Goals, Equipment, Parameters, Methods* and *Results*. Each week a set of process goals is presented to the user along with a list of equipment and the methods used to achieve those goals. The parameters segment is devoted to process dependent parameters specific to the fabrication methods used that week. The parameters are color coded to correspond to a specific process method. The methods section describes the processes used within that week to achieve the desired goals. The methods are numbered to correspond to a process goal. The result section is left blank for users to record the results and progress of their wafer.

14-week Overview

Introduction & Oxidation	Week 1
Creating the Piezoresistors pt 1	Week 2
Documenting, Cleaning & Oxidation	Week 3
Creating the Piezoresistors pt 2	Week 4
Documenting, Cleaning & Oxidation	Week 5
Aluminum Markers	Week 6
Backside Alignment & Si Bulk Etch	Week 7
Bulk Etch, Bonding & Mask #3 Again?	Week 8
Vias & Aluminum Evaporation	Week 9
Aluminum Pads, Debond & Anneal	Week 10
Photolithography & Etching (Vias)	Week 11
Release & Test	Week 12
Testing	Week 13
Testing	Week 14

GOALS:

1. Familiarize students with the cleanroom layout, equipment, safety and procedure.
2. Present an overview of the MEMS fabrication process and various process techniques (i.e. photolithography, etching, etc)
3. Characterize wafer substrates and ID individual wafers
4. RCA clean (Optional for new wafers)
5. Oxidation (Field oxide)

EQUIPMENT:

- Wafer Scribe
- JANDEL 4-point Probe Station
- RCA tanks (Optional)
- MODULAB Oxidation Furnace

PARAMETERS

Oxidation Parameters

Temperature (°C)	Time (minutes)	Type (wet or dry)	N ₂ /O ₂ Flow	Bubbler Setting
1000	90	Wet	7/9	40

Methods:

1. Clean Room Etiquette

The lab employs many hazardous chemicals and processes. The safety of the lab students and users is the number one priority when participating in the lab. Follow all gowning and safety procedures outlined by the lab TA.

To maintain the integrity of the wafers and the equipment, adhere to the process descriptions and details provided by the lab TA.

The most common reason a wafer will not make it to the end of the fabrication sequence, is poor handling. The wafer should be handled with the wafer-tweezers and with great attention. Limit the handling of the wafer with gloved hands to the edges and only during necessary circumstances. Never touch the wafer with a bare hand and never touch the center of the wafer, even with gloved hands.

When processing in the cleanroom, sources of contamination are another factor which may inhibit the success of the fabrication. Therefore, do not talk next to the wafers, keep the lid to the wafer box closed and lastly, do not hastily move about the clean room and do not get in a hurry to finish a process. When a lab student gets in a hurry it creates a situation with a greater likelihood of breaking a wafer or damaging a piece of equipment.

Week 1



Methods:

2. Process Overview:

The piezoresistive MEMS sensors are fabricated using bulk silicon processing techniques. An overview of the sequence is shown to the right (**Figure 1**). The fabrication portion of the lab should take roughly eleven to twelve weeks to complete, with the final two to three weeks devoted to testing.

A copy of the layout of the wafer is shown in the bottom-right (**Figure 2**). The MEMS sensors consist of a wide variety of piezoresistive accelerometers, pressure sensors, and testing devices. A complete list of the devices and their dimensions are included at the end of this document.

The alignment system plays a crucial role in the success of the fabrication. The alignment system is also shown in detail at the end of the manual.

Both sides of the wafer will be processed during the fabrication; therefore, great care should be used when handling and processing the wafers.

Document everything seen and done in a clean room lab notebook. Record all measurable quantities and procedures and any deviations. It is important to record every detail which may help explain device failures or anomalies.

3. Wafer Characterization and ID:

Semiconductor substrates, referred to as wafers, can easily be ordered through retailers and customized for specific applications. The wafers used for the lab are *100mm in diameter, 475±25 μm thick, <100>, double-side polished, single-crystal silicon, doped with phosphorous (N-type) to a resistivity of 1-30 Ω/cm.*

A simple test to determine if the substrate is P-type or N-type silicon is known as the “Hot Probe Test.” Using a DMM and a soldering iron, heat the positive probe of the DMM for several minutes with the soldering iron. Make sure the DMM is set to measure “mV.” Place both probe tips, positive and negative(ground) to the wafer surface. If the DMM indicates a positive voltage the substrate is N-type, if the voltage is negative the substrate is P-type. This test should be accurate up to a resistivity of 1000 Ω/cm.

Figure 1 Overview of the fabrication sequence .

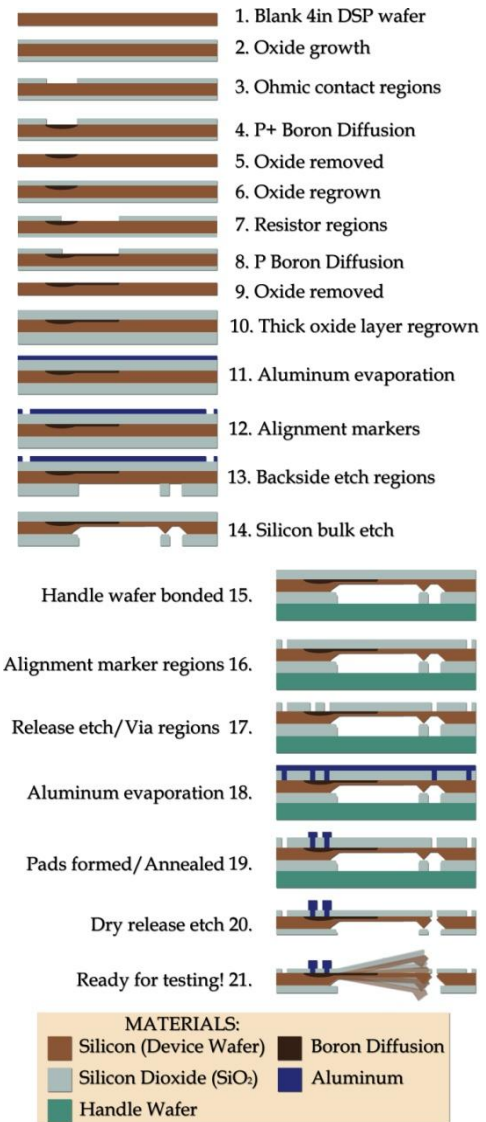
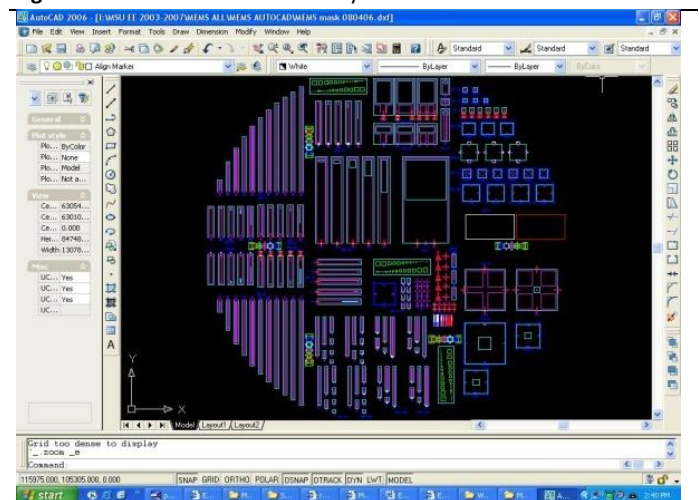


Figure 2 AutoCAD view of wafer layout.



Methods:**3. Wafer Characterization and ID:****Continued...**

The bulk resistivity (Ω/cm) is determined by first acquiring the sheet resistivity (Ω/\square) of the wafers using the *JANDEL 4-point Probe Station* and then multiplying this value by the wafer thickness and a correction factor. See the JANDEL manual for details on using the 4-point probe.

To keep track of individual wafers, a scribe can be used to mark the edge of the wafer with an identification mark, typically a number or letter. With all the etching processes that occur during the lab, scribing can lead to problematic defects, so it should only be used if necessary. To scribe, lightly press the tip of the scribe against the surface of the wafer and with as few strokes as possible 'scribe' a section number and wafer number. Scribing should be done as close to the edge as possible to limit the effect on fabricated devices.

5. Oxidation: Growing SiO_2 **(Check Parameters section for details)**

The goal of the first oxidation run is to grow enough silicon dioxide (SiO_2) to mask the subsequent diffusion, roughly a $0.5\mu\text{m}$ thick film of SiO_2 .

To oxidize, insert the wafers into *MODULAB oxidation furnace* using the quartz rod and quartz boat. There should be two dummy wafers, one at the front of the boat and another at the rear, to maintain uniformity across the boat. Ramp the furnace to 600°C before the removing the quartz boat and loading the wafers. Prior to the temperature reaching 400°C , turn on the nitrogen to purge the furnace. Also, set the potentiometer on the bubbler if performing a wet oxidation (which we are). Once the wafers are loaded and in place at the center of the furnace, ramp the furnace to the desired temperature. When the desired temperature is reached start the timer, stop the nitrogen flow and turn on the oxygen. After the allotted time, ramp the furnace down to 600°C pull the boat, remove the wafers, and set them aside to cool. When finished, turn the furnace to 0°C and turn off the nitrogen when the temperature drops below 400°C .

Figure 3 Scribing the surface of a wafer using a steel-tipped scribe.**Figure 4** A student using a quartz rod to insert wafers into the oxidation furnace.

Creating the Piezoresistors pt 1

Week 2

GOALS:

1. Measure the thickness of the SiO₂ with the Nanospec.
2. Photolithography (Mask #1 Contacts)
3. Hardbake
4. Etch SiO₂
5. Full Wafer Clean (Solvent & RCA)
6. Boron Diffusion

EQUIPMENT:

- Nanospec
- Teflon cassette
- Acetone, Methanol, Isopropyl
- RCA clean tanks
- Boron Diffusion Furnace
- BORONPLUS GS139 Boron Sources

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5000	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #1)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm ²)	UV Dose (J/cm ²)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Hard-bake Parameters

Harbake Program	Temperature (°C)	Time (minutes)
#2	115	2

SiO₂ Etch Parameters * for 4,200-4,500Å thick SiO₂ layer

BOE concentration	SiO ₂ Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5*	Shipley 1813 Photoresist

RCA Clean Parameters

Piranha Solution	Piranha Etch Time (minutes)	BOE solution	BOE Etch Time (seconds)	Ionic Clean	Ionic Clean Etch Time (minutes)
3:1 H ₂ O ₂ :H ₂ SO ₄	10	6:1	10	6:1:1 H ₂ O:H ₂ O ₂ :HCl	10

Boron Diffusion Parameters (DIFFUSED CONTACTS)

Boron Source	Temperature (°C)	Time (minutes)	N ₂ Flow
BORONPLUS GS-139	1050	120	7

Methods:

1. Measuring the SiO_2 thickness:

The thickness of the freshly grown silicon dioxide layer is measured with the *Nanospec*. Choose the appropriate film type during the prompts and use a blank wafer as reference. Measure the thickness at several different points on the wafer to monitor uniformity and determine a maximum film thickness. Also note that the thickness of the SiO_2 determines the color of the wafer, therefore, color can be used to approximate film thicknesses and identify anomalies in film. For reference, the *Nanospec* prompts before measuring the SiO_2 thickness are:

Is wavelength 480nm? Y (if not, type N and value)
Data bank option? N
Refr index option? N
Switch to printer? N
Enter film type: 1-SiO2
Enter obj lens: 1 = 10x

2. Photolithography with Mask #1 (Contacts):

Spin-coating & Soft-baking

(Check Parameters section for details)

The goal of the photolithography step is to transfer patterns from the mask set to the wafer surface. Photoresist, which is a UV sensitive chemical, is patterned by selectively exposing certain regions with UV light. Photoresist is also chemically resistant to the SiO_2 etchant, hydrofluoric acid (also referred to as BOE); therefore it is used to mask, or block, select portions of the SiO_2 from being etched.. The first patterns transferred to the wafer are the diffused contacts, which act as a bridge between the piezoresistors and aluminum contacts.

Begin by using the *BREWER spin-coater* to spin a thin film ($\sim 1\mu\text{m}$) of *SHIPLEY 1813* photoresist onto the topside of the wafer. Next, transfer the wafer to the adjacent hotplate and soft-bake to remove solvents and harden the resist. A good coating of photoresist will be barely visible to the naked eye and have a minimal number of streaks or blotches (see **Figure 7**). If there are a large number of defects, solvent clean, dehydrate, and try re-spinning more photoresist.

Figure 5 Students using the Nanospec to measure the SiO_2 thickness.



Figure 6 View from the Nanospec eyepiece, the edge of the octagon should be in focus for proper measurement.

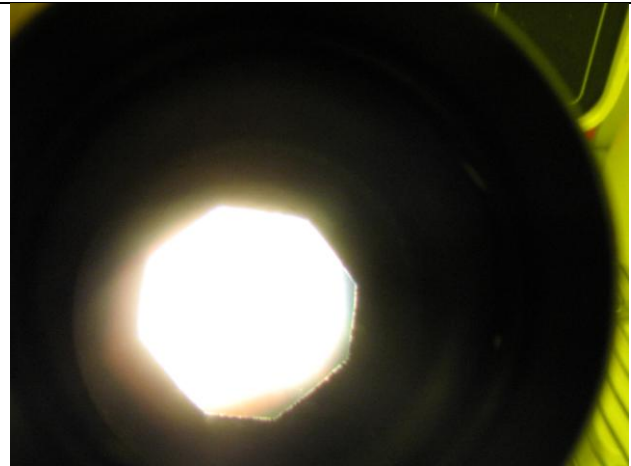
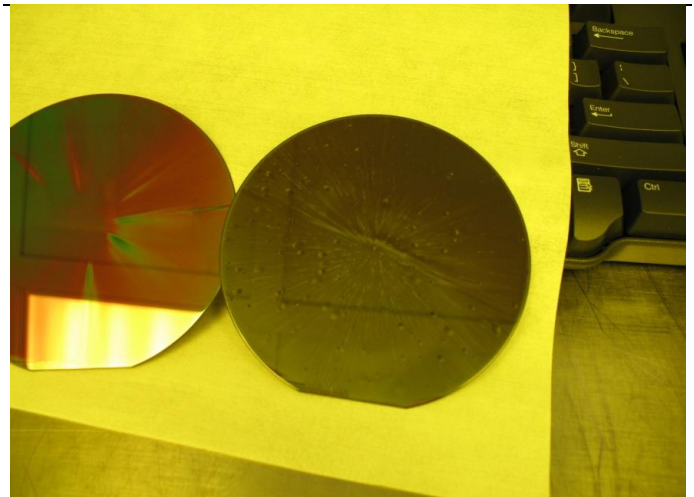


Figure 7 Wafers that have been spun with photoresist and exhibit signs of a poor coating i.e. streaking, blotchiness and color gradients



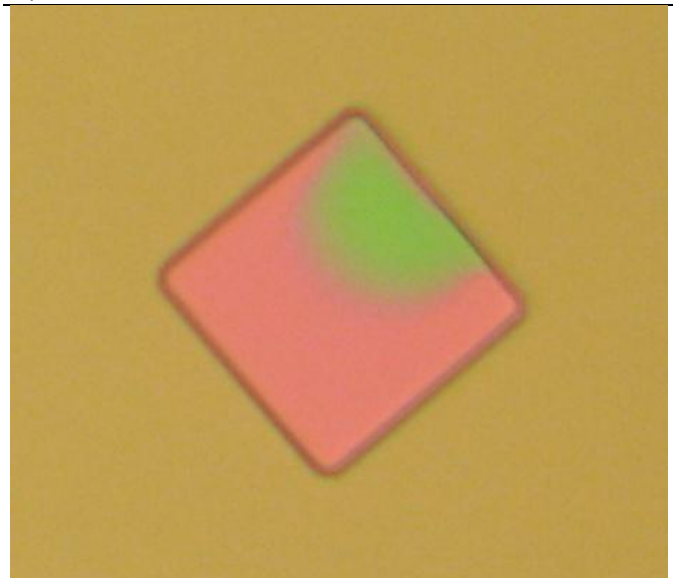
Methods:**2. Photolithography with Mask #1 (Contacts):
Exposure & Development
(Check Parameters section for details)**

Proceed by patterning the photoresist with Mask #1. Start by loading the mask onto the *ABM contact-aligner* mask stage. Turn the mask-vac on and raise the mask stage. Carefully, load the wafer onto the substrate chuck and orient it such that the <110> plane (wafer flat) is to the left and running straight up and down. Turn on the substrate-vac to lock the wafer in place and lower the chuck to avoid hitting the contact mask. Next, lower the mask stage and raise the substrate chuck up to meet the mask, fringe lines will become visible as the wafer and mask come into contact. Align the mask to the wafer using the markers on the sides of the wafer (no alignment for the first photolithography step). Turn on the contact-vac to remove any air gap between mask and wafer. Adjust the exposure time and channel setting then expose. Remove the wafer by turning off the contact-vac, lowering the substrate chuck, raising the mask frame, and turning off the substrate-vac. Transfer the wafer to a dish of *MF319 developer* (a faint outline of the features can be seen at this point), submerge the wafer in *MF319* and gently swirl for 30-60 seconds until the exposed resist is completely dissolved. If done correctly there should be no photoresist left in the diffusion contact regions. If there is (see **Figure 8**), resubmerge the wafer in the *MF319* developer for additional time. If unsuccessful, use a solvent clean to strip the photoresist, dehydrate and re-spin again. When finished, pour the used *MF319* into the *MF319* waste container located under the solvent bench next to the photoresist.

**3. Hard-baking:
(Check Parameters section for details)**

Hard-baking is the final step in the photolithography sequence, but to emphasize its importance it gets its own heading. The goal of the hard-bake is to remove any remaining solvents and/or water from the resist. It has been observed, that without hard-baking, the photoresist exhibits adhesion problems and frequently delaminates from the surface during etching. Hard-baking is very similar to soft-baking and follows the same procedure. Load a wafer onto a hotplate for a set time at the appropriate temperature.

Figure 8 A microscope picture of a patterned feature after development in *MF319*. The color gradient indicates that the photoresist was not completely removed during the development. The wafer should be developed for longer or redone with a longer exposure.



Methods:

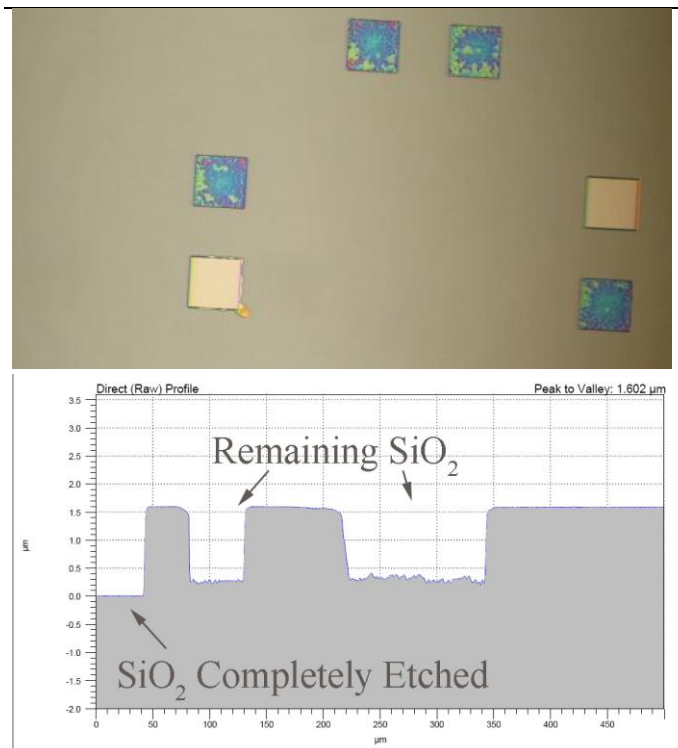
4. Etching the SiO_2 :

(Check Parameters section for details)

The goal of the SiO_2 etch is to remove the silicon dioxide from the exposed regions in the photoresist. Silicon dioxide is etched with BOE (Buffered Oxide Etch) which is a combination of hydrofluoric acid and buffering chemicals to stabilize the reaction. BOE is highly selective to silicon dioxide so the photoresist will not be etched.

This step should be carried out by the lab TA for safety reasons. Begin by loading the wafers into a *Teflon cassette* with equal spacing between wafers. Using the handle, submerge the cassette in *6:1 BOE* for the appropriate amount of time or until the exposed SiO_2 is completely removed. To determine if the SiO_2 is completely removed, check the regions for color (see **Figure 9**) and hydrophobicity. When the etch is complete, remove the cassette and rinse the wafers in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers with DI water and nitrogen gun.

Figure 9 An example of micromasking with features that were etched but had undeveloped photoresist masking the etch. The blue color indicates that SiO_2 still remains over those features. The lighter color is exposed silicon. The following graph is from a profilometer measurement of the etched areas.



5. Wafer Cleaning:

(Check Parameters section for details)

The wafers need to be cleaned to remove photoresist, and any possible sources of contamination before being placed in a high temperature furnace.

To remove the photoresist a solvent clean is performed. Begin by placing an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with *acetone* using the squirt bottle, and follow with *methanol* and *isopropyl*. The acetone will remove the photoresist and the methanol and isopropyl will remove any acetone residue. Rinse the wafers in DI water and dry with a nitrogen gun. When finished pour the solvent waste into the *Solvent Waste Container*.

To remove possible sources of contamination a modified RCA dean is performed. The RCA dean consists of rinsing the wafers in three chemical solutions. The first is a mixture of sulfuric acid and hydrogen peroxide known as *Piranha etch*. The piranha etch will remove any organic material. The second mixture is a simple BOE solution which will strip any native oxide that has accumulated on the wafer surface. The third and final solution is designed to remove any heavy metal ions, it is a mixture of hydrochloric acid, water and hydrogen peroxide. This solution is referred to as *ionic clean*.

This step should also be carried out by the lab TA. Load the wafers into a *Teflon cassette* and transfer the cassette between the RCA solutions until the cleaning is complete. Rinse the wafers and cassette in a bucket of DI water then pull each wafer and rinse and dry by hand.

Figure 10 Solvent deaning chemicals: Acetone, Methanol & Isopropanol.



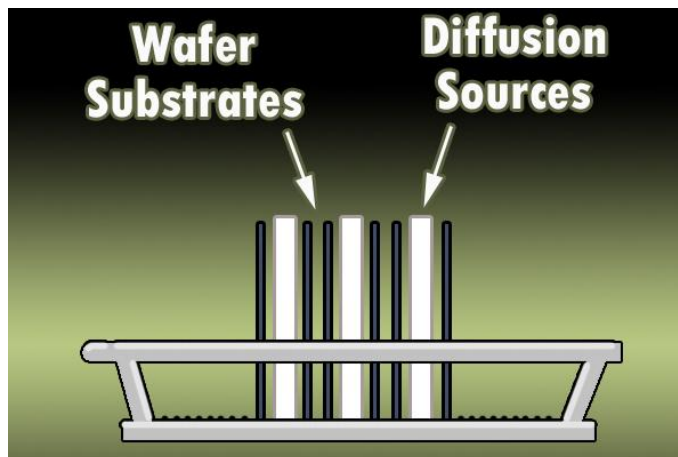
6. Boron Diffusion:

(Check Parameters section for details)

The goal of the boron diffusion is to create the highly conductive regions called diffused contacts. The diffusion is modeled as a solid-solubility-limited diffusion followed by several drive-in steps. The expected resistivity can be derived from this model and verified with the BORONPLUS data sheet.

To diffuse P-type (Boron) material, ramp the *Boron diffusion furnace* to 600°C and set the nitrogen flow. Remove the quartz boat with the solid, white, *BORONPLUS GS139 sources* already in place. Load the silicon wafers next to the sources into the quartz boat with the patterned side facing a source (**see Figure B**). Insert the quartz boat to the center of the furnace and ramp the furnace to the desired temperature. When the desired temperature is reached start the timer. After the allotted time, ramp the furnace down to 600°C, pull the quartz boat and remove the wafers and set them aside to cool. When finished, turn the furnace to 0°C and turn off the nitrogen when the temperature drops below 400°C.

Figure B An illustration of how the wafers are loaded into the quartz boat next to the diffusion sources.



Documenting, Cleaning & Oxidizing

Week 3

GOALS:

1. Take pictures using the microscope and digital camera.
2. Strip the SiO₂ & BSG
3. Obtain 4-point probe measurements of the diffusion
4. RCA clean
5. Oxidation

EQUIPMENT:

- Optical Microscope
- CANON digital camera
- Teflon Cassette
- 6:1 BOE
- JANDEL 4-point Probe Station
- RCA clean tanks
- MODULAB Oxidation Furnace

PARAMETERS:

SiO₂ Etch Parameters* for 4,200-4,500Å thick SiO₂ layer

BOE concentration	SiO ₂ Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5* (will need longer to remove BSG layer)	Shipley 1813 Photoresist

RCA Clean Parameters

Piranha Solution	Piranha Etch Time (minutes)	BOE solution	BOE Etch Time (seconds)	Ionic Clean	Ionic Clean Etch Time (minutes)
3:1 H ₂ O ₂ :H ₂ SO ₄	10	6:1	10	6:1:1 H ₂ O:H ₂ O ₂ :HCl	10

Oxidation Parameters

Temperature (°C)	Time (minutes)	Type (wet or dry)	N ₂ /O ₂ Flow	Bubbler Setting
1000	90	Wet	7/9	40

Methods:

1. Taking Pictures:

With the first diffusion completed, the wafers now have observable features. From this point, one goal of the lab is to document the fabrication progress by taking pictures of the surface of the wafer as it moves through the sequence. Begin by using the *optical microscope* and *CANON digital camera* to take a picture of the diffused contacts (**shown in Figure 12**)

2. Stripping the SiO₂:

(Check Parameters section for details)

The wafer surface needs to be prepared for the next oxidation and diffusion cycle by removing all the patterned SiO₂ and Borosilicate glass (BSG) (this is formed over the diffused regions).

This step should be carried out by the lab TA for safety. Load the wafers into a *Teflon cassette* and submerge in *6:1 BOE* until the SiO₂ and BSG is completely removed. When finished rinse and dry with DI water and nitrogen

The BSG etches at a slower rate than the thermal SiO₂ so the amount of time to completely clear the wafer surface will take longer than the previous SiO₂ etch. To check that the surface is clear of oxide, run the wafer under DI water, if the water beads up and rolls off, the surface is clear, if not there is still some remaining oxide. This phenomenon occurs due to the hydrophobic nature of silicon and hydrophilic nature of silicon dioxide.

The diffused regions should be visible to the naked eye, and most likely brownish grey in color. If the regions are bluish, BSG is still present, and the wafers need to continue etching.

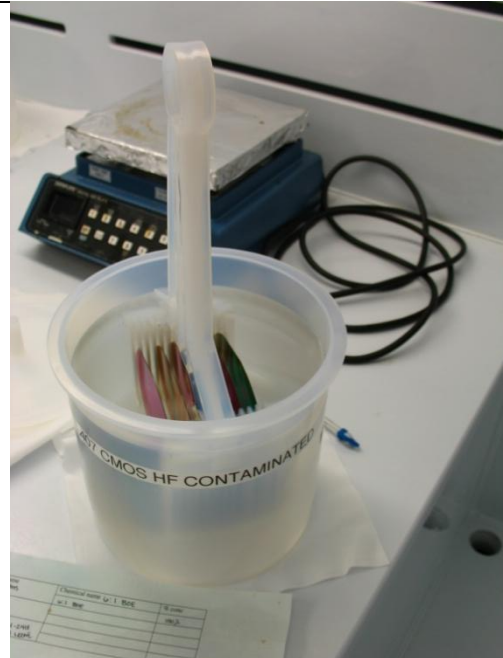
Figure 12 Diffused contacts. The silicon dioxide has been completely removed from the wafer. To the naked eye these features will look like small brownish spots.



Figure 11 A student using the optical microscope and digital camera to document the wafer progress.



Figure 13 Wafers being stripped of SiO₂ in a 6:1 BOE solution.



Methods:

3. Diffusion Measurements:

There is a large diffused rectangle on the side of the wafer (see the *Wafer Layout* section at the end of the document). This is a test region and is used to check the sheet-resistivity associated with the P diffusion. Use the *JANDEL 4-point probe* to measure the sheet resistivity of the diffusion. Start by raising the probe arm, uncapping the tip and placing the wafer on the stage. Align the probes over the test region and lower the arm into contact. Start the test by using a small current, roughly 100nA, and increment the current until the sheet resistivity stabilizes. Consult the JANDEL 4-point probe manual for further assistance.

The suppliers of the boron sources publish a data sheet that contains the expected sheet resistivity for deposition time and temperature. The measured sheet resistivity should correspond to the value found on this data sheet (shown in Figure 14)

4. RCA Cleaning:

(Check Parameters section for details)

REPEAT: To remove possible sources of contamination a modified RCA clean is performed. The RCA clean consists of rinsing the wafers in three chemical solutions. The first is a mixture of sulfuric acid and hydrogen peroxide known as Piranha etch. The piranha etch will remove any organic material. The second mixture is a simple BOE solution which will strip any native oxide that has accumulated on the wafer surface. The third and final solution is designed to remove any heavy metal ions, it is a mixture of hydrochloric acid, water and hydrogen peroxide.

This step should be carried out by the lab TA for safety. Load the wafers into a Teflon cassette transfer the cassette between the RCA solutions until the cleaning is complete. Rinse the wafers and cassette in a bucket of DI water then pull each wafer and rinse and dry by hand.

Figure 14 A graph from the BoronPlus datasheet illustrating the relationship between diffusion time, temperature and sheet resistivity. The graph should be used to verify measurements.

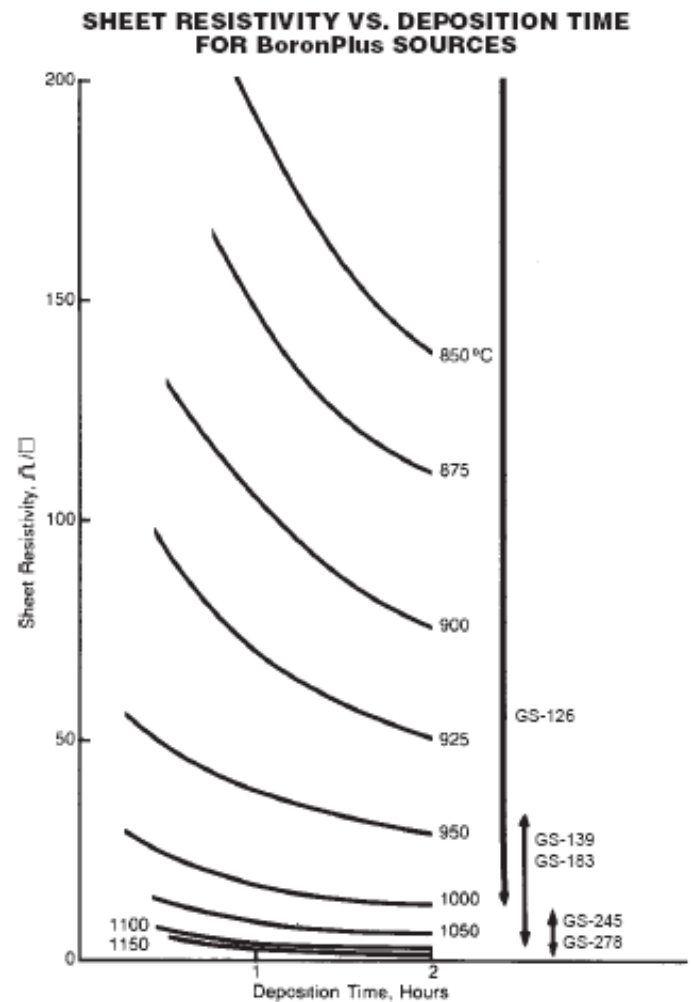
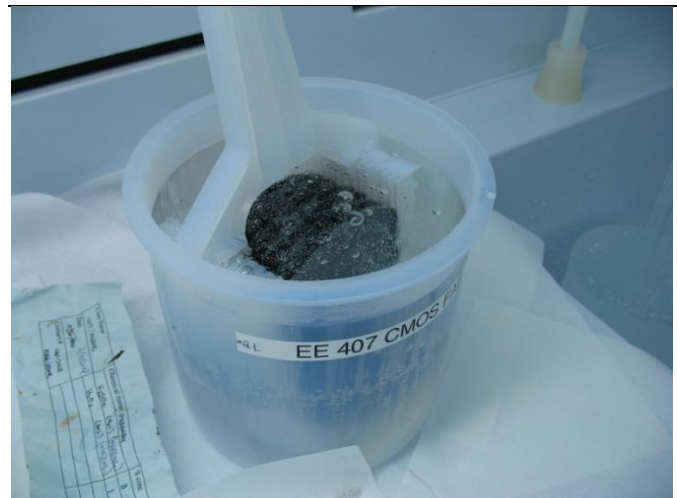


Figure 15 Wafers submerged in Piranha Etch to remove organic contaminants



5. Oxidation: Growing SiO₂**(Check Parameters section for details)**

The goal of the second oxidation run is the same as the first: deposit enough silicon dioxide (SiO₂) to mask the subsequent diffusion.

REPEAT: To oxidize, insert the wafers into oxidation furnace using the quartz rod and quartz boat. There should be two dummy wafers, one at the front of the boat and another at the rear, in order to maintain uniformity across the boat. Ramp the furnace to 600°C before the removing the quartz boat and loading the wafers. Before the furnace reaches 400°C, turn on the nitrogen to purge the furnace. Also, set the potentiometer on the bubbler if performing a wet oxidation (which we are). Once the wafers are in place at the center of the furnace, ramp the furnace to the desired temperature. When the desired temperature is reached start the timer, stop the nitrogen flow and turn on the oxygen. After the allotted time, ramp the furnace down to 600°C, pull the boat, remove the wafers and set them aside to cool. When the temperature drops below 400°C the nitrogen can be turned off.

GOALS:

1. Measure the thickness of the SiO₂ layer with the Nanospec.
2. Photolithography (Mask #2 Resistors)
3. Hardbake
4. Etch SiO₂
5. Full Wafer Clean (Solvent & RCA)
6. Boron Diffusion

EQUIPMENT:

- Nanospec
- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- 6:1 BOE
- Teflon cassette
- Acetone, Methanol, Isopropyl
- RCA clean tanks
- Boron Diffusion Furnace
- BORONPLUS GS139 Boron Sources

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5000	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #1)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm ²)	UV Dose (J/cm ²)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Harbake Parameters

Harbake Program	Temperature (°C)	Time (minutes)
#2	115	2

SiO₂ Etch Parameters * for 4,200-4,500Å thick SiO₂ layer

BOE concentration	SiO ₂ Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5*	Shipley 1813 Photoresist

RCA Clean Parameters

Piranha Solution	Piranha Etch Time (minutes)	BOE solution	BOE Etch Time (seconds)	Ionic Clean	Ionic Clean Etch Time (minutes)
3:1 H ₂ O ₂ :H ₂ SO ₄	10	6:1	10	6:1:1 H ₂ O:H ₂ O ₂ :HCl	10

Boron Diffusion Parameters (DIFFUSED CONTACTS)

Boron Source	Temperature (°C)	Time (minutes)	N ₂ Flow
BORONPLUS GS-139	1050	120	7

Methods:

1. Measuring the SiO_2 thickness:

Measure the thickness of the silicon dioxide at several different points on the wafer using the *Nanospec*. For reference, the *Nanospec* prompts for measuring SiO_2 thickness are:

Is wavelength 480nm? Y (if not, type N and value)
Data bank option? N
Refr index option? N
Switch to printer? N
Enter film type: 1-SiO2
Enter obj lens: 1 = 10x

2. Photolithography with Mask #2 (Resistors):

Spin-coating & Soft-baking

(Check Parameters section for details)

The goal of the photolithography step is to transfer patterns from the mask set to the wafer surface. Mask #2 contains the piezoresistor features which act as the sensing element for the MEMS devices.

REPEAT: Begin by using the *BREWER spin-coater* to spin a thin film of *SHIPLEY 1813* photoresist onto the topside of the wafer. Next, transfer the wafer to the adjacent hotplate and soft-bake to remove solvents and harden the resist. If done correctly, the layer of photoresist should have minimal streaks and blotches. The film will be barely visible to the naked eye. If there are a large number of defects, solvent clean, dehydrate, and try re-spinning more photoresist.

Figure 16 Completed Type-2 piezoresistors.

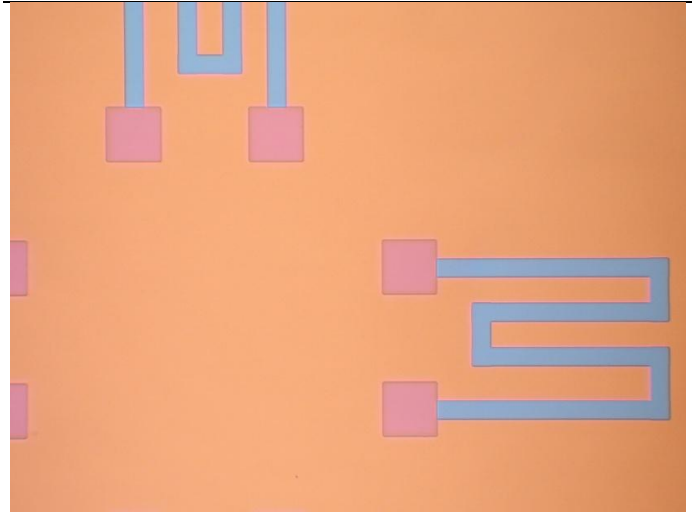


Figure 17 Two students using the ABM contact aligner for photolithography with Mask #2.



Figure 18 A lab TA handles acids at the rinse sink with full acid protection clothing.



Methods:**2. Photolithography with Mask #1 (Resistors):
Exposure & Development
(Check Parameters section for details)**

Start by loading Mask #2 onto the *ABM contact-aligner* mask stage. Turn the mask-vac on and raise the mask stage. Carefully, load the wafer onto the substrate chuck and orient it such that the <110> plane (wafer flat) is to the left and running straight up and down. Turn on the substrate-vac to lock the wafer in place and lower the chuck to avoid hitting the contact mask. Next, lower the mask stage and raise the substrate chuck up to meet the mask, fringe lines will become visible as the wafer and mask come into contact. Align the mask to the wafer using the markers on the sides of the wafer (see *Alignment System* at the end of the manual for details on the alignment marks). Turn on the contact-vac to remove any air gap between mask and wafer. Adjust the exposure time and channel setting then expose. Remove the wafer by turning off the contact-vac, lowering the substrate chuck, raising the mask frame, and turning off the substrate-vac. Transfer the wafer to a dish of *MF319 developer* (a faint outline of the features can be seen at this point), submerge the wafer in MF319 and gently swirl for 30-60 seconds until the exposed resist is completely dissolved. If done correctly there should be no photoresist left in the diffusion contact regions. If there is, resubmerge the wafer in the MF319 developer for additional time. If unsuccessful, use a solvent clean to strip the photoresist, dehydrate and re-spin again. When finished, pour the used MF319 into the MF319 waste container located under the solvent bench next to the photoresist.

4. Hard-baking:**(Check Parameters section for details)**

The goal of the hard-bake is to remove any remaining solvents and/or water from the resist. It has been observed, that without hard-baking, the photoresist exhibits adhesion problems and frequently delaminates from the surface during etching. Hard-baking is very similar to soft-baking and follows the same procedure. Load a wafer onto a *hotplate* for the desired temperature and time.

4. Etching the SiO₂:**(Check Parameters section for details)**

REPEAT: This step should be carried out by the lab TA for safety reasons. Begin by loading the wafers into a Teflon cassette with equal spacing between wafers. Using the handle, submerge the cassette in 6:1 *BOE* for the appropriate amount of time or until the exposed SiO₂ is completely removed. Once the etch is complete, remove the cassette and rinse the wafers by submerging them in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers.

5. Full Wafer Cleaning:**(Check Parameters section for details)**

REPEAT: The wafers need to be cleaned to remove photoresist, and any possible sources of contamination before being placed in a high temperature furnace.

Remove photoresist with a solvent clean. Begin by placing an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with *acetone* using the squirt bottle, follow with *methanol* and *isopropyl*. The acetone will remove the photoresist and the methanol and isopropyl will remove any acetone residue. Finish by rinsing the wafer in DI water and dry with a nitrogen gun. Pour the solvent waste into the *Solvent Waste Container*.

Remove possible sources of contamination and strip native oxide with an RCA clean. This step should be carried out by the lab TA for safety. Load the wafers into a Teflon cassette transfer the cassette between the RCA solutions until the cleaning is complete. Rinse the wafers and cassette in a bucket of DI water then pull each wafer and rinse and dry by hand.

5. Boron Diffusion:**(Check Parameters section for details)**

The goal of this diffusion is to create kilo-ohm piezoresistors. The diffusion is modeled as a solid-solubility-limited diffusion followed by several drive-in steps. The expected resistivity can be derived from this model and verified with the BORONPLUS data sheet.

REPEAT: To diffuse P-type (Boron) material, ramp the *Boron diffusion furnace* to 600°C and set the nitrogen flow. Remove the quartz boat with the solid, white, *BORONPLUS GS139 sources* already in place. Load the silicon wafers next to the sources into the quartz boat with the patterned side facing a source. Insert the quartz boat to the center of the furnace and ramp the furnace to the desired temperature. When the desired temperature is reached start the timer. After the allotted time, ramp the furnace down to 600°C, pull the quartz boat and remove the wafers and set them aside to cool.

Documenting, Cleaning & Oxidizing

Week 5

GOALS:

1. Take pictures using the microscope and digital camera
2. Strip the SiO₂ and BSG
3. Obtain 4-point probe measurements of the diffusion
4. RCA clean
5. Oxidation

EQUIPMENT:

- Optical Microscope
- CANON digital camera
- Teflon Cassette
- 6:1 BOE
- JANDEL 4-point Probe Station
- RCA clean tanks
- MODULAB Oxidation Furnace

PARAMETERS:

SiO₂ Etch Parameters* for 4,200-4,500Å thick SiO₂ layer

BOE concentration	SiO ₂ Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	5* (will need longer to remove BSG layer ~10-15min)	Shipley 1813 Photoresist

RCA Clean Parameters

Piranha Solution	Piranha Etch Time (minutes)	BOE solution	BOE Etch Time (seconds)	Ionic Clean	Ionic Clean Etch Time (minutes)
3:1 H ₂ O ₂ :H ₂ SO ₄	10	6:1	10	6:1:1 H ₂ O:H ₂ O ₂ :HCl	10

Oxidation Parameters

Temperature (°C)	Time (minutes)	Type (wet or dry)	N ₂ /O ₂ Flow	Bubbler Setting
1050	180	Wet	7/9	40

Methods:

1. Taking Pictures:

Use the optical microscope and digital camera to take a picture of the diffused resistors (shown in Figure 19)

2. Stripping the SiO_2 :

(Check *Parameters* section for details)

The wafer surface needs to be prepared for the next oxidation run.

REPEAT: This step should be carried out by the lab TA for safety reasons. Load the wafers into a Teflon cassette and submerge in BOE until the SiO_2 and BSG is completely removed. When finished rinse and dry with DI water and nitrogen

The BSG etches at a slower rate than the thermal SiO_2 so the amount of time to completely clear the wafer surface will take longer than the previous SiO_2 etch. To check that the surface is clear of oxide, run the wafer under DI water, if the water beads up and rolls off, the surface is clear, if not there is still some remaining oxide. This phenomenon occurs due to the hydrophobic nature of silicon and hydrophilic nature of silicon dioxide.

The diffused regions should be visible to the naked eye, and most likely brownish grey in color (see Figure 21). If the regions are bluish, BSG is still present, and the wafers need to continue etching.

3. Diffusion Measurements:

There is another diffusion test region adjacent to the other. Use the 4-point probe to measure the sheet resistivity of the diffusion. The sheet resistivity of this region should correspond with data sheet for BORONPLUS sources (data sheet in previous section). Also measure and record the old (diffused contacts) test region. The two thermal cycles (oxidation and diffusion) will have diffused the dopant further into the wafer which should be observed as an increase in the sheet resistivity.

See equipment operations manual for details on using the 4-point probe.

Figure 19 An example of a microscope picture that should be taken to document the progress of the wafers. Shown are fully diffused piezoresistors

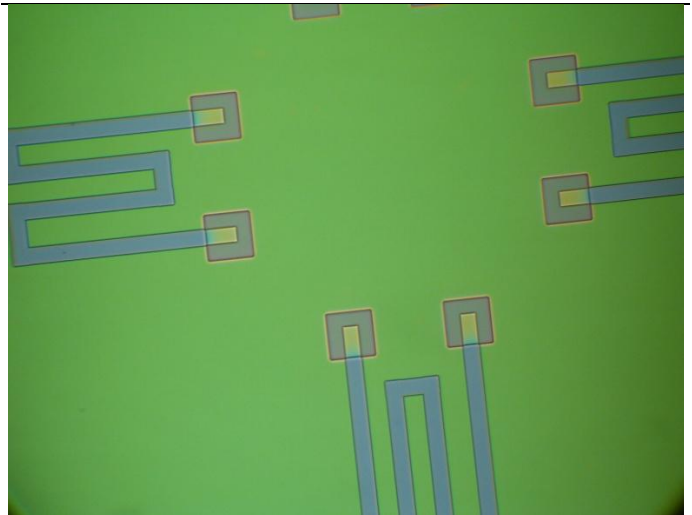


Figure 20 The surface of the wafer after the SiO_2 is removed. The features will be hard to see with the naked eye and may be difficult to find with the microscope.

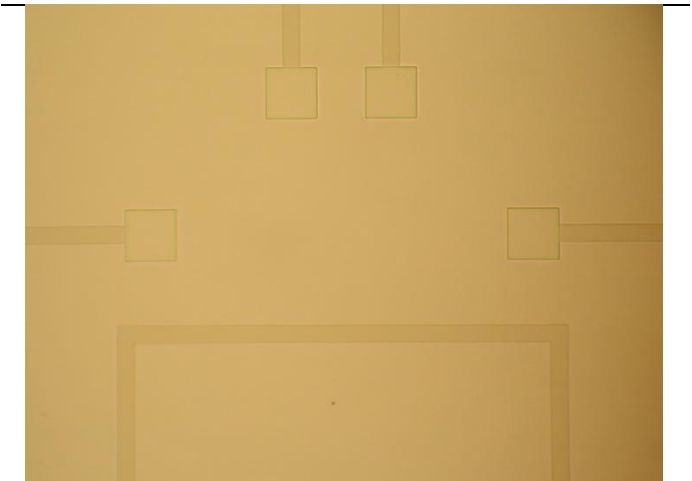


Figure 21 A student using the JANDEL 4-point probe to document the sheet resistivity of the second diffusion.



4. RCA Cleaning:

(Check Parameters section for details)

REPEAT: To remove possible sources of contamination a modified RCA clean is performed. The RCA clean consists of rinsing the wafers in three chemical solutions: Piranha etch, BOE, Ionic clean.

This step should be carried out by the lab TA for safety. Load the wafers into a *Teflon cassette* transfer the cassette between the RCA solutions until the cleaning is complete. Rinse the wafers and cassette in a bucket of DI water then pull each wafer and rinse and dry by hand.

5. Oxidation: Growing SiO₂

(Check Parameters section for details)

The goal of the third oxidation run is slightly different from the first two. Its purpose is to create a thick, 0.8-1 μ m, layer of SiO₂ to mask the bulk silicon etch and final plasma release etch. It is important that the wafer surface be clean of any impurities before the oxidation to ensure the highest quality film and avoid pinholes.

REPEAT: To oxidize, insert the wafers into oxidation furnace using the quartz rod and quartz boat. There should be two dummy wafers, one at the front of the boat and another at the rear, in order to maintain uniformity across the boat. Ramp the furnace to 600°C before the removing the quartz boat and loading the wafers. Before the furnace reaches 400°C, turn on the nitrogen to purge the furnace. Also, set the potentiometer on the bubbler if performing a wet oxidation (which we are). Once the wafers are in place at the center of the furnace, ramp the furnace to the desired temperature. When the desired temperature is reached start the timer, stop the nitrogen flow and turn on the oxygen. After the allotted time, ramp the furnace down to 600°C, pull the boat, remove the wafers and set them aside to cool.

GOALS:

1. Measure the thickness of the SiO₂ layer with the Nanospec
2. Aluminum PVD
3. Photolithography (Mask #3 Alignment Markers)
4. Hardbake
5. Aluminum Etch

EQUIPMENT:

- Nanospec
- MODULAB Physical Vapor Deposition (PVD) system
- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- PAE etchant
- Teflon or Pyrex evaporating dish

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5000	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #1)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm ²)	UV Dose (J/cm ²)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Hard-bake Parameters

Harbake Program	Temperature (°C)	Time (minutes)
#2	115	2

Aluminum Etch Parameters* for 0.5-1um thick aluminum layer

Etchant	Approx. Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
PAE	350	15*	Shipley 1813 Photoresist

Methods:

1. Measuring the SiO_2 thickness:

Measure the thickness of the silicon dioxide at several different points on the wafer using the *Nanospec*. For reference, the *Nanospec* prompts for measuring SiO_2 thickness are:

Is wavelength 480nm? Y (if not, type N and value)
Data bank option? N
Refr index option? N
Switch to printer? N
Enter film type: 1-SiO2
Enter obj lens: 1 = 10x

2. Aluminum PVD:

The goal of the aluminum evaporation is to create a thin film of aluminum on the topside of the wafer. The aluminum will be patterned with alignment marks to allow for backside alignment. Evaporation is accomplished with the *MODULAB PVD system*. See the *MODULAB PVD operations manual* for more information.

Approximately 30 cm^2 of aluminum should be evaporated. This will provide roughly a $0.3\text{-}0.6\mu\text{m}$ film of aluminum, enough for backside alignment markers. If time allows, verify the film thickness by taking measurements with the profilometer.

Figure 22 Wafers being loaded into the aluminum physical vapor deposition system.



3. Photolithography with Mask #3

(Alignment Markers):

Spin-coating & Soft-baking

(Check Parameters section for details)

Mask #3 contains the alignment marks needed to perform backside alignment.

REPEAT: Begin by using the *BREWER spin-coater* to spin a thin film of *SHIPLEY 1813* photoresist onto the topside of the wafer. Next, transfer the wafer to the adjacent hotplate and soft-bake to remove solvents and harden the resist. If done correctly, the layer of photoresist should have minimal streaks and blotches. The film will be barely visible to the naked eye. If there are a large number of defects, solvent clean, dehydrate, and try re-spinning more photoresist.

Figure 23 Students and professor looking on as a wafer is aligned and exposed at the ABM contact aligner.



Methods:

3. Photolithography with Mask #3

(Alignment Markers):

Exposure & Development

(Check Parameters section for details)

REPEAT: Load Mask #3 onto the ABM contact-aligner mask stage. Turn the mask-vac on and raise the mask stage. Carefully, load the wafer onto the substrate chuck and orient it such that the <110> plane (wafer flat) is to the left and running straight up and down. Turn on the substrate-vac to lock the wafer in place and lower the chuck to avoid hitting the contact mask. Next, lower the mask stage and raise the substrate chuck up to meet the mask, fringe lines will become visible as the wafer and mask come into contact. Align the mask to the wafer using the markers on the sides of the wafer (see *Alignment System* at the end of the manual for details on the alignment marks). Turn on the contact-vac to remove any air gap between mask and wafer. Adjust the exposure time and channel setting then expose. Remove the wafer by turning off the contact-vac, lowering the substrate chuck, raising the mask frame, and turning off the substrate-vac. Transfer the wafer to a dish of MF319 developer (a faint outline of the features can be seen at this point), submerge the wafer in MF319 and gently swirl for 30-60 seconds until the exposed resist is completely dissolved. If done correctly there should be no photoresist left in the diffusion contact regions. If there is, resubmerge the wafer in the MF319 developer for additional time. If unsuccessful, use a solvent clean to strip the photoresist, dehydrate and re-spin again. When finished, pour the used MF319 into the MF319 waste container located under the solvent bench next to the photoresist.

4. Hard-baking:

(Check Parameters section for details)

Remove any remaining solvents and/or water from the resist by loading a wafer onto a hotplate for the desired temperature and time.

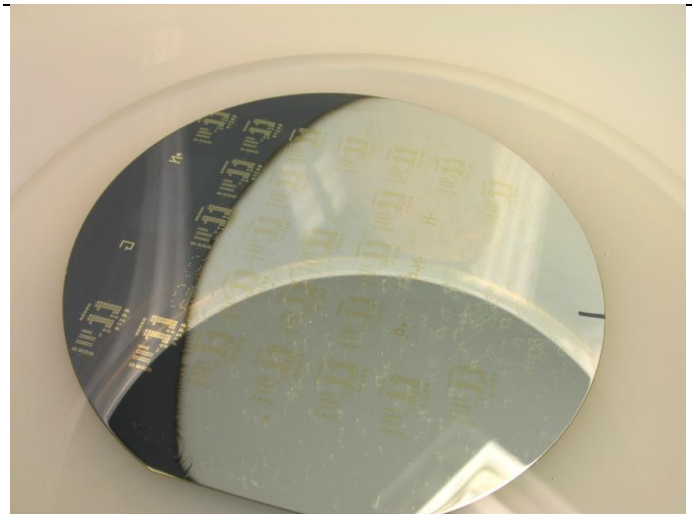
5. Etching Aluminum:

(Check Parameters section for details)

The exposed aluminum is removed in *PAE etchant* (Phosphoric Acid Etch) one wafer at a time. The PAE contains three acids: phosphoric, acetic, and nitric. It etches aluminum at approximately 350Å/min and is highly selective to aluminum compared to photoresist.

Begin by pouring a small amount of PAE into a *Pyrex or Teflon evaporating dish*. Submerge a wafer and gently swirl until the exposed aluminum has been etched. A visible etch front will move across the wafer as the aluminum is removed (**see Figure 24**). The etch will take between 10-15 minutes to complete.

Figure 24 Aluminum being etched in PAE. Note the etch front moving from left to right. This is a result of a varying thickness in the aluminum created during the evaporation



Backside Alignment & Bulk Si Etch

Week 7

GOALS:

1. Solvent Clean
2. Photolithography (Mask#4 Backside Etch)
3. Etch SiO₂
4. Solvent Clean
5. Aluminum Strip
6. Start Bulk Silicon Etch in TMAH
7. Monitor etch depth/rates with profilometer

EQUIPMENT:

- Acetone, Methanol, Isopropyl
- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- PAE etchant
- Hotplate
- 2.5L Pyrex Beaker
- 25% TMAH
- AMBIOS profilometer
- 6:1 BOE
- Teflon Cassette

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5000	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #1)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm ²)	UV Dose (J/cm ²)	Exposure Time (seconds)	Development Time (seconds)
Away	Right	30	~135	4.5	30-60

Hard-bake Parameters

Harbake Program	Temperature (°C)	Time (minutes)
#2	115	2

SiO₂ Etch Parameters* for 7000Å thick SiO₂ layer

BOE concentration	SiO ₂ Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	7-8*	Shipley 1813 Photoresist

Aluminum Etch Parameters* for 0.5-1um thick aluminum layer

Etchant	Approx. Etch Rate (nm/min)	Approx. Etch Time (minutes)	Etch Mask
PAE	400	15*	Shipley 1813 Photoresist

Bulk Silicon Etch Parameters *for multiple wafer etch setup

Etchant	Hotplate Temperature* (°C)	Solution Temperature (°C)	Hotplate Spinner Speed* (RPM)	TMAH fill line* (mL)	Etch Mask
25% TMAH	135	85-90	1000	1900	SiO ₂

Methods:**1. Solvent Clean:**

REPEAT: To remove photoresist with a solvent clean, begin by placing an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with *acetone* using the squirt bottle and follow with *methanol* and *isopropyl*. The acetone will remove the photoresist and the methanol and isopropyl will remove any acetone residue. Rinse the wafers in DI water and dry with a nitrogen gun. When finished pour the solvent waste into the *Solvent Waste Container*.

2. Photolithography with Mask #4**(Backside Etch):****Spin-coating & Soft-baking****(Check Parameters section for details)**

This photolithography step is slightly different from the previous steps. Mask #4 defines the silicon bulk etch for the backside of the wafer. Therefore, begin by spinning *SHIPLEY 1813* photoresist onto the backside of the wafer and performing a soft-bake.

2. Photolithography with Mask #4**(Backside Etch):****Exposure & Development****(Check Parameters section for details)**

Load Mask #4 onto the *ABM contact-aligner* mask stage. Turn the mask-vac on and raise the mask stage. Carefully, load the wafer onto the substrate chuck, with backside pointed upward, oriented such that the <110> plane (wafer flat) is to the right and running straight up and down. This is necessary to ensure that the topside features align with the backside features. Turn on the substrate-vac to lock the wafer in place and lower the chuck to avoid hitting the contact mask. Next, lower the mask stage and raise the substrate chuck up to meet the mask, fringe lines will become visible as the wafer and mask come into contact.

Next to the substrate chuck are two snake-like fiber optic cables. These need to be secured to the right and left sides of the chuck. Beneath the ABM mask-aligner there are two IR light sources (**see Figure 25**). Turn both to 100% power. Continued...

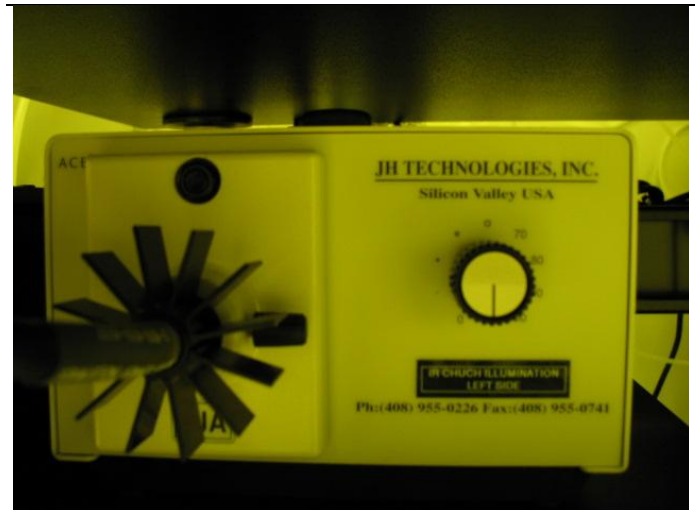
**Photolithography with Mask #4
Continued...**

If setup properly, the IR sources will shine light through the silicon wafer and appear as white light in cameras. The aluminum alignment markers on the topside of the wafer (which is facing downward on the chuck) effectively block the IR light from passing through the silicon and create alignment shadows. These shadows must be aligned to Mask #4. Align by adjusting focal depths and zoom factors.

After aligning the mask and wafer, adjust the exposure time and channel setting and expose. Remove the wafer by turning off the contact-vac, lowering the substrate chuck, raising the mask frame, and turning off the substrate-vac. Transfer the wafer to a dish of *MF319 developer*, submerge the wafer in MF319 and gently swirl for 30-60 seconds until the exposed resist is completely dissolved. When finished, pour the used MF319 into the MF319 waste container located under the solvent bench next to the photoresist.

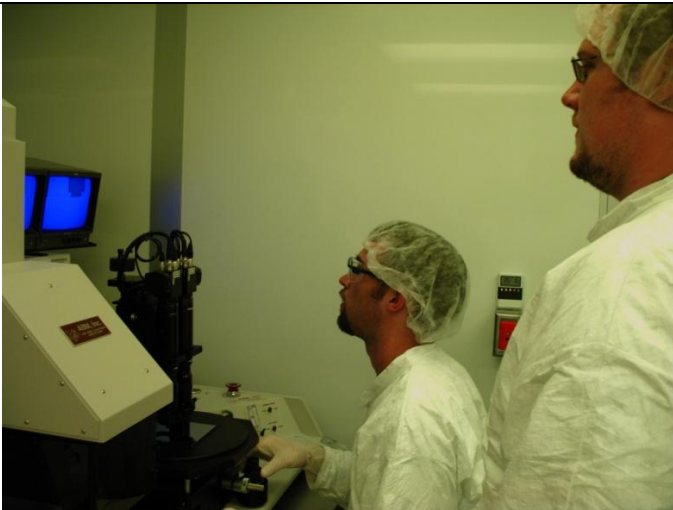
Be aware that the exposed aluminum on the topside will react with the MF319 and inhibit the development. Therefore development may take longer than expected. If necessary replace MF319 solution every 1-2 wafers.

Figure 25 The infrared light sources used for backside alignment located beneath the mask aligner



Methods:

Figure 26 Two students using the ABM mask aligner to perform the backside alignment,



2. Hard-baking:

(Check Parameters section for details)

REPEAT: Remove any remaining solvents and/or water from the resist by loading a wafer onto a hotplate for the desired temperature and time.

2. Spin-coating, Soft-baking & Hard-baking Again...

(Check Parameters section for details)

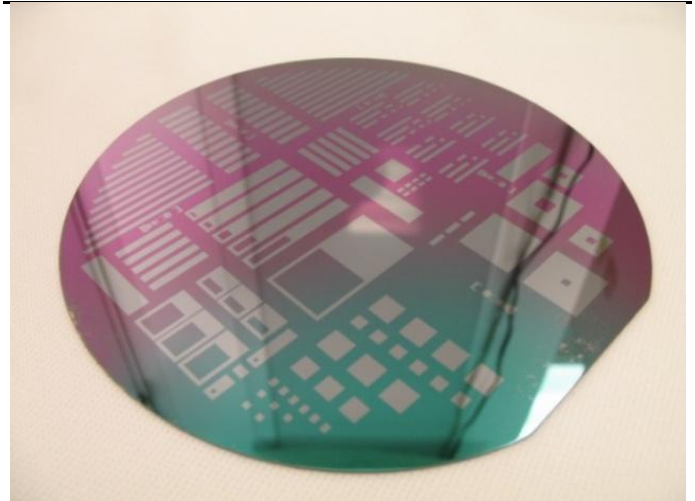
It is necessary to spin photoresist onto the topside of the wafer to avoid etching the exposed silicon dioxide. Use the BREWER spin-coater to spin a thin film of *SHIPLEY 1813* onto the topside. Perform a soft-bake and hard-bake to harden the photoresist. Note, if a large ramp acceleration is used for this step, photoresist tends to splash onto the backside. The photoresist splash is usually limited to the edges of the wafer but can interfere with the patterned resist. It is recommended that the ramp speed be slowed for this spin-coat step.

3. Etching the SiO_2 :

(Check Parameters section for details)

REPEAT: This step should be carried out by the lab TA for safety reasons. Load the wafers into a *Teflon cassette* with equal spacing between wafers. Using the handle, submerge the cassette in BOE for the appropriate amount of time or until the exposed SiO_2 is completely removed. Once the etch is complete, remove the cassette and rinse the wafers by submerging them in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers.

Figure 27 The backside of a wafer with patterned SiO_2 layer prior to the silicon bulk etch.



4. Solvent Clean:

REPEAT: To remove photoresist with a solvent clean begin by placing an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with *acetone* using the squirt bottle, follow with *methanol* and *isopropyl*. The acetone will remove the photoresist and the methanol and isopropyl will remove any acetone residue. Rinse the wafers in DI water and dry with a nitrogen gun.

5. Stripping the Aluminum:

(Check Parameters section for details)

The aluminum that was used for the topside alignment marks is no longer necessary so it needs to be removed. Remove the aluminum by etching a wafer in *PAE etchant*. The etch will take between 10-15 minutes to completely remove the aluminum

Methods:

6. Bulk Silicon Etch in TMAH: (Check Parameters section for details)

The goal of the bulk silicon etch is to create the thin silicon membranes for the pressure sensors and accelerometers. The etching should take place over a 1-2 day time span, depending on start and stop times. The total etch time will vary between 15-18 hours. It is critical the etch is stopped before completely etching through the wafer, otherwise, subsequent photolithography steps will be nearly impossible. **The etch will be complete when the silicon is approximately $30\mu\text{m}$ thick.**

In the past, there have been two successful etching setups: one for multiple wafers and the other for a single wafer (**Figure 30**). The setup for a multiple-wafer etch is shown in **Figure 28** and will be used to save time.

To prepare the etch, insert a *Teflon cassette* and magnetic stirrer into a *2.5L Pyrex beaker*. Place the beaker onto a *hotplate* and fill with enough *25% TMAH* to completely submerge the Teflon cassette. Set the spinner and temperature to the desired settings. Meanwhile remove any native oxide from the wafers by dipping them into *6:1 BOE* for 10 seconds. When the solution reaches its equilibrium temperature, load the wafers into the Teflon cassette, cover the beaker with a watch glass (allow room for gases to escape) and start the timer. Note the TMAH will take roughly 45-60 minutes to reach equilibrium temperature.

Figure 30 An alternate setup for bulk silicon etching a single wafer. A single wafer sits atop a magnetic spinner in an evaporating dish with a small amount of 25% TMAH. This method uses considerably less TMAH but is only effective for a single etch.

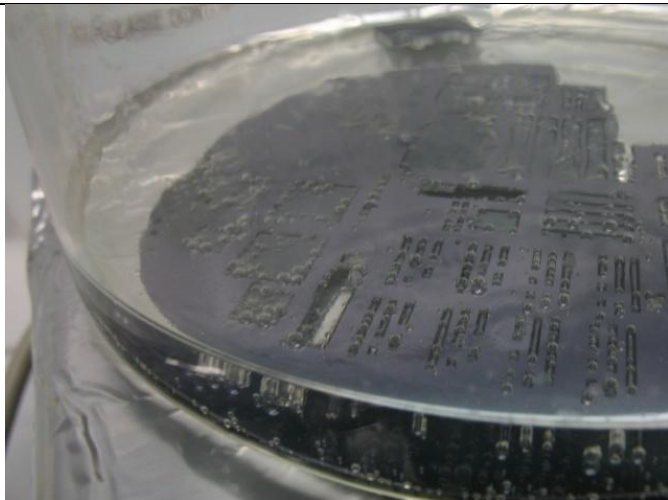


Figure 28 The bulk silicon etch setup for a multiple wafer etch. Note the 2.5L beaker is filled with 25% TMAH and loaded with Teflon cassette and magnetic spinner.

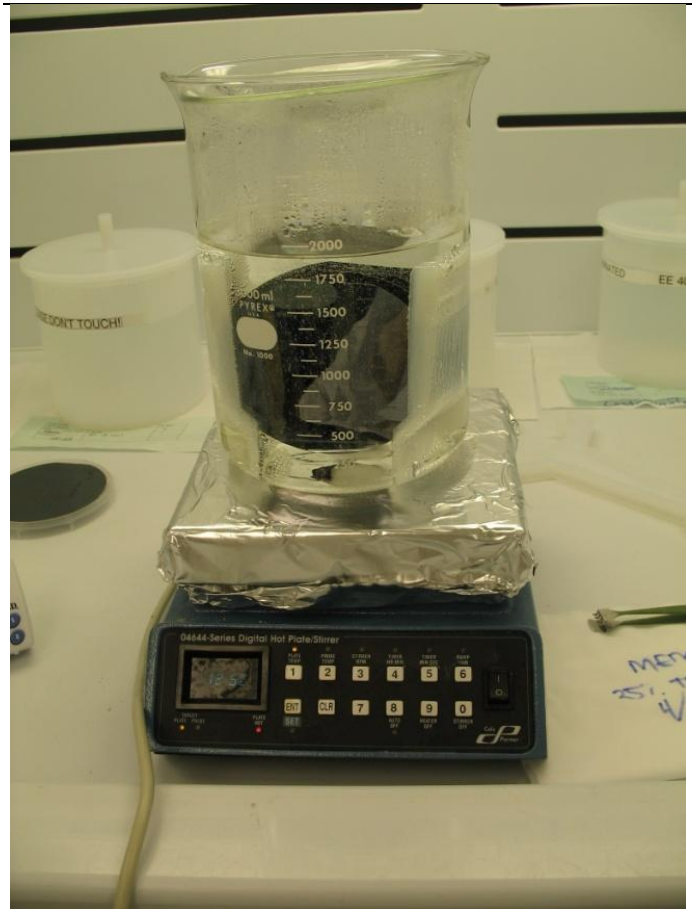
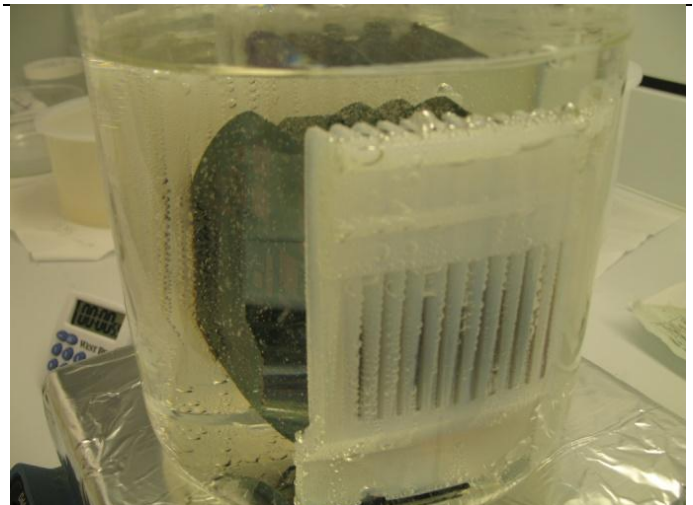


Figure 29 A close-up view of the bulk silicon etch setup for multiple wafers.



Methods:

7. Checking the Etch Depth/Rate:

To ensure the etch is working properly, pull the wafers periodically (every 4-6 hours) to monitor the etch rate and etch depth. Upon removing the wafers from the etch tank, rinse thoroughly with DI water and dry with a nitrogen gun.

Check the etch depth by taking measurements with the *AMBIOS Stylus Profilometer*. Place the wafer on the stage and perform measurements at multiple locations around the wafer. Observe the varying etch depths and associated etch rates. Note that the AMBIOS profilometer has a range of 400 μm , so there will come a point when depth measurements will need to be made with the microscope and micrometer focus adjustment (see following week's instructions).

Although TMAH is highly selective to silicon it will still etch the exposed oxide. The etch rate of the oxide is very slow but still observable. Measure the etch rate of the silicon dioxide by taking thickness measurements with the *Nanospec*. If the SiO_2 layer becomes too thin the underlying features could be damaged, so be sure to monitor it often.

The etch rate of the SiO_2 is dependent on the amount of dissolved silicon in the solution, as a result, the longer the wafers are etched and as more water evaporates from the solution, the faster the SiO_2 will be etched.

Week 7

Figure 31 Two students operating the AMBIOS profilometer to monitor the etch depths of the bulk silicon etch.



Bulk Etch, Bonding & Mask#3 Again? Week 8

GOALS:

1. Finish Bulk Silicon Etch
2. Determine final etch depth and average etch rate with profilometer, microscope & Nanospec
3. Take pictures using the microscope and digital camera
4. Wafer Bonding
5. Photolithography (Mask #3/5 Alignment markers)
6. Hard-bake
7. Etch SiO₂

EQUIPMENT:

- Hotplate
- 2.5L Pyrex Beaker
- 25% TMAH
- AMBIOS profilometer
- Nanospec
- Optical microscope
- CANON Digital Camera
- WAFERGRIP adhesive
- Single-side polished Handle Wafers
- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- 6:1 BOE
- Teflon Cassette

PARAMETERS:

Bulk Silicon Etch Parameters **for multiple wafer etch setup*

Etchant	Hotplate Temperature* (°C)	Solution Temperature (°C)	Hotplate Spinner Speed* (RPM)	TMAH fill line* (mL)	Etch Mask
25% TMAH	135	85-90	1000	1900	SiO ₂

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5000	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #1)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm ²)	UV Dose (J/cm ²)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Hard-bake Parameters

Harbake Program	Temperature (°C)	Time (minutes)
#2	115	2

SiO₂ Etch Parameters ** for 7000Å thick SiO₂ layer*

BOE concentration	SiO ₂ Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	7-8*	Shipley 1813 Photoresist

Methods:

**1. Finish Bulk Silicon Etch in TMAH:
(Check Parameters section for details)**

Continue etching the wafers in the heated 25% TMAH bath until the final etch depth has been reached e.g. if the starting wafer thickness was $475 \pm 25 \mu\text{m}$, then the final etch depth should be roughly 430-450 μm . Only pull the wafer early if a large number of pinholes (see **Figure 33**) start to form. The pinholes result from defects in the SiO_2 , allowing the TMAH to attack the underlying silicon and etch through the wafer from both sides. A large number of pinholes will severely limit the ability to clean, etch or spin on photoresist during the subsequent process steps (see **Figure 34**).

Determining when the etch is complete is a trade-off between quality (i.e. pinholes, etch uniformity) and etch depth. If the wafer is under-etched, the membranes will be too thick and problems will arise during the plasma release etch. If too many pinholes begin to form the photolithography and SiO_2 etching steps will be very difficult to perform. For this reason, the bulk silicon etch is the most critical step in the process and the most difficult to achieve good results.

When the bulk silicon etch is complete, dehydrate the wafers for several hours (overnight is optimal), by placing the wafers in an oven or on a hotplate between 115-150°C. If not properly dehydrated, adhesion problems will arise during the following photolithography steps.

Figure 36 The backside of a wafer after completing the bulk silicon etch. Note the geometries of the proof masses have changed due to the anisotropy of the etch.

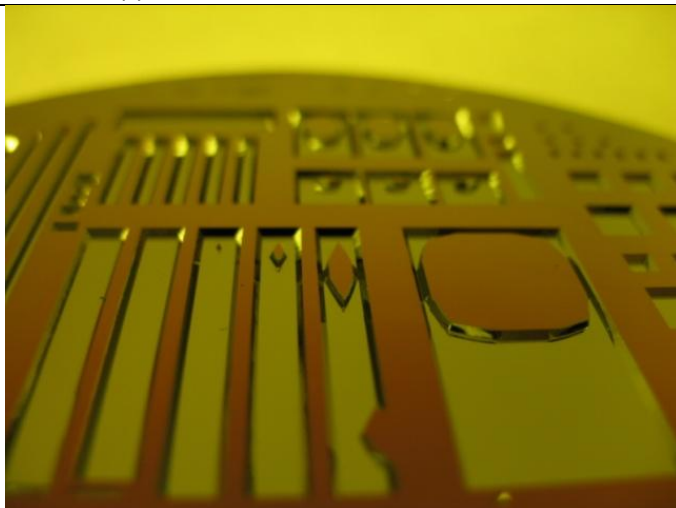


Figure 32 The backside of a wafer that has been overetched in 25% TMAH. Note the non-uniform etch depth.

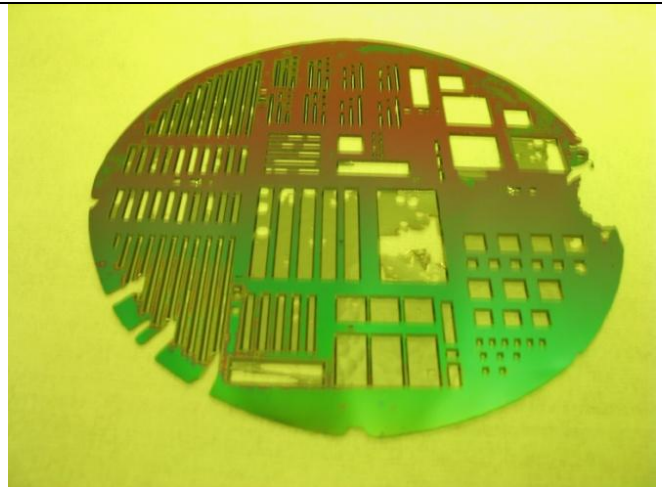


Figure 33 The topside of a wafer exhibiting a large amount of pinholes due to imperfections in the protecting SiO_2 layer. The pinholes can be easily seen by holding an etched wafer up to a light source.

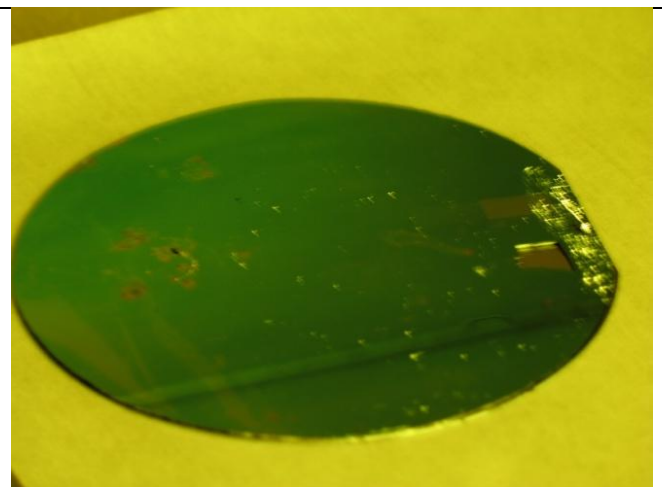
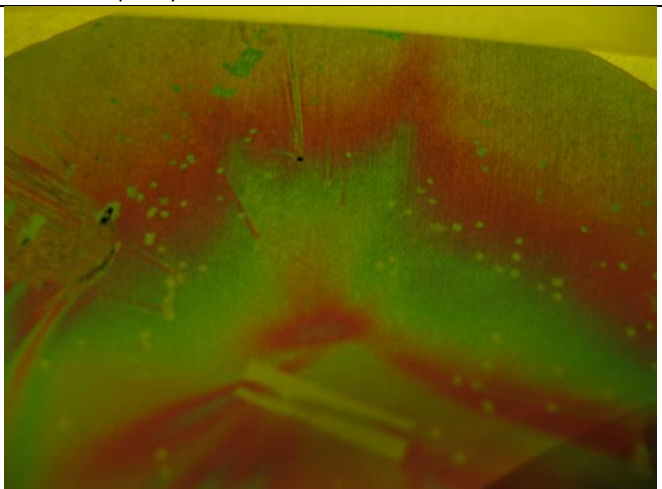


Figure 34 The effect of pinholes on the spin coating of photoresist. The pinholes make the subsequent photolithography steps nearly impossible. Not only do they interfere with the vacuum, but also allow chemicals to seep through the wafer and create poor adhesion and feature quality.



Methods:

2. Measuring Final Depth & SiO₂:

Measure the completed etch-depth using the *optical microscope*. To measure the depth, use the 20x lens, and focus the wafer on the surface of the backside, noting the starting point on the micrometer focus knob. Adjust the focus until the etched plane becomes clear, counting the number of ticks between the surface and etched plane, this will be the etch depth within $\pm 5\mu\text{m}$.

Also measure and record the final thickness of the SiO₂, on both the top and backsides of the wafer. The final thickness should be less than 1000Å from the original thickness. Roughly 6000-7000Å of SiO₂ is needed to mask the release etch.

3. Documenting & Taking Pictures:

Use the *optical microscope* and *CANON digital camera* to document the wafer after completing the bulk silicon etch. Take pictures of etched features (see **Figure 36 or 39**) and defects that have been exaggerated by the etch (see **Figure 37**).

Figure 39 Another etched feature on the backside of the wafer.

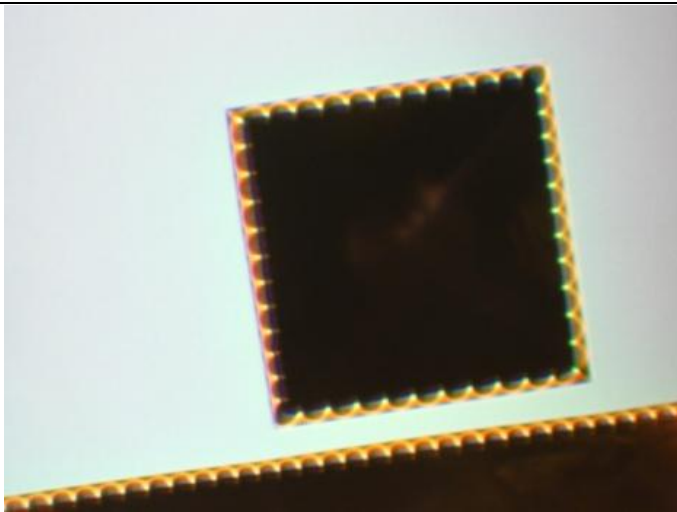


Figure 37 A close up of defects on the topside of the wafer after bulk etching. Holes in the silicon dioxide have allowed TMAH to reach the underlying silicon and etch these small imperfections.

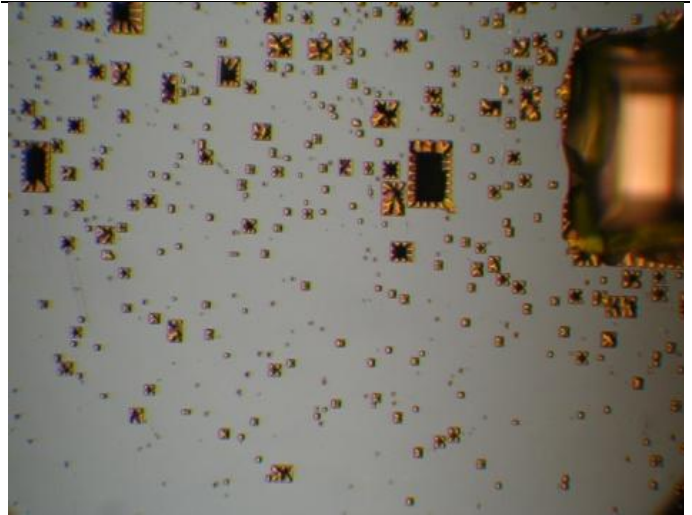
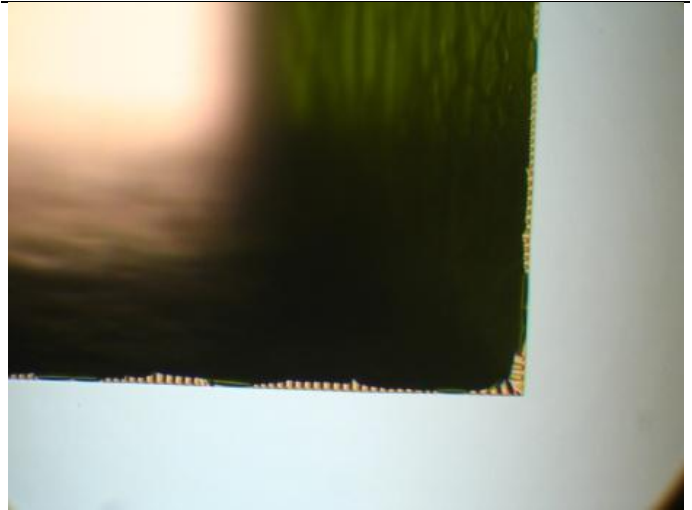


Figure 38 A dose-up of an etched features on the backside of the wafer. Note the fringe pattern around the perimeter from lateral etching.



Methods:**4. Wafer Bonding:**

The goal of the wafer bonding is to create a temporary surface on the backside for handling and processing the etched wafer. Without a bonded handle wafer, the vacuum needed for spin-coating and aligning could not be achieved. For this lab, a product called *WAFERGRIP* (see **Figure 40**) is used to achieve a temporary bond between the etched wafer and a blank single-side polished handle wafer.

To bond, begin by setting a hotplate to 140°C. Place the handle wafer on the hotplate and the *WAFERGRIP adhesive* atop the handle wafer. Let the pair heat-up then place the etched wafer, backside (etched-side) down on the adhesive. Press the handle and etched wafers firmly together, but be careful, the etched wafer is very fragile and can easily crack. Once secured, set the bonded wafers aside to cool. For more information, consult the *WAFERGRIP* datasheet.

Figure 40. The *WAFERGRIP* adhesive used for the temporary wafer bonding.

**5. Photolithography with Mask #3/5**

(Alignment Markers):

Spin-coating & Soft-baking

(Check Parameters section for details)

From this point on, all photolithography will take place on the topside of the wafer.

The reason this mask is repeated is due to a flaw in the alignment system. The alignment markers were designed to be used in sequential order, but because of fabrication process, the markers etched in the aluminum were removed. Therefore, the goal of this step is to pattern Mask #3 into the SiO_2 so the final two masks can be aligned.

Use the BREWER spin-coater to spin a thin film of SHIPLEY 1813 onto the topside of the wafer, and perform a soft-bake to harden the photoresist.

5. Photolithography with Mask #3/5

(Alignment Markers):

Exposure & Development

(Check Parameters section for details)

Load Mask #3/5 onto the *ABM contact-aligner* mask stage and align the mask to the wafer (see *Alignment System* section), using the standard procedure. Transfer the wafer to a dish of *MF319* and develop the exposed resist for 30-60 seconds. When finished, pour the used *MF319* into the *MF319* waste container located under the solvent bench next to the photoresist.

6. Hard-baking:

(Check Parameters section for details)

REPEAT: Remove any remaining solvents and/or water from the resist by loading a wafer onto a *hotplate* for the desired temperature and time.

Methods:

Week 8

7. Etching the SiO_2 :

(Check Parameters section for details)

REPEAT: This step should be carried out by the lab TA for safety. Load the wafers into a Teflon cassette with equal spacing between wafers. Using the handle, submerge the cassette in BOE for the appropriate amount of time or until the exposed SiO_2 is completely removed. Once the etch is complete, remove the cassette and rinse the wafers by submerging them in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers.

Vias & Aluminum Evaporation

Week 9

GOALS:

1. Solvent Clean
2. Photolithography (Mask #6 Release & Via Etch)
3. Hard-bake
4. Etch SiO₂
5. Solvent Clean
5. Aluminum PVD

EQUIPMENT:

- Acetone, Methanol, Isopropyl
- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- 6:1 BOE
- Teflon Cassette
- MODULAB Physical Vapor Deposition system
- Hotplate

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5000	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #1)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm ²)	UV Dose (J/cm ²)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Harbake Parameters

Harbake Program	Temperature (°C)	Time (minutes)
#2	115	2

SiO₂ Etch Parameters* for 7000Å thick SiO₂ layer

BOE concentration	SiO ₂ Etch Rate (Å/min)	Approx. Etch Time (minutes)	Etch Mask
6:1	900	7-8*	Shipley 1813 Photoresist

Methods:

1. Solvent Clean:

REPEAT: Place an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with *acetone* using the squirt bottle and follow with *methanol* and *isopropyl*. Rinse the wafers in DI water and dry with a nitrogen gun.

2. Photolithography with Mask #6

(Release & Via Etch):

Spin-coating & Soft-baking

(Check Parameters section for details)

Mask #6 contains the features for the release-etch and vias. The vias connect the aluminum pads (next week) to the diffused contacts of the piezoresistors. The release etch defines the geometries of the cantilever accelerometers

Use the BREWER spin-coater to spin a thin film of SHIPLEY 1813 onto the topside of the wafer, and perform a soft-bake to harden the photoresist.

2. Photolithography with Mask #6

(Release & Via Etch):

Exposure & Development

(Check Parameters section for details)

Load Mask #6 onto the *ABM contact-aligner* mask stage and align the mask to the wafer (see *Alignment System* section). Transfer the wafer to a dish of *MF319* and develop the exposed resist for 30-60 seconds. When finished, pour the used *MF319* into the *MF319* waste container located under the solvent bench next to the photoresist.

3. Hard-baking:

(Check Parameters section for details)

This hard-bake tends to be critical to achieve a good SiO_2 etch profile (see **Figures 40-44**). Remove any remaining solvents and/or water from the resist by loading a wafer onto a *hotplate* for the desired temperature and time.

Figure 40 Vias etched into the silicon dioxide. Note the fringe pattern indicating a thickness gradient and sloping sidewalls. This was caused by the photoresist peeling up from the patterned regions allowing the etchant to attack the surrounding area.

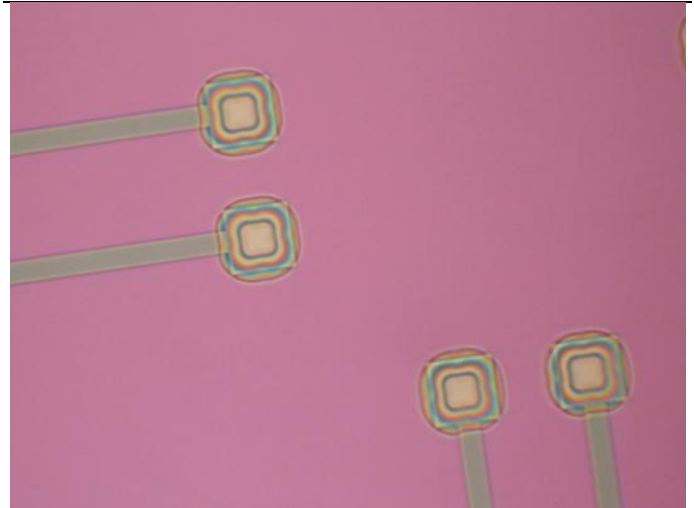


Figure 41 A good-quality etch of the vias and release areas. The edges are sharp and straight and the piezoresistor is well-aligned

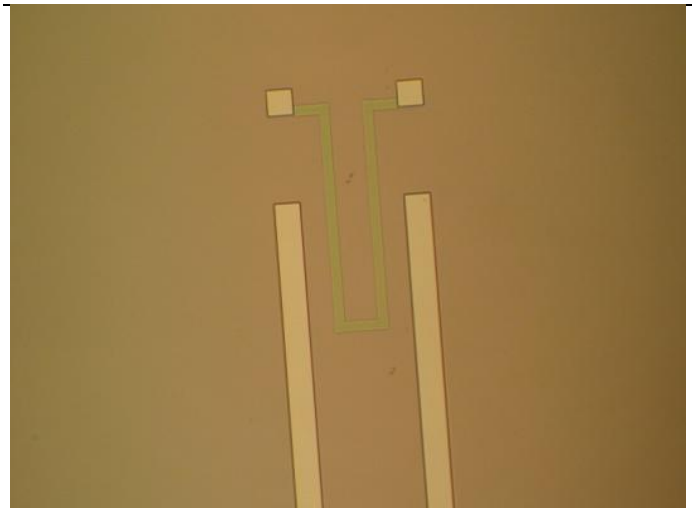
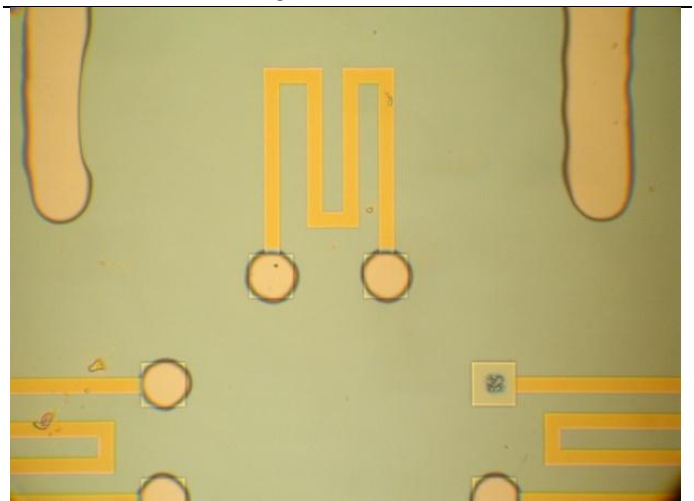


Figure 42 An example of a poor-quality via etch due to photoresist adhesion problems and micromasking. The etched features are not well-defined and one feature (bottom-right) has not been entirely etched due to micromasking.



Methods:

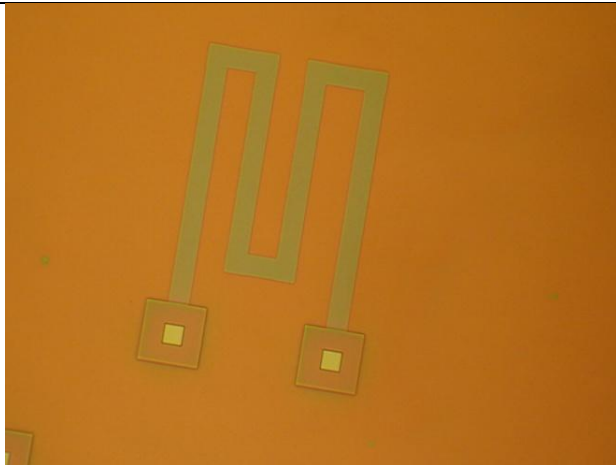
4. Etching the SiO_2 :

(Check Parameters section for details)

This etch step tends to produce mixed results. In some instances the etch is clear and well-defined, in others, it is rough and un-manageable. The reason for the low-quality etch is not fully understood but may stem from inadequate wafer dehydration or a large number of pinholes and defects in the oxide. Despite the quality, in most cases the fabrication can continue and yield decent devices.

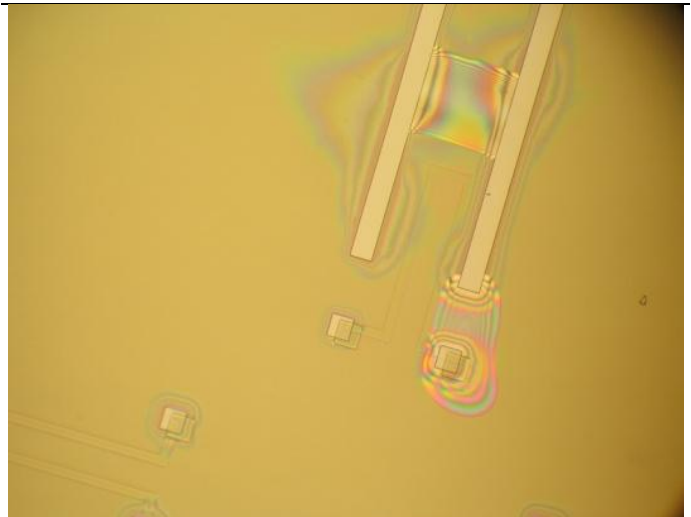
REPEAT: This step should be carried out by the lab TA for safety. Load the wafers into a Teflon cassette with equal spacing between wafers. Using the handle, submerge the cassette in BOE for the appropriate amount of time or until the exposed SiO_2 is completely removed. Once the etch is complete, remove the cassette and rinse the wafers by submerging them in a bucket of DI water. Pull the cassette from the rinse bucket and rinse and dry individual wafers.

Figure 43 Another good-quality etch of the vias. The vias are centered and the etch is well-defined.



Week 9

Figure 44 Another poor quality via etch. The color gradients indicate that some of the photoresist has delaminated causing the underlying SiO_2 to be etched.



5. Solvent Clean:

REPEAT: Place an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with acetone using the squirt bottle and follow with methanol and isopropyl. Rinse the wafers in DI water and dry with a nitrogen gun. When finished pour the solvent waste into the *Solvent Waste Container*.

6. Aluminum PVD:

The goal of the aluminum evaporation is to create a thin film of aluminum on the topside of the wafer. The aluminum will be patterned with Mask #7 to create electrical contact pads for characterizing the finished devices. The evaporation is accomplished with the *MODULAB PVD system*. See the *MODULAB PVD operations manual* for more information.

Approximately $40\text{-}50\text{ cm}^2$ of aluminum should be evaporated. This will provide roughly $0.5\text{-}0.7\mu\text{m}$ of aluminum on the wafer surface. If time allows, verify the film thickness by taking measurements with the profilometer

Aluminum Pads, De-bond & Anneal

Week 10

GOALS:

1. Photolithography (Mask #7)
2. Aluminum etch
3. Hard-bake
4. Solvent clean
5. Take pictures with microscope and camera
6. Remove handle wafer
7. Anneal

EQUIPMENT:

- Acetone, Methanol, Isopropyl
- BREWER spin-coater and hotplate
- SHIPLEY 1813 positive photoresist
- ABM Contact Mask Aligner
- MF 319 developer
- PAE etchant
- Microscope
- CANON Digital Camera
- SVC-175
- Hotplate
- Evaporating Dish
- Boron Diffusion Furnace

PARAMETERS:

Spin-coat & Soft-bake Parameters

Spin Program	Speed (RPM)	Time (seconds)	Ramp (RPM/s)	Dispense Type (automatic or manual)	Softbake Program	Temperature (°C)	Time (minutes)
#9	5000	30	20000	Manual (static)	#2	115	2

Exposure & Development Parameters (MASK #1)

Mask Orientation (writing toward or away from user)	Wafer Orientation (flat to the left or the right)	UV Intensity Channel B (mW/cm ²)	UV Dose (J/cm ²)	Exposure Time (seconds)	Development Time (seconds)
Away	Left	30	~135	4.5	30-60

Harbake Parameters

Harbake Program	Temperature (°C)	Time (minutes)
#2	115	2

Aluminum Etch Parameters* for 0.5-1um thick aluminum layer

Etchant	Approx. Etch Rate (nm/min)	Approx. Etch Time (minutes)	Etch Mask
PAE	400	15*	Shipley 1813 Photoresist

Anneal Parameters

Furnace	Temperature (°C)	N ₂ Flow	Time (min)
Boron Diffusion Furnace	450	7	45

Methods:

1. Photolithography with Mask #7

(Aluminum Contacts):

Spin-coating & Soft-baking

(Check Parameters section for details)

The goal of the final photolithography step is to create the aluminum contact pads. Mask #7 (see Figure 46) is a lightfield mask and noticeable different from the previous masks, but the processing uses the same parameters.

Begin by spinning SHIPLEY 1813 photoresist onto the topside of the wafer and performing a soft-bake.

1. Photolithography with Mask #6

(Aluminum Contacts):

Exposure & Development

(Check Parameters section for details)

REPEAT: Load Mask #7 onto the ABM contact-aligner mask stage and align the mask to the wafer (see Alignment System section). Transfer the wafer to a dish of MF319 and develop the exposed resist for 30-60 seconds. When finished, pour the used MF319 into the MF319 waste container located under the solvent bench next to the photoresist.

2. Hard-baking:

(Check Parameters section for details)

Remove any remaining solvents and/or water from the resist by loading a wafer onto a *hotplate* for the desired temperature and time.

3. Etching Aluminum:

(Check Parameters section for details)

Pour a small amount of *PAE etchant*, enough to cover a wafer, into a pyrex or Teflon evaporating dish. Submerge the wafer and gently swirl until all the exposed aluminum has been etched. A visible etch front will move across the wafer as the aluminum is removed. The etch will take between 10-15 minutes to complete.

Figure 45 A student using the ABM mask aligner to align Mask #7.



Figure 46 One of the features generated by mask #7. The squares represent the aluminum pads and will be used for testing the devices. The writing is an identifier for individual devices, it reads "A1R6" meaning "Accelerometer #1, Resistor Type-6"

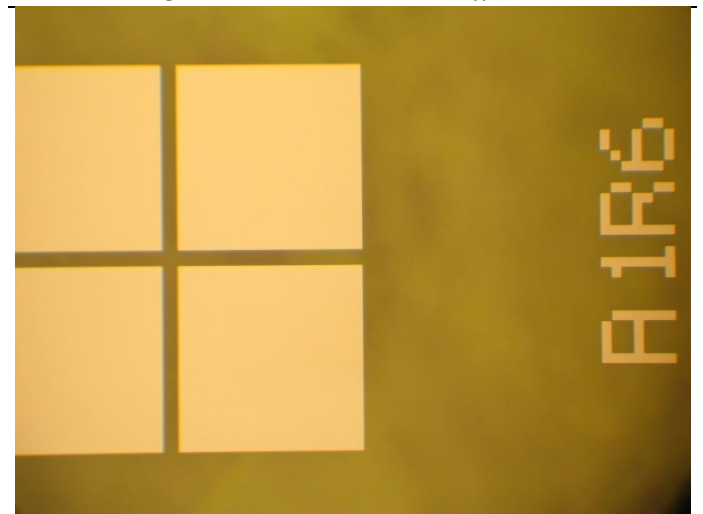
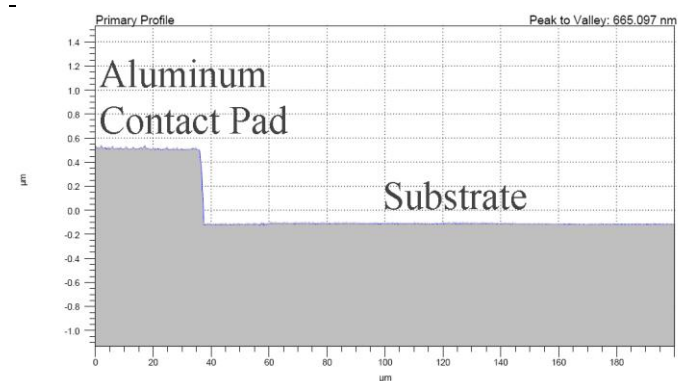


Figure 47 Profilometer data of an aluminum pad. The data reveals the thickness of the aluminum film.



Methods:

4. Solvent Clean:

REPEAT: Place an evaporating dish on the solvent bench to catch solvent waste. Rinse the wafer with acetone using the squirt bottle and follow with methanol and isopropyl. Rinse the wafers in DI water and dry with a nitrogen gun. When finished pour the solvent waste into the *Solvent Waste Container*.

5. Documenting & Taking Pictures:

Use the microscope and digital camera to document the wafer after etching the aluminum. Take pictures of the fully formed piezoresistors (see **Figure 48**).

6. Removing the Handle wafer:

The WAFERGRIP adhesive needs to be de-bonded before annealing to avoid melting in the furnace. The WAFERGRIP bond can be removed with a special stripper or a heated bath of *SVC-175* (positive resist stripper).

Pour a small amount *SVC-175*, enough to cover a single bonded wafer, into a *Pyrex evaporating dish*. Place the dish onto a *hotplate* set to 100°C, to heat the solution to 90°C. When the solution has reached 90°C, submerge a wafer in the *SVC-175* and place a watch glass over the dish. Keep the wafer in the solution for several hours (overnight if possible) until the WAFERGRIP is dissolved. When the bond is removed, rinse and dry the etched wafer, and remove any WAFERGRIP adhesive still attached to the backside with a pair of tweezers. Note, the solution will also become saturated after several wafers and may need replacing.

Week 10

Figure 48 A completed piezoresistor with patterned aluminum pads.

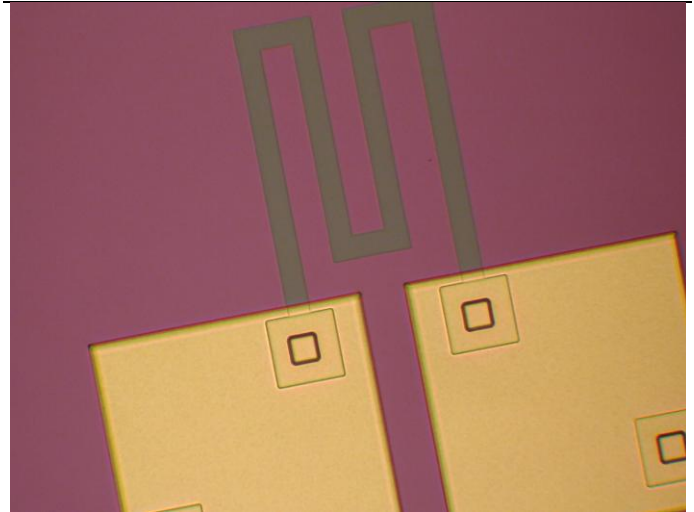


Figure 49 The lab TA helping setup the *SVC-175* to detach to bonded wafer.



7. Annealing:

The goal of the anneal is to improve the junction between the silicon and aluminum. Before the anneal, the junction is highly resistive and inhibits the effectiveness of the piezoresistors. Afterward, the junction is more conductive and creates a more stable sensor.

To anneal, place wafers into the quartz boat (away from the diffusion sources) and insert into the heated furnace. Leave for the desired time, then remove and allow wafers to cool

GOALS:

1. Wafer Cleaving (optional)
2. Plasma Release etch
3. Start Testing and Characterization

EQUIPMENT:

- Wafer Scribe
- MARCH plasma etcher
- AMBIOS Profilometer
- Optical microscope
- CASCADE probe station
- DMM
- Oscilloscope

PARAMETERS:

Plasma Release Etch Parameters

Power (W)	Gas mixture	Pressure (mTorr)	Time (90 sec increments)
175	85 SF ₆ : 10 O ₂	375	Approx. 4x (4.5mins)

Methods:

1. Cleaving (Optional):

The wafer can be cleaved in sections to help with loading effects during the plasma release etch, however it is not necessary and in most cases not be done. The wafer is very fragile from the bulk silicon etch so great care must be used if cleaving. This step should only be performed by experienced handlers.

To cleave, use the diamond or steel-tipped scribed and make a notch on the edge of the backside of the wafer, between etched features. On both sides of the notch, hold the wafer firmly and bend. The wafer should break apart along the crystal plane (and hopefully not shatter into a thousand pieces)

2. Plasma Release Etch:

(Check *Parameters* section for details)

The final step is the plasma release-etch. The goal is to release the cantilever accelerometers by removing the exposed silicon from the topside. The etch is performed at the *MARCH plasma etcher* and will take roughly 5-10 minutes to complete. The exposed silicon is removed in a mixture of SF_6 and O_2 . Note, the SiO_2 is used to mask the etch but will be etched considerably during the process. Measure the thickness of the SiO_2 prior to etching and monitor its etch rate as the devices are released. Do not continue etching if the SiO_2 is completely removed, as this could damage the diffused piezoresistors.

Begin by consulting the *MARCH plasma etcher* operations manual for details on setting up the equipment and check the *Parameter* section for details on the etching recipe. Load the wafer into the center of the etching chamber, topside facing upward. Follow the operations manual to ignite the plasma and begin the etch. Etch the wafer in 90 second increments, observing the wafer under the microscope, profilometer and Nanospec after each increment. About 50% of the devices should be released after 1-2 etching attempts and all should be released after 4-5 attempts.

Figure 50 A close-up of the wafer surface after the release etch. Note the released sensor to the right.

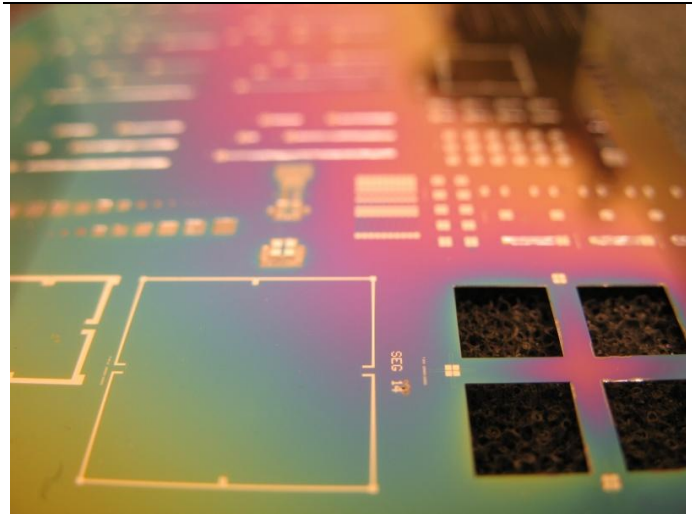
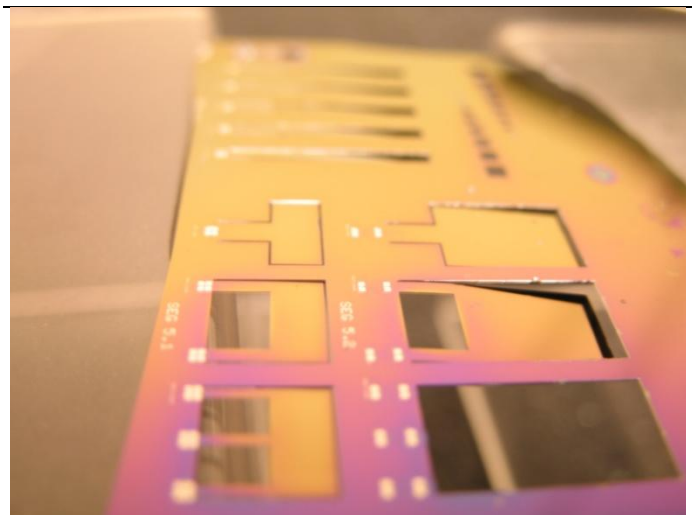


Figure 51 Two students operating the MARCH plasma etcher.



Figure 52 A close-up of a wafer segment with released accelerometers.



Methods:

3. Start Testing & Characterizing:

Device testing is performed at the *CASCADE probe station* (see **Figure 55**). Perform qualitative and quantitative tests on the piezoresistors, Wheatstone bridges, cantilevers, membranes, and resistors. Testing methods will vary but measurable values can be obtained for changes in resistance, gauge factors, resonant frequencies, Young’s modulus, and more.

Measuring ΔR vs Deflection:

To measure the change in resistance as a function of deflection for a cantilever accelerometer, a simple test is performed with three probes and a *DMM* (see **Figure 51**). Begin by placing the wafer on the *CASCADE* stage. Attach two of the probes to the *AGILENT device analyzer* or *DMM*. Adjust the two probes using the *XYZ micropositioners*, and place them on the aluminum pads of the piezoresistor closest to the cantilever beam (see **Figure 53**). Center a third probe directly above the center of the cantilever. Adjust the *Z* position of the third probe and record the resistance measured by the other two probes. Continue deflecting the beam to obtain a plot of Resistance vs Deflection (see **Figure 56**). Note, a full revolution of the *Z* adjustment knob deflects the probe tip approximately $250\mu\text{m}$.

Figure 55 A view of a wafer being probed and tested at the *CASCADE* probe station.

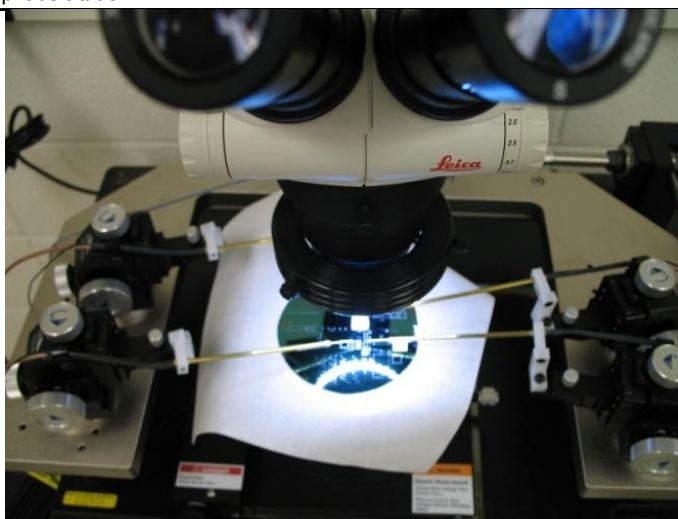


Figure 53 An accelerometer under the *CASCADE* probe station. The beam is being deflected by one probe while two others measure the change in resistance of the piezoresistors.

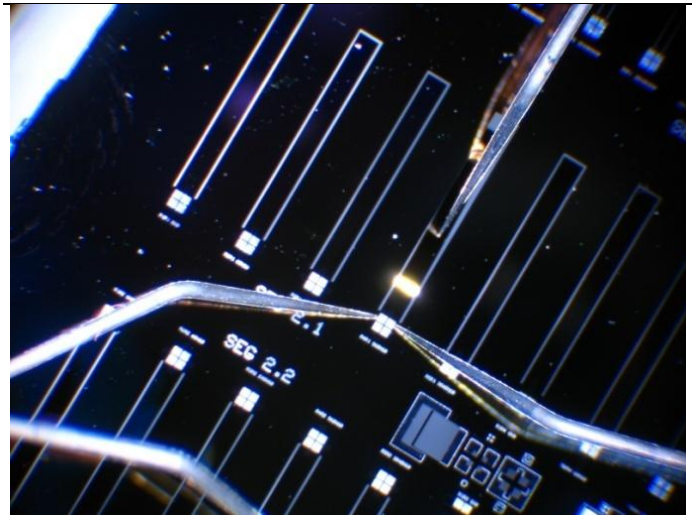


Figure 54 A small accelerometer being probed and characterized.

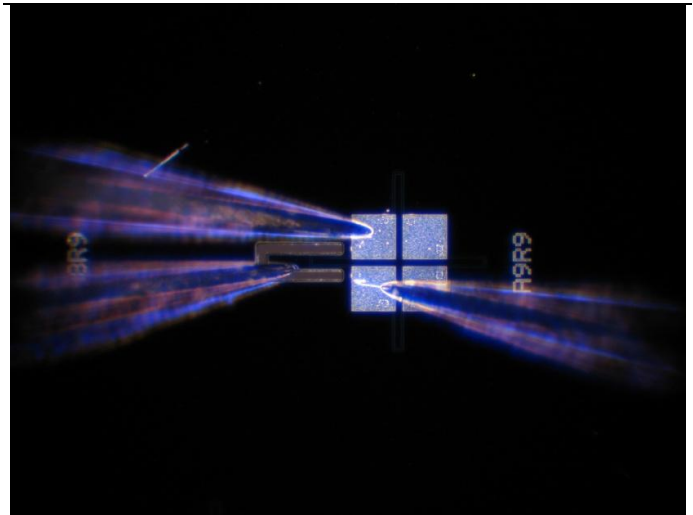
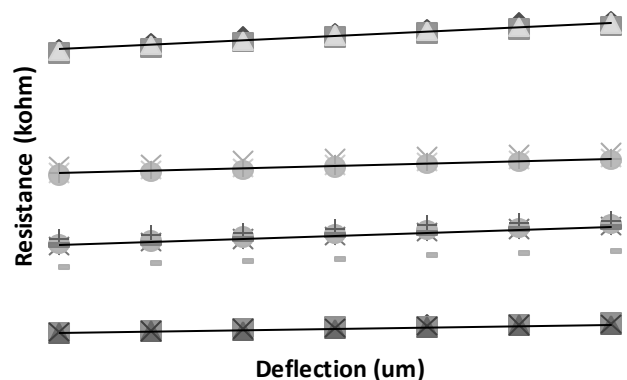


Figure 56 A plot of the change in resistance as a function of deflection, for several cantilever accelerometers. The maximum deflection was $1500\mu\text{m}$. Resistance values change between $100\text{--}500\Omega$, given different cantilevers geometries and piezoresistor types.

Resistance vs Deflection



GOALS:

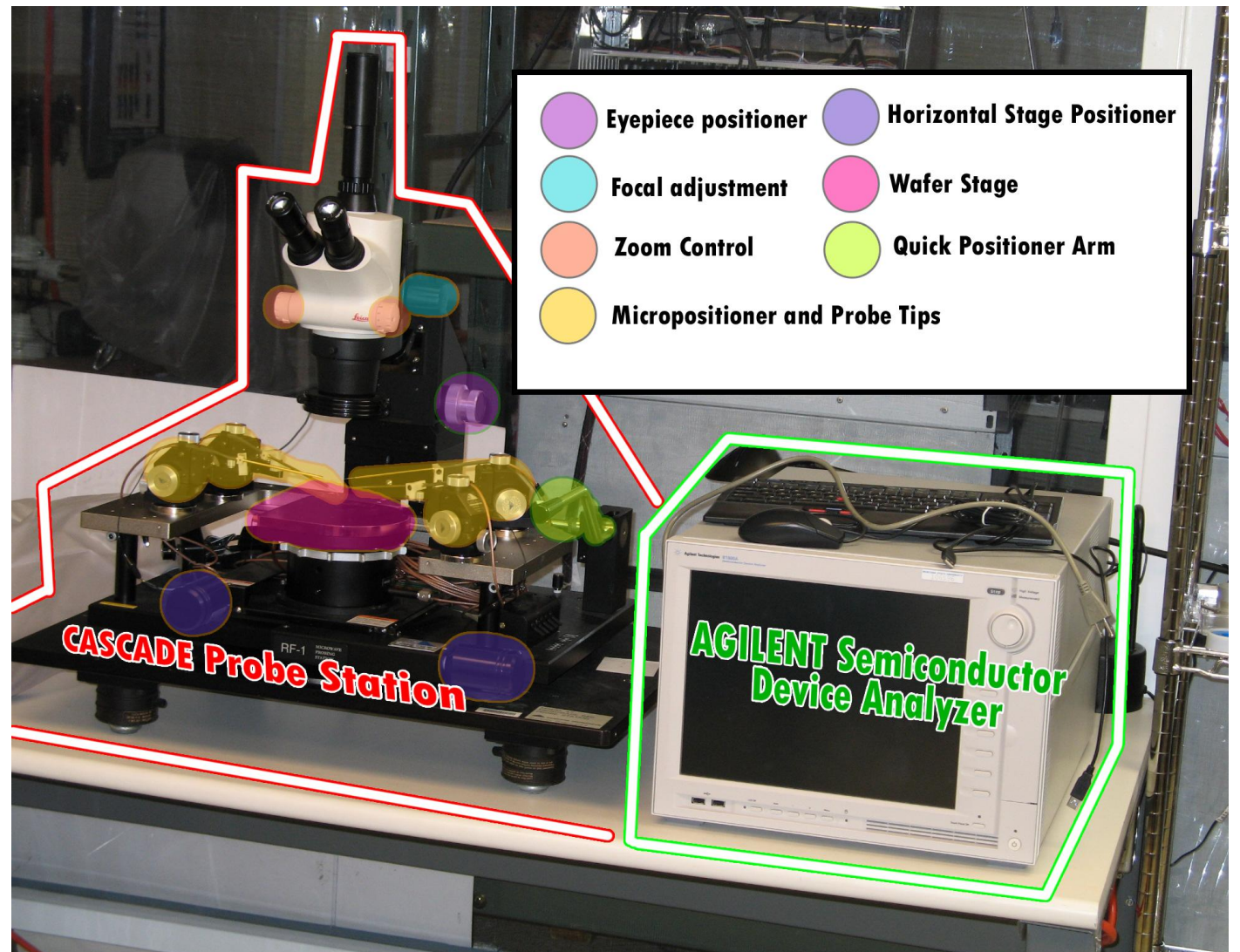
1. Characterize and test as many devices as possible

EQUIPMENT:

- Wafer Scribe
- MARCH plasma etcher
- AMBIOS PROFILOMETER
- Optical microscope
- CASCADE probe station
- DMM
- Oscilloscope
- Additional microprobe and XYZ micropositioner
- Power Supply

PARAMETERS:

Figure 57 Overview of the probe station.



Methods:

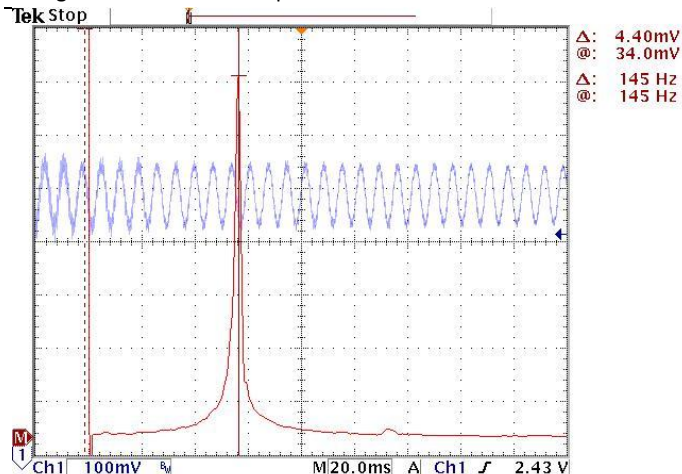
1. Continue Testing:

Continue testing devices and obtaining qualitative and quantitative results.

Measuring Resonant Frequency:

To measure the resonant frequency of a cantilever accelerometer, an advanced test setup is necessary. Begin by obtaining an additional microprobe and XYZ micropositioner. Set up the extra probe so that is parallel with the wafer. Use one of the CASCADE probes to press down on a cantilever and slide the extra probe between the cantilever and the bottom of the wafer as shown in **Figure 58**. Position the four CASCADE probes on the four aluminum pads of a cantilever sensor. Connect the probes to the oscilloscope and DC power supply as shown in **Figure 58**. Be sure to connect the power supply ground to the oscilloscope ground. To measure the oscillations a trigger will need to be set on the oscilloscope to capture the oscillations when the extra probe is released. Before measuring, be sure to adjust the vertical and horizontal scales to the appropriate levels. When all the probes are in place and the oscilloscope is adjusted to the correct settings, pull the probe from the cantilever. The oscilloscope should capture the resulting oscillations as shown in **Figure 59 and 60**. It may take several attempts to get the appropriate settings on the oscilloscope. With the resulting waveform, use the FFT function of the oscilloscope to acquire the resonant frequency.

Figure 60 An accelerometer under the CASCADE probe station. The beam is being deflected by one probe will two others measure the change in resistance of the piezoresistors.



Week 12,13,14

Figure 58 An accelerometer under the CASCADE probe station. The beam is being deflected by one probe will two others measure the change in resistance of the piezoresistors.

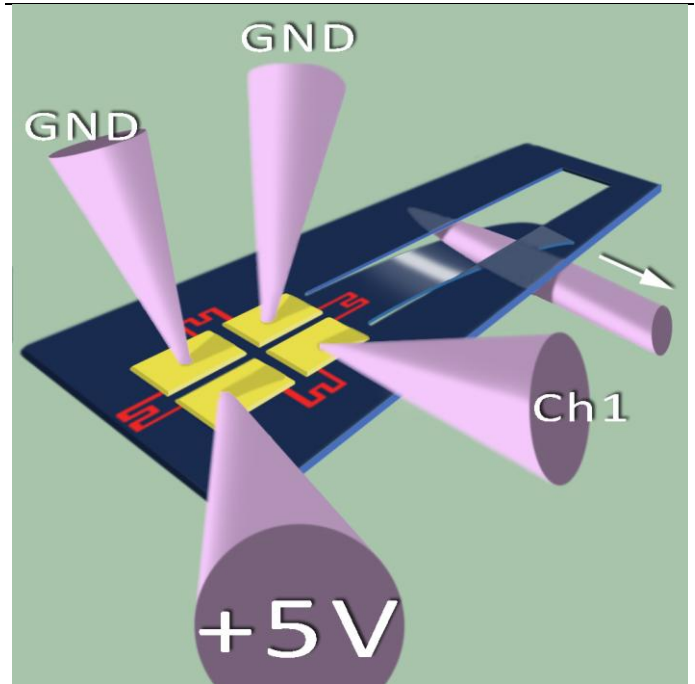
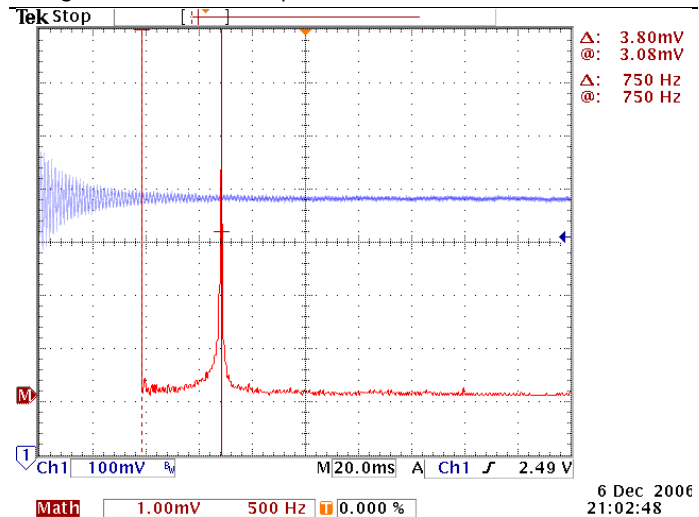


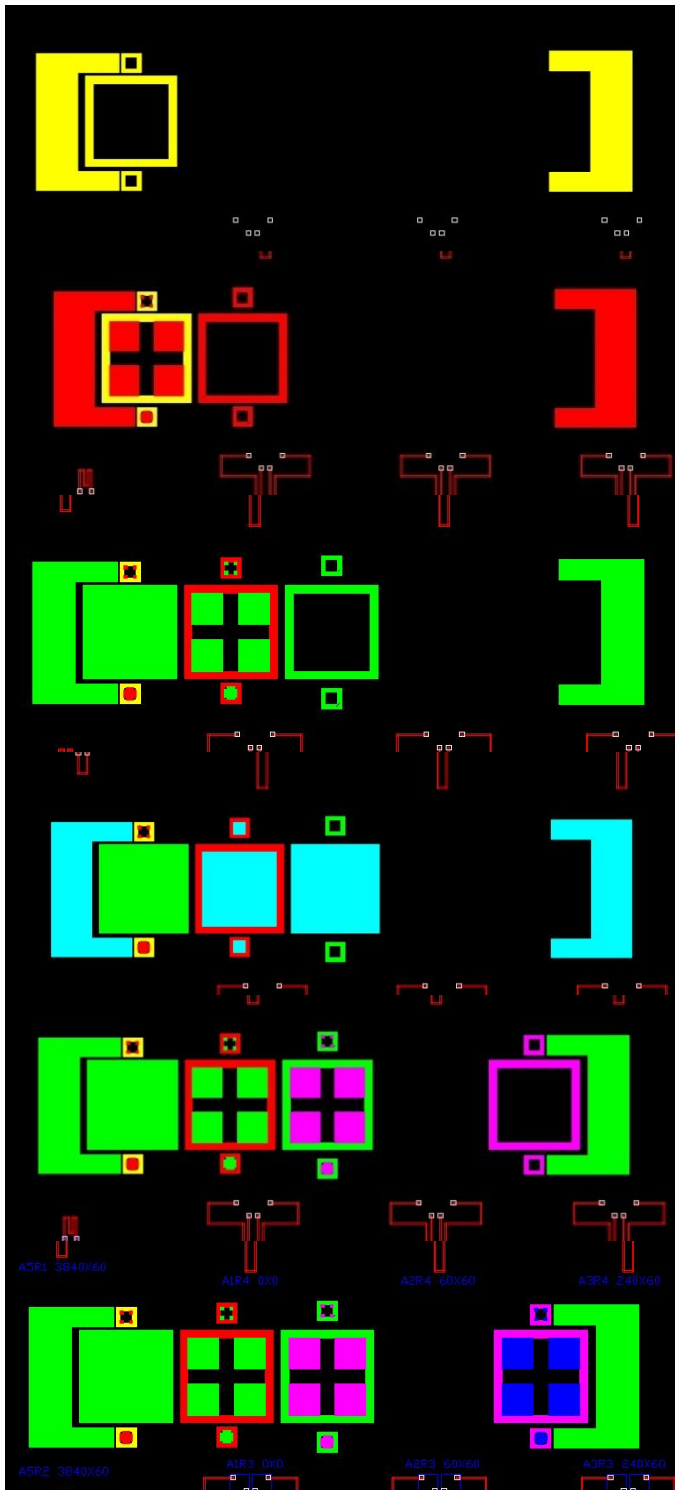
Figure 59 An accelerometer under the CASCADE probe station. The beam is being deflected by one probe will two others measure the change in resistance of the piezoresistors.



Alignment System

The alignment system has yet to be optimized. The first three masks are straightforward in the alignment marks. The fourth mask is the backside alignment mask and requires IR light sources to get the marks to line up. The next alignment would normally be the Top etch & Vias mask (Mask 6), however the marks from Mask 3/5 were removed in a previous process step. Therefore, Mask 3/5 must be aligned again. Once it's realigned, then Mask 6 and Mask 7 can be easily aligned. The repeat could be removed if Mask 6 was aligned to Mask 1 or Mask 2.

Layout:



Description:

Mask 1: Resistor Contacts: Dark Field

Mask 2: Resistor: Dark Field

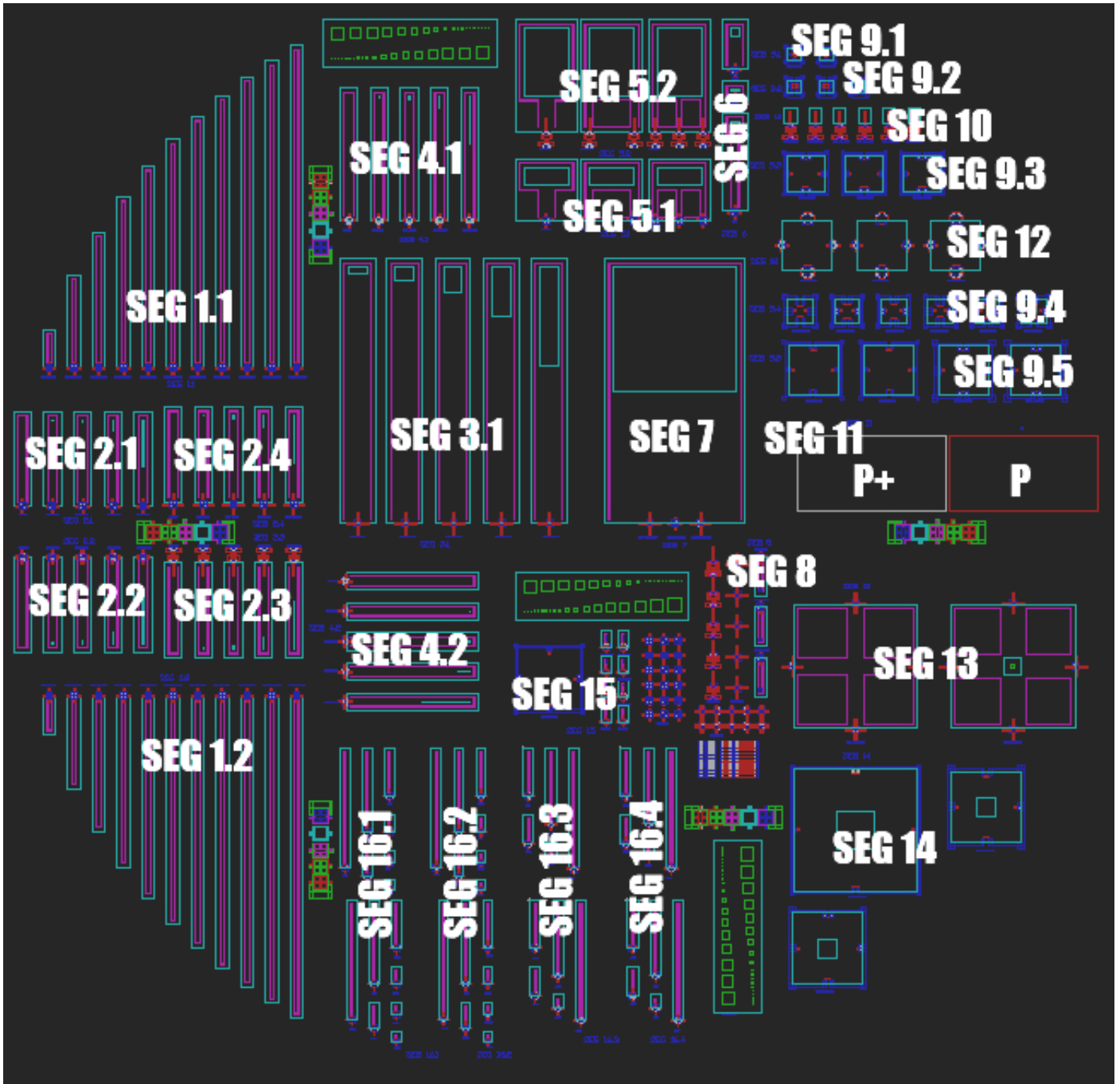
Mask 3/5: Align Marker: Dark Field

Mask 4: Fixed Back Etch: Dark Field

Mask 6: Top Etch & Vias: Dark Field

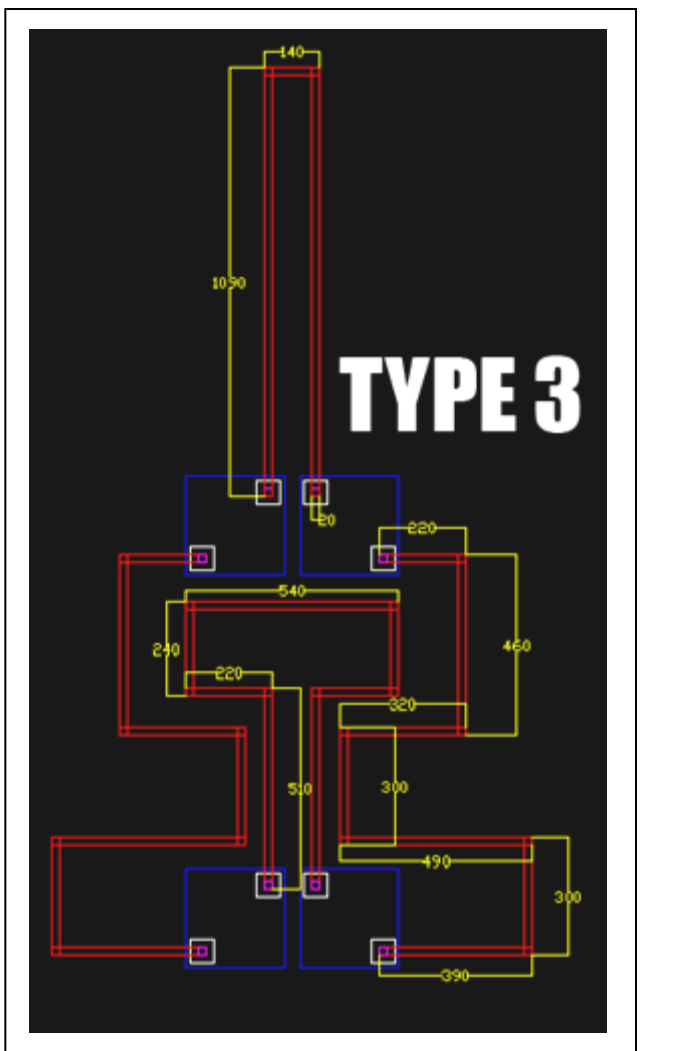
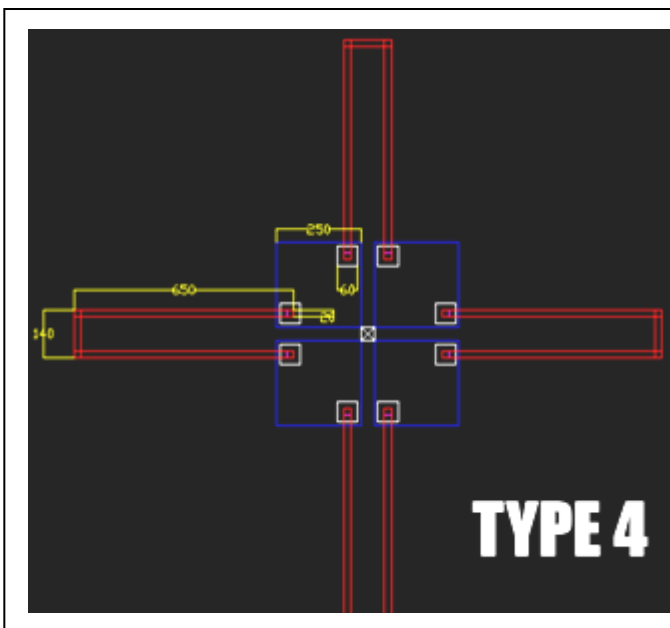
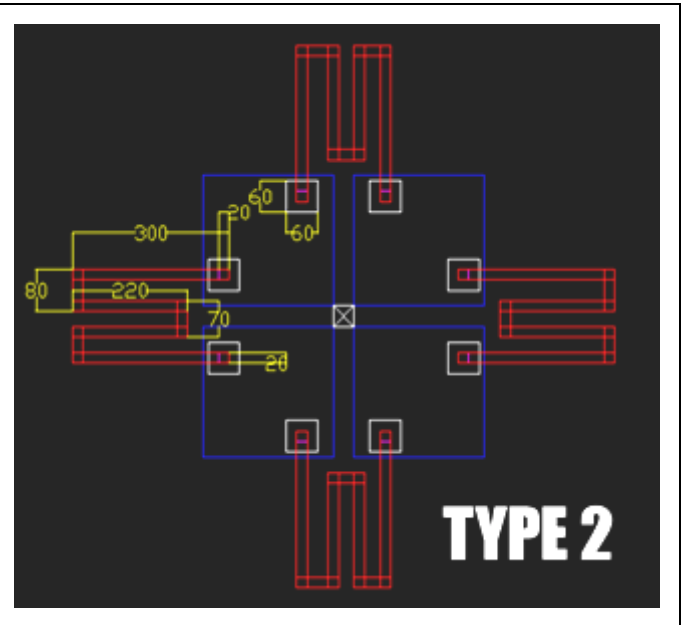
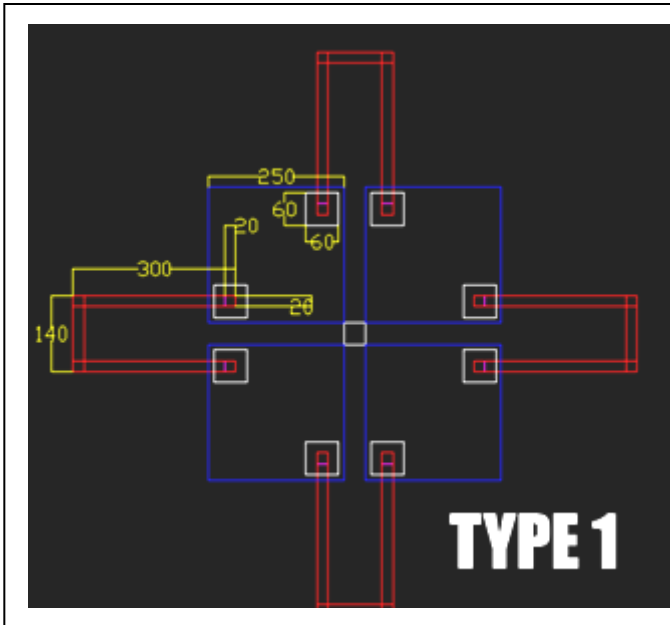
Mask 7: Metal Pads: Light Field

Wafer Layout



Refer to the following *Device Listing* Section for more details on the devices in each numbered segment.

Common Piezoresistor Types



SUMMARY OF DEVICES			Thickness: 20-45um, Youngs Modulus: 160GPa				
IN MICRONS			Overall Device		Ideal Proof mass		Multi Cantilever/Flexure
SEGMENT	DEVICE:RESISTOR No.	Length	Width	Length	Width	Length	Width
1.1	A1R1	2440	280	0	0		
	A2R1	6860	280	0	0		
	A3R1	10290	280	0	0		
	A4R1	13140	280	0	0		
	A5R1	15630	280	0	0		
	A6R1	17780	280	0	0		
	A7R1	19630	280	0	0		
	A8R1	21330	280	0	0		
	A9R1	22840	280	0	0		
	A10R1	24150	280	0	0		
	A11R1	25360	280	0	0		
1.2	A1R1	2440	280	0	0		
	A2R1	6860	280	0	0		
	A3R1	10290	280	0	0		
	A4R1	13140	280	0	0		
	A5R1	15630	280	0	0		
	A6R1	17780	280	0	0		
	A7R1	19630	280	0	0		
	A8R1	21330	280	0	0		
	A9R1	22840	280	0	0		
	A10R1	24150	280	0	0		
	A11R1	25360	280	0	0		
2.1	A1R1	7000	720	0	0		
	A2R1	7000	720	60	60		
	A3R1	7000	720	240	60		
	A4R1	7000	720	960	60		
	A5R1	7000	720	3840	60		
2.2	A1R2	7000	720	0	0		
	A2R2	7000	720	60	60		
	A3R2	7000	720	240	60		
	A4R2	7000	720	960	60		
	A5R2	7000	720	3840	60		
2.3	A1R3	7000	720	0	0		
	A2R3	7000	720	60	60		
	A3R3	7000	720	240	60		
	A4R3	7000	720	960	60		
	A5R3	7000	720	3840	60		
2.4	A1R4	7000	720	0	0		
	A2R4	7000	720	60	60		
	A3R4	7000	720	240	60		
	A4R4	7000	720	960	60		
	A5R4	7000	720	3840	60		
3.1	A1R4	20690	2160	1500	500		
	A2R4	20690	2160	1500	1000		
	A3R4	20690	2160	1500	2000		
	A4R4	20690	2160	1500	4000		
	A5R4	20690	2160	1500	8000		
4.1	A1R1	10000	720	0	0		
	A2R1	10000	720	60	60		
	A3R1	10000	720	240	60		
	A4R1	10000	720	960	60		
	A5R1	10000	720	3840	60		

SEGMENT	DEVICE:RESISTOR No.	Length	Width	Length	Width	Length	Width
4.2	A1R1	720	10000	0	0		
	A2R1	720	10000	60	60		
	A3R1	720	10000	60	240		
	A4R1	720	10000	60	960		
	A5R1	720	10000	60	3840		
5.1	A1R1	4310	4280	1480	3620	2140	1320
	A2R1	4310	4280	1480	3620	2140	660X2
	A3R1	4310	4280	1480	3620	2140	440X3
5.2	A1R1	8340	4280	5510	3620	2140	1320
	A2R1	8340	4280	5510	3620	2140	660X2
	A3R1	8340	4280	5510	3620	2140	440X3
6	A1R1	7310	1280	620	620	6000	560
	A1R2	810	1280	60	620		
	A1R3	3310	1280	620	620		
7	A1R4	20690	10660	10000	10000		
	A1R1						
	A1R4						
8	A1R1	2430	280	Insignificant Alum			
	A1R2	2430	280	Insignificant Alum			
	A1R3	2430	280	Insignificant Alum			
9.1	P1R11	340	340	0	0		
	P2R11	340	340	0	0		
9.2	P1R12	340	340	0	0		
	P2R12	340	340	0	0		
	P3R12	340	340	0	0		
9.3	P1R02	2340	2340	0	0		
	P2R02	2340	2340	0	0		
	P3R02	2340	2340	0	0		
9.4	P1R02	1340	1340	0	0		
	P2R02	1340	1340	0	0		
	P3R02	1340	1340	0	0		
	P4R02	1340	1340	0	0		
	P5R02	1340	1340	0	0		
	P6R02	1340	1340	0	0		
9.5	P1R12	3340	3340	0	0		
	P2R12	3340	3340	0	0		
	P3R12	3340	3340	0	0		
	P4R12	3340	3340	0	0		
10	P1R3	610	340	0	0		
	P2R3	610	340	0	0		
	P3R3	610	340	0	0		
	P4R3	610	340	0	0		
	P5R3	610	340	0	0		
	P6R3	610	340	0	0		
11	Diffusion incorrectly labeled P+(LEFT) P(RIGHT)						
	Contacts RESISTORS						
12	P1R03	3340	3340	0	0		
	P2R03	3340	3340	0	0		
	P3R03	3340	3340	0	0		
13	T1R4	9340	9340	0	0	4000	1340
	T2R4	9340	9340	1340	1340	3670	2000
14	P1R12	9340	9340	3000	3000		
	P2R02	5030	5030	1500	1500		
	P3R02	5030	5030	1500	1500		

SEGMENT	DEVICE:RESISTOR No.	Length	Width	Length	Width	Length	Width
15	P1R01	4340	4340	0	0		
	A1R5	690	80	Insignicant Alum			
	A2R5	690	80	Insignicant Alum			
	A3R5	690	80	Insignicant Alum			
	A4R5	690	80	Insignicant Alum			
	A5R5	690	80	Insignicant Alum			
	A6R5	690	80	Insignicant Alum			
	A7R5	690	80	Insignicant Alum			
	A8R5	690	80	Insignicant Alum			
16.1	A1R6	8990	80	0	0		
	A2R6	6110	80	0	0		
	A3R6	3210	80	0	0		
	A4R6	690	80	0	0		
	A5R6	1410	80	0	0		
	A6R7	360	80	0	0		
	A7R8	120	80	0	0		
	A8R6	8990	80	0	0		
	A9R6	6110	80	0	0		
	A10R6	3210	80	0	0		
	A11R6	690	80	0	0		
	A12R6	1410	80	0	0		
	A13R7	360	80	0	0		
	A14R8	120	80	0	0		
16.2	A1R9	8990	80	0	0		
	A2R9	6110	80	0	0		
	A3R9	3210	80	0	0		
	A4R9	690	80	0	0		
	A5R9	1410	80	0	0		
	A6R10	360	80	0	0		
	A7R11	120	80	0	0		
	A8R9	8990	80	0	0		
	A9R9	6110	80	0	0		
	A10R9	3210	80	0	0		
	A11R9	690	80	0	0		
	A12R9	1410	80	0	0		
	A13R10	360	80	0	0		
	A14R11	120	80	0	0		
16.3	A1R6	3150	120	0	0		
	A2R6	1700	120	0	0		
	A3R6	5450	120	0	0		
	A4R6	430	120	0	0		
	A5R6	9060	120	0	0		
	A6R6	3150	120	0	0		
	A7R6	1700	120	0	0		
	A8R6	5450	120	0	0		
	A9R6	430	120	0	0		
	A10R6	9060	120	0	0		

Device Listing

SEGMENT	DEVICE:RESISTOR No.	Length	Width	Length	Width	Length	Width
16.4	A1R9	3150	120	0	0		
	A2R9	1700	120	0	0		
	A3R9	5450	120	0	0		
	A4R9	430	120	0	0		
	A5R9	9060	120	0	0		
	A6R9	3150	120	0	0		
	A7R9	1700	120	0	0		
	A8R9	5450	120	0	0		
	A9R9	430	120	0	0		
	A10R9	9060	120	0	0		
Whtstone Bridges	18 Type R1						
	10 Type R2						
	5 Type R3						
	5 Type R4						
Test Resis	20 P+ Diffusion Resistors of varying lengths and widths						
	20 P Diffusion Resistors of varying lengths and widths						