Design of a Radiation Tolerant Computing System Based on a Many-Core Architecture

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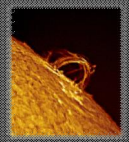
Summary

In this project, we designed a redundant processor computing system on reprogrammable hardware for use in aerospace systems. The system is designed with 64 redundant PicoBlaze soft processors in order to detect and recover from faults that may occur due to radiation strikes. Three processors at a time run in Triple Modular Redundancy (TMR) with voting to check whether a fault has occurred in one of the processors. A software interface was designed to allow a user to disable one of the active processors to simulate a processor failing due to a hard fault. The system should continue to run while seamlessly disabling the faulted processor and bringing a new processor online to take its place.

Background



When high-energy cosmic particles strike integrated circuits, a variety of fault conditions occur. Such fault conditions are called Single Event Effects. Single Event Upsets (SEU), or soft faults, occur when the particles create soft errors such as bit flips. Soft faults can be remedied with a software reset. Single Event Damage, or a hard fault, causes physical damage to the circuit and cannot be remedied by a reset. Instead, other mitigation techniques, such as swapping in spare circuitry, must be investigated. Both of these failure conditions are of great concern to NASA as they develop the technology for interplanetary missions in the coming decades.

Design Objectives

The advising entity for this design project was the NASA *Radiation Hardened Electronics for Space Exploration (RHESE)* program. This group specified the following design objectives:

Task #1: Design a graphical user interface (GUI) that shows an 8x8 array of processors. A user will be able to disable one of the processors using the GUI. This application mimics a processor being physically damaged by a radiation strike.

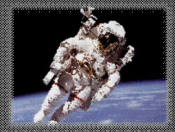
Task #2: Design digital hardware to communicate with a PC in order to receive the information from the application described in task 1.

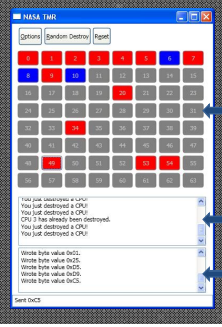
Task #3: Design a computer system containing 64 redundant microprocessors to control a basic set of peripherals. The system will disable damaged processors and enable inactive processors, depending on the information received from the GUI.

System Operation

User Interface:

- Shows the status of each of the 64 processors.
- Blue - Active
- Gray - Inactive
- Red - Damaged





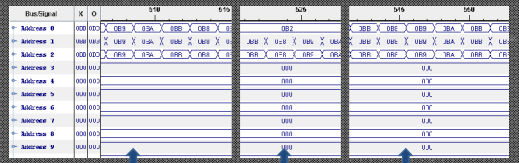
Processor status window. Clicking on a processor damages it.

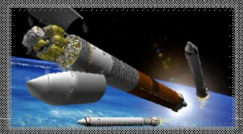
CPU Destruction Log

System Communications Log

Verifying Soft Fault Functionality:

- During a soft fault, the corrupted processor is not disabled. Instead, it is reset and re-synchronized with the two working processors.





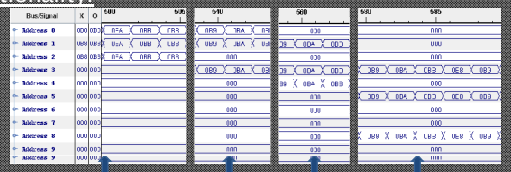
System initialized and running normally in TMR mode.

Processor 0 has been corrupted by an SEU. The TMR detects the failure.

Processor 0 brought back into synch with other two processors.

Verifying Hard Fault Functionality:

- When a hard fault occurs, a simple reset will not suffice. The system therefore has 61 back-up processors that can be brought online, initialized, and synchronized with the two working processors should one processor fail.



System initialized and running normally.

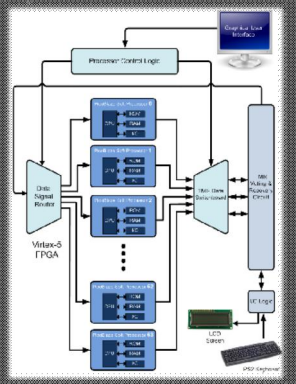
Processor 2 faults; processor 3 initialized and synchronized.

Processor 0 faults; replaced by processor 4.

System after several additional hard faults.

System Overview

- 64 redundant soft processors are implemented on a Xilinx Virtex-5 FPGA. Three processors are active at any given time.
- The TMR Data Switchboard sends outputs from the three active processors to the TMR circuit.
- The TMR circuit checks for soft faults and resets faulted processors.
- The Data Signal Router intercepts signals sent back from the TMR circuit and routes them to the three active processors.
- Processor Control Logic block takes in commands from the Graphical User Interface and tells the Router and Switchboard which processors have been damaged.



Results

- The computer system is able to control 64 processors and seamlessly switch between them when a hard fault occurs.
- There is negligible performance degradation when recovering from a fault or when switching between processors for this application.

Acknowledgements

We would like to thank the Montana Space Grant Consortium and the NASA *Exploration Systems Mission Directorate* (ESMD) Higher Education Program for sponsoring this project. We would like to especially thank NASA RHESE engineers Andrew Keys and Bob Ray, last semester's team of Anthony Thomason and Colin Tilleman, and Clint Gauer for their help and support.

Design of a Radiation Sensor for a Tolerant Computing System

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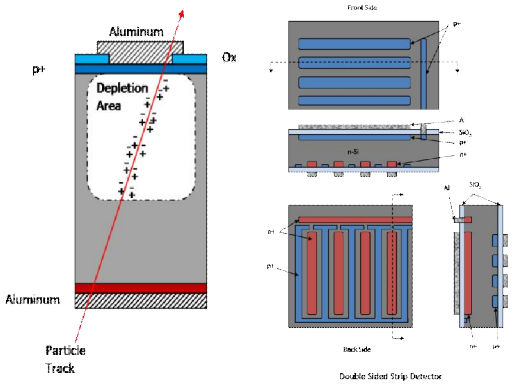
Summary

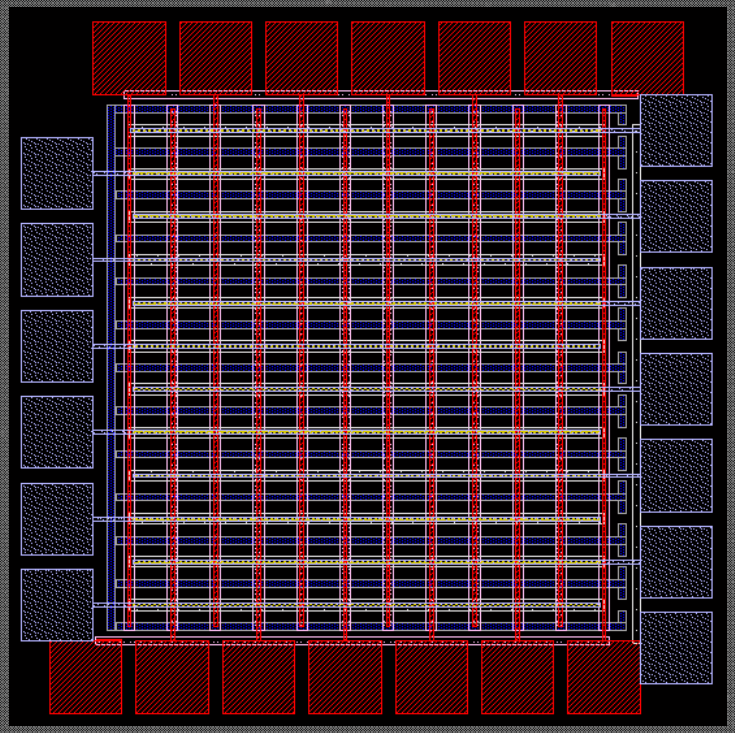
Ionization radiation passing through the sensor creates electron hole pairs on an average energy rate of 3.6 eV per electron-hole pair. In silicon, 1 MeV of energy corresponds to 44.4 fC of charge, which is more than enough to flip the state of a logic circuit fabricated in a modern process. The integrated radiation sensor gives spatial location of radiation strikes for dynamic reconfiguration of the FPGA
The energy of the radiation and the size of the depletion volume determine the amount of charge ultimately collected which is a function of the sensor design, materials, and bias voltage.

Double Sided Strip Detectors



This sensor is a double sided strip detector (DSSD) based on a large area p-n junction. The electrodes in the radiation sensor are broken up into narrow electrically isolated strips running orthogonal to each other on opposite sides of the silicon substrate. Each strip will be monitored by a separate electronic channel. The location of the ionization particle is given by the position of the intersection of the strips receiving the signals from the front and back side electronics.

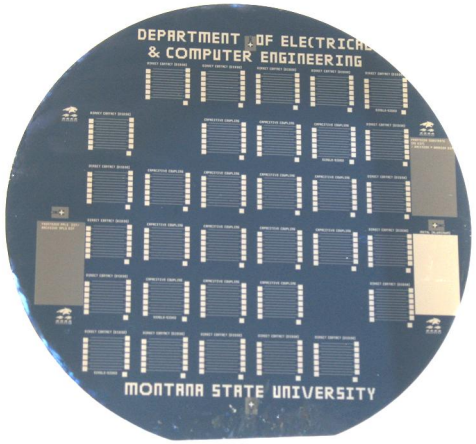
Mask Layers



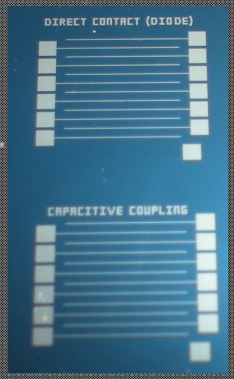
Mask Set

The mask set was reduced to four individual masks by designing the mask set symmetrically such that they could be used for both surfaces of the wafer. The back side surface is rotated 90 degrees relative to front side pattern. Two different sensor designs are fabricated simultaneously with the mask set. One is a directly coupled p-n junction and the other uses capacitive coupling by creating a Metal-Oxide- Semiconductor junction.

Fabricated Wafer



Die



Thirty-six 1cm^{2}individual die are created on each wafer: 16 direct contact double sided devices, 4 direct contact single sided devices, 12 capacitive coupled double sided devices, & 4 capacitive single sided devices.

There are also 3 test areas for measuring the sheet resistivity of the diffusion and metal layers on both sides of the wafer used to characterize the fabrication process.