

# Controlled Impedance Chip-to-Chip Interconnect Using Coplanar Wire Bond Structures

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**Abstract: This paper presents the design and Finite Element Analysis (FEA) of a controlled impedance chip-to-chip interconnect system using coplanar wire bonds. Our proposed system uses on-chip coplanar transmission lines which interface to 3 adjacent wire bonds configured to yield a fully impedance matched system.**

## I. INTRODUCTION

3-Dimensional (3D) packaging has emerged in the past decade as a way to cost-effectively achieve functionally diverse systems with very high chip/package ratios [1,2]. The ability to segment a design into multiple die within the same package provides a method to: (1) optimize substrate materials for a given application; (2) mitigate power density issues associated with high transistor counts on a single-die, and (3) use the most economical design partitioning of the various components in the system. System-in-Package (SiP) has been adopted in portable computing applications which require very efficient package footprints. The most widely used combination of technology in SiP is the integration of CMOS processors and memory [3]. The most common technique to interconnect multiple die within a single package is with a wire bond. A wire bond provides a flexible and robust connection between arbitrary-placed pads across multiple die and has been established as the most commonly used package interconnect over the past decade [4].

Historically, the wire bond has not had a significant impact on the off-chip signal path performance due to its electrical response being relatively small compared to the transistor gate and on-chip interconnect delay. However, with the recent advances in CMOS fabrication technology, the wire bond in the signal path is becoming an increasing problem [6]. As transistor features shrink, faster edge rates are possible. These increased edge rates are exposing the distributed nature of the interconnect structures used to carry the signals. In the mid 1990's, CMOS edge rates became fast enough ( $<1\text{ns}$ ) such that the printed circuit board (PCB) traces used to connect multiple packaged parts had to be treated as distributed transmission lines. This required the use of controlled impedance and terminations in order for the systems to operate at higher data rates. While this approach has worked quite well over the past decade, we are now seeing a new class of edge rates ( $<100\text{ps}$ ) that are causing secondary interconnect structures such as on-chip traces and package interconnect to behave as distributed elements. Since these secondary interconnect structures are not designed to have controlled impedance, they cause reflections due to the impedance mismatches they introduce to the system.

SiP has improved electrical performance by completely eliminating the PCB transmission lines in a typical system and instead has created an architecture in which dies are connected directly together using wire bonds. This approach reduces the electrical length of the chip-to-chip interconnect, thus avoiding the distributed behavior and the need for controlled impedance and terminations to accommodate the long PCB traces. However, the forthcoming edge rates of CMOS transistors are predicated to be fast enough ( $<10\text{ps}$ ) to cause even a direct wire bond connection between dies to behave as a distributed element. As a result, packaging engineering must begin developing novel interconnect schemes in order to overcome the next electrical performance barrier. In this work, we propose using coplanar transmission lines to achieve controlled impedance on the die itself. A G-S-G configuration of wire bonds is then used to connect the coplanar transmission lines on multiple dies. The wire diameter ( $D_{wb}$ ), wire pitch ( $P_{wb}$ ), and encapsulate permittivity ( $\epsilon_{r-pkg}$ ) dictates the characteristic impedance of the G-S-G wire bond configuration. This paper presents the design of a chip-to-chip interconnect system consisting of two on-chip coplanar transmission lines connected with a coplanar wire bond configuration that is designed to achieve a fully impedance matched system. This type of system can be used in both adjacently-placed and stacked-die configurations as shown in figure 1(a) and 1(b).

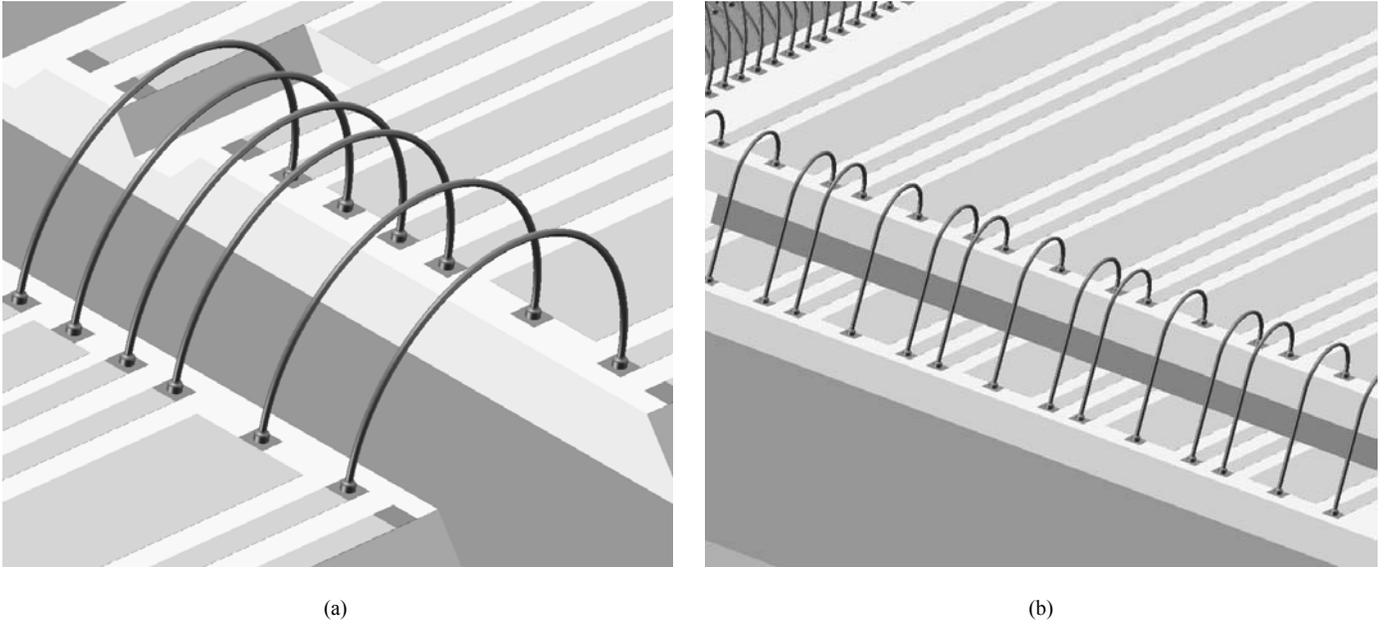


Fig. 1. 3-D Rendering of our interconnect approach used in an SiP application with adjacently-placed dies (a) and stacked-dies (b). Coplanar transmission lines on the two dies are connected using a G-S-G wire bond configuration.

## II. SYSTEM DESIGN

Our proposed interconnect system is constructed using two controlled impedance structures. The first is an on-chip coplanar transmission line on-chip. It is assumed that this type of on-chip structure is used between the diffusion regions of an integrated circuit (IC) and the wire bond pads along the perimeter of the substrate. The transmitter (Tx) and receiver (Rx) are also assumed to contain terminations with an impedance equal to that of the interconnect structure. The second controlled impedance structure is the G-S-G configuration of 3 wire bonds. The wire bonds are designed to be adjacent to each other and maintain the same center-to-center pitch as they pass from die-to-die. We call this a *coplanar wire bond structure* because the wire bonds are always parallel to each other and on the same plane along all cross-sections of the structure. By always using the center wire as the signal and the two outer wires as the grounds (or return), a controlled impedance structure is created. Figure 2 shows the critical dimensions of the two controlled impedance structures in this system. In the coplanar structure,  $\epsilon_{r1}$  represents the electric permittivity of the material above the traces and  $\epsilon_{r2}$  is the permittivity of the substrate (typically Silicon). In the wire bond structure,  $\epsilon_{r-pkg}$  is the permittivity of the package encapsulate. In most cases,  $\epsilon_{r1}$  will be the same as  $\epsilon_{r-pkg}$ .

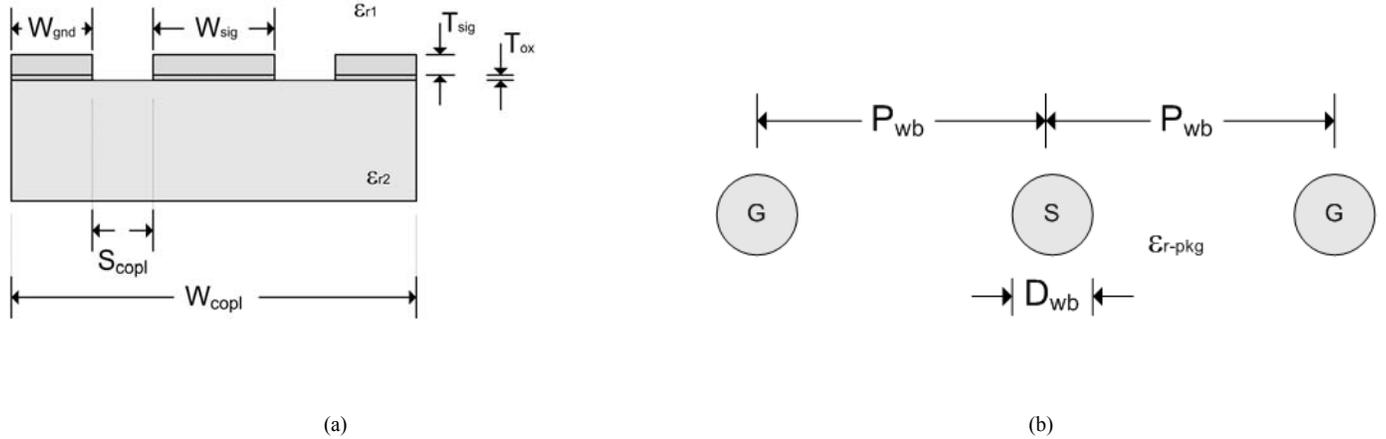


Fig. 2. Critical dimensions for the on-chip coplanar traces (a) and the off-chip coplanar wire bond (b) structures.

The design of this system involves selecting the dimensions for the interconnect structures in order to achieve the designed characteristic impedance. For the coplanar structure,  $T_{\text{sig}}$ ,  $T_{\text{ox}}$ ,  $\epsilon_{r1}$ , and  $\epsilon_{r2}$  are dictated by the IC fabrication and packaging process. This leaves  $W_{\text{sig}}$ ,  $W_{\text{gnd}}$ , and  $S_{\text{copl}}$  as the only design variables. For the wire bond configuration, the diameter of the wire bond ( $D_{\text{wb}}$ ) can be chosen by using different commercially available wire products. These typically range from  $25\mu\text{m}$ - $75\mu\text{m}$  in diameter. The pitch of the wire ( $P_{\text{wb}}$ ) is a design variable. The interfacing of the controlled impedance wire bond structure to the on-chip coplanar structures requires that the pitch of the two outer ground wires align with the two outer coplanar traces. This sets a design constraint for the on-chip structure.

We performed a case study using three different diameters of wire ( $25\mu\text{m}$ ,  $50\mu\text{m}$ , and  $75\mu\text{m}$ ). For each of these diameters we designed both  $50\Omega$  and  $75\Omega$  transmission line structures assuming an encapsulate permittivity of  $\epsilon_{r\text{-pkg}}=4.3$  [7]. For the corresponding wire bond pitch ( $P_{\text{wb}}$ ) that gave the desired impedance, we calculated the coplanar structure dimensions that would interface to the wire bonds assuming a Silicon substrate and  $\epsilon_{r1}=\epsilon_{r\text{-pkg}}$ . Fig 3 shows a plot of the corresponding pitch and diameters to achieve  $50\Omega$  and  $75\Omega$  impedances in the wire bond structure. Table I shows the corresponding coplanar structure dimensions to achieve  $50\Omega$  and  $75\Omega$  while also aligning to the wire bonds. The sizes illustrated in this table show that this type of controlled impedance approach uses approximately the same amount of area as the traditional perimeter placed wire bond pads.

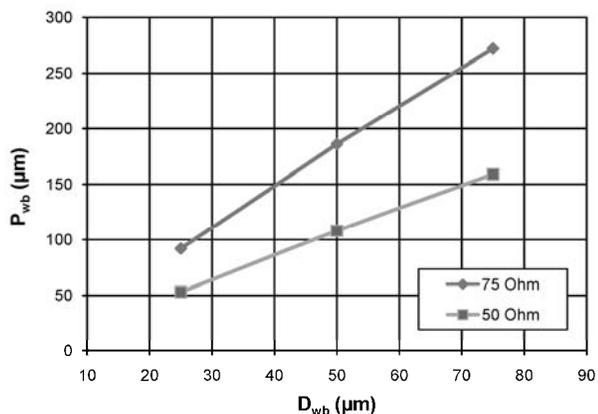


Fig. 3. Pitch vs. Diameter for the controlled impedance coplanar wire bond structure showing both a  $50\Omega$  and  $75\Omega$  system.

| Structure   | Param             | Units         | Dimensions  |     |     |             |     |     |
|---|-------------------|---------------|-------------|-----|-----|-------------|-----|-----|
|   |                   |               | 50 $\Omega$ |     |     | 75 $\Omega$ |     |     |
| Wire Bond<br>( $\epsilon_{r\text{-pkg}}=4.3$ )                  | $D_{\text{wb}}$   | $\mu\text{m}$ | 25          | 50  | 75  | 25          | 50  | 75  |
|   | $P_{\text{wb}}$   | $\mu\text{m}$ | 53          | 108 | 159 | 92          | 186 | 272 |
| Coplanar<br>( $\epsilon_{r1}=4.3$ )<br>( $\epsilon_{r2}=11.7$ ) | $T_{\text{sig}}$  | $\mu\text{m}$ | 1           | 1   | 1   | 1           | 1   | 1   |
|   | $T_{\text{ox}}$   | $\mu\text{m}$ | 1           | 1   | 1   | 1           | 1   | 1   |
|   | $W_{\text{sig}}$  | $\mu\text{m}$ | 26          | 48  | 74  | 24          | 44  | 76  |
|   | $W_{\text{gnd}}$  | $\mu\text{m}$ | 50          | 100 | 150 | 50          | 100 | 150 |
|   | $S_{\text{copl}}$ | $\mu\text{m}$ | 30          | 68  | 94  | 110         | 228 | 318 |

Table I. Dimensions for the matched impedance interconnect system for three sizes of commercially available wire bonds.

### III. FINITE ELEMENT ANALYSIS (FEA) RESULTS

Finite Element Analysis was performed on our design to evaluate the loss through the coplanar and wire bond structures. The *Electromagnetic Design System (EMDS)* from *Agilent Technologies, Inc* was used for the FEA simulations. This analysis was performed on two different wire bond materials, Aluminium and Gold. The coplanar structures were designed using Aluminium traces above a thin layer of Silicon Oxide ( $\text{SiO}_2$ ). The system evaluated consisted of two dies, each containing 3mm coplanar traces which were connected together by 3mm wire bonds. Fig 4-7 show the S-parameter responses of each of the configurations evaluated. Fig 4 and Fig 5 give the transmitted response for a  $50\Omega$  and  $75\Omega$  system using Aluminum wires. Fig 6 and Fig 7 give the transmitted response for a  $50\Omega$  and  $75\Omega$  system using Gold wires. In all cases, the loss of the system remains above  $-2.2\text{dB}$  up to  $20\text{GHz}$ . The  $75\Omega$  systems outperform the  $50\Omega$  systems due to the inherent advantage of lower loss in higher impedance systems. The Gold wire bonds outperform the Aluminum wire bonds due to the increased conductivity of the metals.

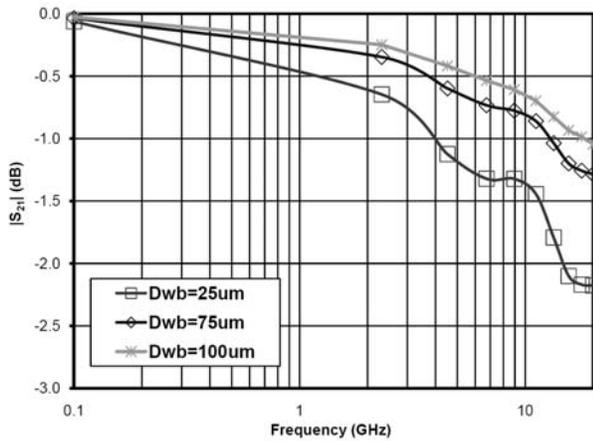


Fig 4.  $|S_{21}|$  response for the 50 $\Omega$  system with Aluminum wire bonds

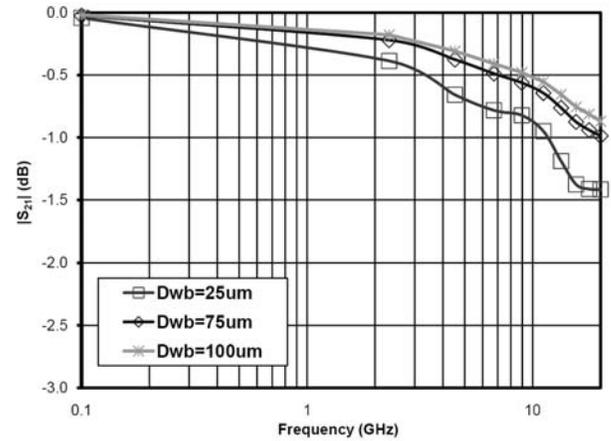


Fig 5.  $|S_{21}|$  response for the 75 $\Omega$  system with Aluminum wire bonds

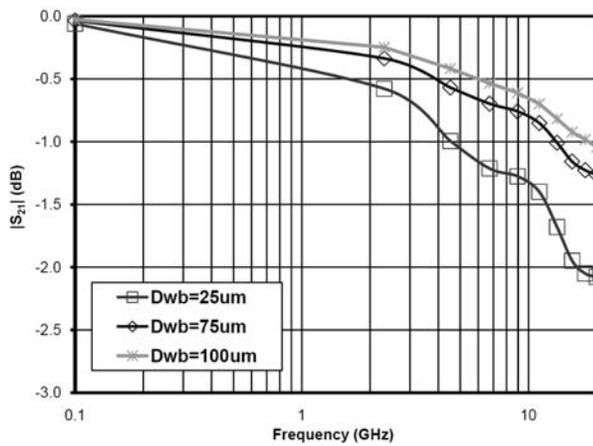


Fig 6.  $|S_{21}|$  response for the 50 $\Omega$  system with Gold wire bonds

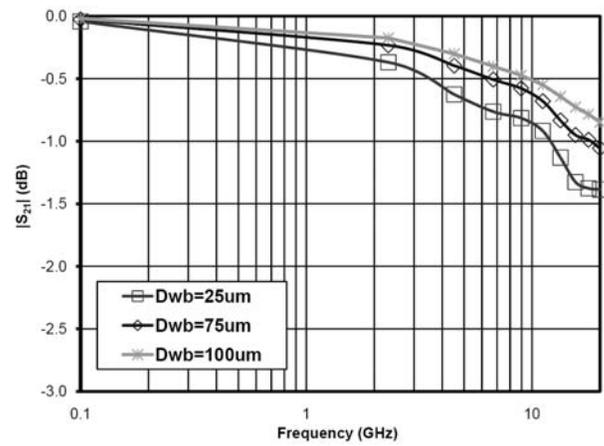


Fig 7.  $|S_{21}|$  response for the 75 $\Omega$  system with Gold wire bonds

#### IV. CONCLUSION

In this paper we presented a chip-to-chip interconnect system that consists of on-chip coplanar transmission lines and off-chip, coplanar wire bonds. This system provides a fully matched impedance signal path for high speed nets in SiP applications. The design of the system was presented for both 50 $\Omega$  and 75 $\Omega$  configurations. FEA was performed to analyze the loss of the system for Aluminum and Gold wire bonds. This system promises to deliver the off-chip electrical performance required by future mobile computing applications while still using existing manufacturing processes.

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