Position Sensitive Radiation Detector Integrated with an FPGA for Radiation Tolerant Computing

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Abstract

A position sensitive radiation sensor was modeled, developed and fabricated then interfaced with a field programmable gate array (FPGA) to create a radiation hardened computing platform. The system exploits environmental information from the sensor in order to determine regions within the FPGA that may have been affected by radiation. The spatial radiation sensor provides the computer system with the location of radiation strikes. This information is used by the computer system to avoid and repair effected circuits on the programmable fabric. By giving the recovery circuitry insight into the location where a fault may have occurred, the latency between detection of a fault and repair can be reduced. This provides an additional level of reliability by more efficiently detecting and correcting faults in SRAM-based FPGAs faults compared to the traditional voting and sequential search approaches.

Spatial Radiation Sensor Design

Sensing Element

A 12x12, XY strip detector configuration is used on top of a PN sensing element.

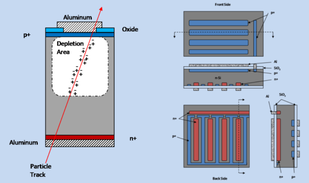

Fig 3. Cross-section, top, and bottom view of sensor.

FEA Simulations of electron/hole Generation

COMSOL FEA simulation of electron/hole generation for a particle striking the sensor.

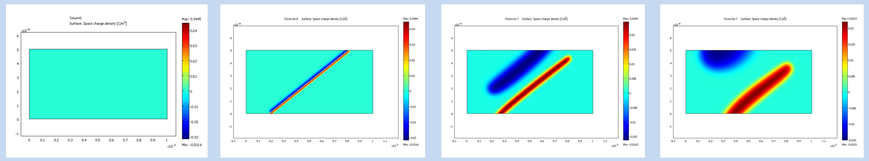

Fig 4. Electron/hole pair generation at t=0 (left), t=30ns (middle-left), t=100ns (middle-right), and t=200ns (right)

Simulated Output Pulse

COMSOL simulation of transient pulses due to electrons and holes

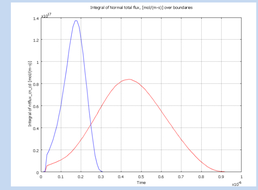

Fig 5. Transient Pulse Generated by electron (blue) and holes (red)

Many-Core Computer System

A 4x4 array of soft processors are implemented on an FPGA. At any given time, three processors run in triple modulo redundancy. If the sensor detects a potential fault in a processor, it is replaced with a spare processor and normal operation resumes. The damaged processor is then replaced in the background using partial reconfiguration of the configuration SRAM. The system was prototyped using a *picoBlaze* soft processor implemented on a Xilinx Virtex-5 LX110 FPGA.

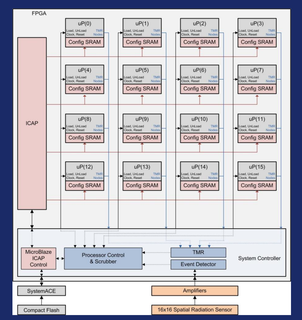

Fig 1. Block Diagram of 16-Processor System.

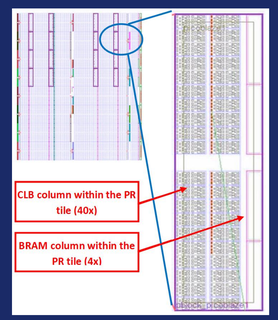

Fig 2. FPGA floor plan showing the resources used by each of the reconfigurable tiles.

Sensor Fab & Characterization

A 12x12 channel, 15mm X 15mm sensor was fabricated at the Montana Microfabrication Facility at MSU. The sensor was tested using both 5mW HeNe and 1064nm lasers.

Fig 6. Prototype sensor attached to package PCB.

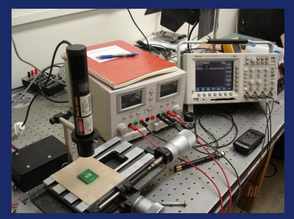

Fig 7. Lab setup for testing

TABLE 1. CURRENT FROM 5mW HeNe LASER

I (uA)	Target Channel											
Observation Channel	1	2	3	4	5	6	7	8	9	10	11	12
1	41	39	-	35	31	30	30	28	25	24	22	19
2	37	43	-	38	33	32	32	29	27	25	23	19
3	-	-	-	-	-	-	-	-	-	-	-	-
4	30	35	-	40	36	34	34	31	28	26	24	20
5	29	31	-	36	39	35	35	32	29	27	25	20
6	26	28	-	33	35	36	37	34	30	28	26	21
7	23	25	-	29	31	33	38	37	32	29	27	22
8	19	22	-	26	27	29	35	41	34	32	28	23
9	16	18	-	22	23	25	30	34	34	35	29	24
10	14	15	-	19	20	21	26	29	30	40	32	27
11	12	13	-	11	17	18	22	24	26	32	34	29
12	11	12	-	9	15	16	19	21	23	27	30	31

TABLE 2. VOLTAGE FROM 5mW HeNe LASER

V (mV)	Target Channel											
Observation Channel	1	2	3	4	5	6	7	8	9	10	11	12
1	146	142		127	113	109	110	104	94	90	84	70
2	155	152		133	120	115	115	106	98	93	86	72
3	-	-		-	-	-	-	-	-	-	-	-
4	114	124		142	130	123	121	114	103	97	90	75
5	103	113		132	139	127	127	118	107	100	92	76
6	93	101		119	127	130	135	124	111	103	95	78
7	82	90		106	112	118	138	134	116	108	98	80
8	72	78		94	99	105	126	148	123	116	103	84
9	62	68		82	86	92	109	123	121	119	108	89
10	52	57		71	74	79	94	105	110	144	116	97
11	44	48		60	63	68	81	89	95	116	122	106
12	40	44		54	57	61	72	78	84	100	110	115

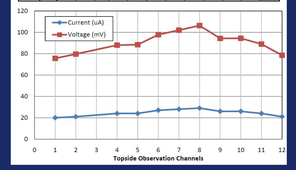

Fig 8. Channel responses when striking channel 8

System Integration & Test

An amplifier board was created to take the low energy signals from the sensor and convert them into full swing digital signals that could be read by the FPGA. A GUI was created to monitor the information coming out of the sensor as seen by the FPGA. This corresponds to the locations of the processors that are being faulted and need to be relocated and repaired.

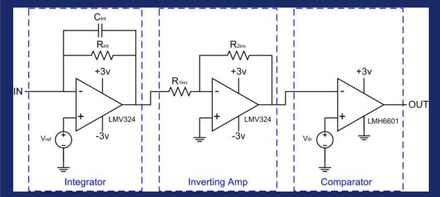

Fig 9. Amplifier circuit for pulse processing.

Fig 10. Amplifier Board containing 24 channels.

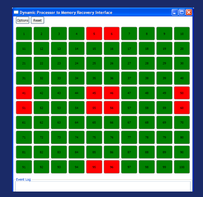

Fig 11. GUI showing location of radiation strikes (red)

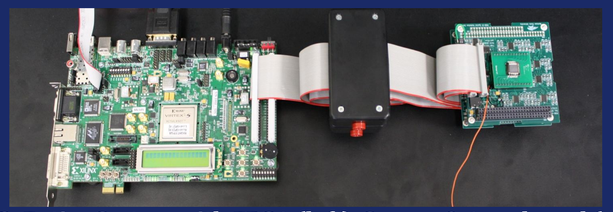

Fig 13. Entire System with FPGA (left), Sensor & Amp board (right) and clamping diode box (middle)

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