Power Efficiency Benchmarking of a Partially Reconfigurable, Many-Tile System Implemented on a Xilinx Virtex-6 FPGA

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Abstract

Field Programmable Gate Arrays are an attractive platform for reconfigurable computing due to their inherent flexibility and low cost relative to custom integrated circuits. This poster presents the performance and power efficiency of a variety of standard benchmarks implemented on a Xilinx Virtex-6 75k device using a reconfigurable computing architecture. The architecture provides the ability to instantiate processing units in real-time using partial reconfiguration. This allows multiple processors and/or hardware accelerators to be brought online as the application requires. Additionally, this realizes increased power efficiency by deactivating unused tiles thereby reducing static power consumption. This paper presents the performance and power efficiency of a custom reconfigurable computer architecture implemented on a Virtex-6 board for Dhrystone, Whetstone, LINPACK, and NAS-EP benchmarks.

Introduction

FPGAs in Reconfigurable Computing

- FPGAs have emerged as the platform of choice for reconfigurable computing due to:
  - Design flexibility
  - Runtime reconfiguration
  - Abundant logic resources
  - Cost savings over ASICs

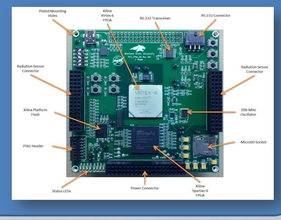
Many-Tile Computer System

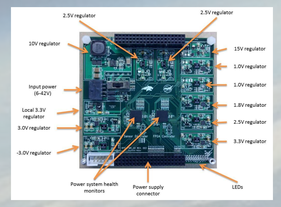
- FPGA logic resources are partitioned into many partially reconfigurable regions, called “tiles”
- Unused tiles are left deprogrammed thereby reducing static power
- Tiles are configured on an as-needed basis either as a MicroBlaze soft processor, or as a hardware accelerator core, using active partial reconfiguration
- Computationally intensive, parallelizable tasks are offloaded to custom hardware cores for higher performance over soft processors
- Real-time power consumption is recorded to determine Performance-per-Watt metric

Research Hardware

FPGA Board

- Xilinx Spartan-6 XC6SLX75 control FPGA
- Xilinx Virtex-6 XC6VLX75T main FPGA
- Active partial reconfiguration of the Virtex-6 via SelectMAP 8-bit parallel configuration interface
- Configuration memory readback and scrubbing
- MicroSD card to store full and partial bitstreams
- USB and RS-232 serial communication interfaces





Power Supply Board

- Real-time voltage, current and power measurement
- 12 dynamically configurable voltage rails
- Over-current detection with automatic shutdown
- 6V to 42V input voltage supply range

System Architecture

Control FPGA

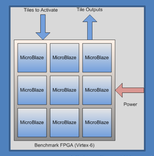
- Activates/deactivates cores on the main FPGA
- Transmits benchmark data to PC user interface

Main FPGA

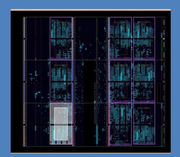
- Implements the architecture being benchmarked
- 9-tile agnostic system

User PC

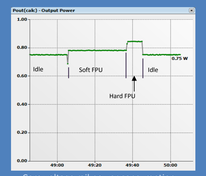
- Logs benchmark results and power consumption



Virtex-6 partitioned into 9 reconfigurable tiles



TI FUSION Power Designer Monitor GUI



Core voltage rail power consumption with double precision LINPACK

Results

Benchmark performance results for Dhrystone, Whetstone and LINPACK with a system clock of 120MHz

Benchmark	FPGA Tile Configuration	
	Single Core	Single Core with Floating Point Hardware Accelerator
Dhrystone	122 DMIPS	n/a
Whetstone (single precision)	6.3 MFLOPS	n/a
LINPACK (single precision)	11.3 MFLOPS	n/a
LINPACK (double precision)	0.31 MFLOPS	1.9 MFLOPS

- Single MicroBlaze core
- 120-MHz system clock
- Single precision operations use native ALU support
- Double precision operations use custom FPU

- Benchmark results normalized to 1-MHz clock frequency
- Addition of FPU accelerator results in ~450% improvement

Benchmark performance results for Dhrystone, Whetstone and LINPACK normalized to a system clock of 1MHz

Benchmark	FPGA Tile Configuration	
	Single Core	Single Core with Floating Point Hardware Accelerator
Dhrystone	1.01 DMIPS/MHz	n/a
Whetstone (single precision)	52.5 KFLOPS/MHz	n/a
LINPACK (single precision)	94.2 KFLOPS/MHz	n/a
LINPACK (double precision)	2.9 KFLOPS/MHz	15.8 KFLOPS/MHz

Benchmark power efficiency for Dhrystone, Whetstone and LINPACK with a system clock of 120 MHz

Benchmark	FPGA Tile Configuration	
	Single Core	Single Core with Floating Point Hardware Accelerator
Dhrystone	200 DMIPS/Watt	n/a
Whetstone (single precision)	10.3 MFLOPS/Watt	n/a
LINPACK (single precision)	18.5 MFLOPS/Watt	n/a
LINPACK (double precision)	0.51 MFLOPS/Watt	3.1 MFLOPS/Watt

- Power efficiency for Dhrystone, Whetstone and LINPACK benchmarks
- 500% increase in performance efficiency with accelerator core

- Performance results for NAS-EP with varying number of instantiated cores
- Linear speedup is noted with a minimal power increase

Benchmark performance results for NAS-EP with a system clock of 120MHz

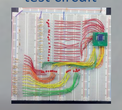
FPGA Tile Configuration	Results (2^{20} Iterations)			
	Completion Time	Speed Up Over 1 Core	Power Consumption	Power Increase Over 1 Core
1 Core	393 s	-	610mW	-
2 Cores	195 s	202%	618mW	1.3%
3 Cores	131 s	300%	626mW	2.6%
4 Cores	97 s	405%	634mW	3.9%
5 Cores	77 s	501%	642mW	5.2%

Conclusions

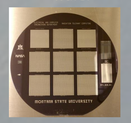
- Montana State University’s Many-Tile, Partially Reconfigurable Computing Platform has been developed and tested
- Hardware accelerator tiles were implemented to demonstrate power efficiency and performance using Dhrystone, Whetstone, LINPACK, and NAS-EP benchmark routines
- Hardware cores demonstrated increased performance over MicroBlaze system
- Additional cores increased performance with minimal increases in power consumption

Research Timeline

Early computer system on development boards

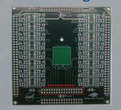


Radiation sensor test circuit



Radiation sensor wafer

Packaged radiation sensor

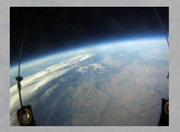


Sensor signal conditioning PCB

Integrated sensor/FPGA development system

1st & 2nd sounding balloon flights (~90k ft) MSGC BOREALIS

1st & 2nd radiation tests at Texas A&M cyclotron facility



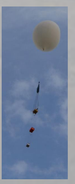
3rd & 4th sounding balloon flights (~90k ft) MSGC BOREALIS

RockOn sounding rocket training program

Custom research hardware finished

5th sounding balloon flight (~120k ft) NASA/LSU HASP

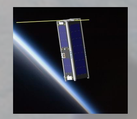
3rd radiation test at Texas A&M cyclotron facility



6th & 7th sounding balloon flights (~90k ft) MSGC BOREALIS

8th sounding balloon flight (~120k ft) NASA/LSU HASP

1st suborbital rocket flight ~100 mi..



CubeSat development, orbital testing

2010 2011 2012 2013 2014