



Overview

The purpose of this project is to **develop and test** a set of adaptive learning course materials to address background deficiencies in computer engineering. The interventions proposed will target a sequence of introductory digital logic courses that are found in every ABET accredited computer engineering program.

Motivation

Can an adaptive, e-learning environment that provides personalized instruction improve student understanding of computer engineering?

Student Interest – Students lose interest when course material is *either* too hard **or** too easy.

Background Deficiencies - Students often lack the necessary prerequisite knowledge in introductory engineering courses due to their varied backgrounds and different high school curricula.

Large Entry-Level Courses – The sheer number of students in introductory courses prevents teachers from providing personalized instruction.

Remote Delivery – Online instruction often lacks the instructor interaction that can be provided in a live offering.

Project Plan

- 1) Create introductory-level logic circuits curriculum.
- 2) Analyze baseline level of understanding and identify sections suitable for adaptive learning.
- 3) Develop and test impact of adaptive learning.
- 4) Refine modules based on mixed-method data.



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Page 6:		OF		
13		OF		
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Measuring the Impact of Adaptive Learning **Modules in Digital Logic Courses**

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2) Baseline Understanding

9	Learning Outcome				Perfo	rmanc '	: e on l "200-Lev	
odule is to:	After completing this module, a student will be able to:	Avg	200-Level (n=176)					
sic ystems.	1.1: Describe the fundamental differences between analog and digital systems.	Mod 1 (n=176)	1.1	-				
	1.2: Describe advantages of digital systems compared to analog systems.		1.2	-				
sic ems.	2.1: Describe the formation and use of positional number systems.		2.1	-				
	2.2: Convert numbers between different bases.	Module 2 (n=176)	2.2					
	2.3: Perform binary addition and subtraction by hand.	1 [₽] [⊆]	2.3	- 1				
	2.4: Use two's complement numbers to represent negative numbers.	1 —	2.4	-				
sic electrical	3.1: Describe the functional operation of a basic logic gate using truth tables, logic expressions, and logic waveforms.	<u>و</u>) ش	3.1					
	3.2: Analyze the DC and AC behavior of a digital circuit to verify it is operating within specification.	Module 3 (n=176)	3.2	-				
ľ	3.3: Describe the meaning of a logic family and the operation of the most common technologies used today.	- ^{≥ -}	3.4	- 1				
	3.4: Determine the operating conditions of a logic circuit when driving various types of loads.	1 —	4.1	-				
sic	4.1: Describe the fundamental principles and theorems of Boolean algebra.		4.2	- 1				
design.	4.2: Analyze a combinational logic circuit to determine its logic expression, truth table, and timing information.	Module 4 (n=176)	4.3	- 1				
	4.3: Synthesis a logic circuit in canonical form (Sum of Products or Product of Sums) from a functional description.	ٿ ¥	4.4					
	4.4: Synthesize a logic circuit in minimized form (Sum of Products or Product of Sums).		4.5					
	4.5: Describe the causes of timing hazards in digital logic circuits and the approaches to mitigate them.		5.1					
sic on -	5.1: Describe the role of hardware description languages in modern digital design.		5.2					
	5.2: Describe the fundamentals of design abstraction in modern digital design.	e ⁵	5.3					
	5.3: Describe the modern digital design flow based on hardware description languages.	Module 5 (n=176)	5.4					
	5.4: Describe the fundamental constructs of VHDL.	1 ²	5.5					
	5.5: Design a VHDL model for a combinational logic circuit using concurrent modeling techniques.		5.6					
	5.6: Design a VHDL model for a combinational logic circuit using a structural design approach.	1	5.7	-				
	5.7: Describe the role of a VHDL test bench.	9_	6.1	-				
sic rated circuit -	6.1: Design a decoder circuit using both the classical digital design approach and the modern HDL-based approach.	Module 6 (n=176)	6.2	-				
	6.2: Design an encoder circuit using both the classical digital design approach and the modern HDL-based approach.		6.3	-				
	6.3: Design a multiplexer circuit using both the classical digital design approach and the modern HDL-based approach.	1 —	7.1	-				
	6.4: Design a demultiplexer circuit using both the classical digital design approach and the modern HDL-based approach.		7.2	- 1				
sic	7.1: Describe the operation of a sequential logic storage device.	1	7.3	-				
uits.	7.2: Describe sequential logic timing considerations.	Module 7 (n=176)	7.4					
	7.3: Design a variety of common circuits based on sequential storage devices.	ٿ ¥	7.5					
-	7.4: Design a finite state machine using the classical digital design approach.		7.6					
	7.5: Design a counter using the classical digital design approach and using an HDL-based, structural approach.		7.7					
	7.6: Describe the finite state machine reset condition.			40 45	50	55	60	65
	7.7: Analyze a finite state machine to determine its functional operation and maximum clock frequency.							
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3) Adaptive Learning Modules

Learning outcomes 4.4 (Logic Minimization) and 5.5 (VHDL Concurrent Signal Assignments) were selected for intervention due to high-level of student confusion observed by instructors. Modules pilot tested in fall-16, spring-17, and summer-17 on students from three universities. Performance on subsequent homework was measured and focus groups were conducted.

Everyone must pass the module at a level of "Proficient". However, if you need a little background refresher, there are "Basic Level" activities that will catch you up. The first step is to decide whether you should start at the "Basic" or	Conclusion
<complex-block> Hereicher Bescher bescher Kinnen für Statute statute inter Bescher Hereicher Hereicher Bescher Hereicher Hereicher Bescher Hereicher Hereicher</complex-block>	 A significant improvement in the homework score was observed for a GPAs between 2.5-3.0. This confilearning can help with background d Majority of results were damped by so it isn't clear if modules are impacted. Focus groups revealed students was to be optional, multi-mode (both the and are not necessary for every sected. A module for section 7.4 is necessary.

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in the associated ved for students with is confirms adaptive round deficiencies. nped by ceiling effect, e impacting <u>mastery</u>. ents wanted modules (both text & video), very section.

