Design & Evaluation of a Multipurpose Course Structure for Teaching Digital Logic

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Design & Evaluation of a Multi-Purpose Course Structure for Teaching Digital Logic

Abstract

This paper presents the design and evaluation of a portable course to teach introductory digital logic. The goals of this course are to simultaneously meet existing accreditation criteria while providing a course that has the potential of being administered completely online. The online characteristic of the course gives the instructor the ability to teach the class in numerous delivery modes. These include an asynchronous online delivery or as supplementary resources for a synchronous face-to-face delivery. The inclusion of a low-cost portable lab kit provides additional flexibility by supporting either the traditional 2-hour on-campus lab section or a more asynchronous lab-anywhere mode. This paper will describe the design of the course, the corresponding learning objectives, the supporting learning activities, and the learning assessment. This paper will present student performance comparisons for different delivery modes collected over the past 4 years at a medium-sized land grant university. This paper will also provide data on the impact of an adaptive learning component of the course that was implemented for the more difficult course concepts. The adaptive learning component allows the student to receive additional computer instruction on a topic that varies the level of difficulty based on automated formative assessment. The adaptive learning component of the course was shown to have a significant impact on students with GPAs between 2.5 – 3.0 on one of the outcomes without needing instructor interaction. This work was supported by the National Science Foundation Improving Undergraduate STEM Education (IUSE) program, thus all resources for the course are open to the engineering education community. This paper will be of interest to any engineering educator that teaches digital logic or anyone that has interest in augmenting their current course with online resources or switching to a portable lab kit.

Introduction

Digital logic is a course that can be found in every ABET accredited electrical and computer engineering degree in the US. This subject introduces students to the basic building blocks of modern computer systems and prepares them for more advanced courses in embedded systems. Institutions typically offer dedicated courses in digital circuits while some include the content within their analog circuits sequence. Since digital logic is typically offered in the first or second year of the program and does not have calculus as a prerequisite, it is a course that usually has high enrollments with varied student preparedness levels. These factors contribute to increased instructor time spent on helping students that don't have a strong algebra background.

Digital logic is a subject that is more amenable to online instruction compared to other engineering courses [1]. Without complex, calculus-based derivations, the foundation of digital logic can be effectively taught using instructional videos. This characteristic opens opportunities to help struggling students without consuming excessive instructor time. Whether taught fully online, or in a face-to-face mode, the use of instructional videos provides students a learning resource that can help address background deficiencies. Additionally, the lab component of a digital logic course is becoming increasingly feasible due to the low cost of portable lab equipment and digital development boards. A lab component is critical for most engineering courses because it provides opportunities for the deepest levels of learning [2,3].

There are two barriers that must be addressed when creating a fully portable, digital logic course. The first is how to help students that get *stuck* in an online environment and need additional assistance with learning the material. It is desired to have an online environment that can help these students without relying on instructor inquiries. Second, the portable lab kit must be both comprehensive and low cost to be practical. A portable lab kit that is cost prohibitive to the majority of students is a barrier that limits access to the content and defeats moving to an online delivery mode.

This paper presents a course material for digital logic that can be administered in a fully online format. The course includes a comprehensive set of learning outcomes that mirror the majority of ABET accredited curriculums for this area [4,5]. The course materials to support the learning outcomes include written content (i.e., textbooks), videos, and lab exercises. Assessment tools are provided in the form of multiple-choice questions and design simulations. Finally, a portable lab kit is provided presented that has a cost <$300 US to complete the lab exercises in any location. This is significantly lower in cost than existing portable lab kits used for engineering electronics [6] and has the potential to be used across a number of other electrical and computer engineering courses. The course presented has the potential to expand access to digital logic education to a wide range of learners. Assessment data is also provided across multiple instructional modes and the impact of an adaptive learning system is presented that was shown to help students with background deficiencies.

The Digital Logic Course Material

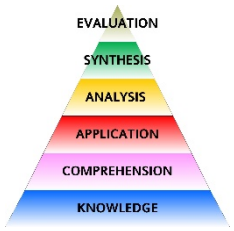
Content Outline

All ABET accredited electrical and computer engineering BS degrees contain some coverage of digital logic circuits. While the breadth and depth of the coverage depends on the university, most digital logic courses contain a coverage of both classical digital design (pen and paper) and the modern digital design flow (VHDL or Verilog). Some universities will cover these topics in a sequence of two courses, or in one accelerated course, or just cover the classical theory in depth and provide an introduction to the HDL-based design in a single class. The course outline designed for the digital logic course is shown in the following list.

- Module 1: Analog vs. Digital
- Module 2: Number Systems
- Module 3: Digital Circuitry & Interfacing
- Module 4: Combinational Logic Design
- Module 5: Introduction to HDLs
- Module 6: Medium Scale Logic (MSI)
- Module 7: Sequential Logic Design
- Module 8: Advanced HDL Modeling
- Module 9: Behavioral Modeling using an HDL
- Module 10: Memory
- Module 11: Programmable Logic
- Module 12: Arithmetic Circuits
- Module 13: Computer Systems

Detailed Learning Outcomes

Table 1 gives the specific learning outcomes developed for the course. Each of the outcomes is designed to be assessed using either multiple-choice questions or through design simulations. The level of learning within Bloom's Taxonomy is also provided for each outcome.



6
5
4
3
2

Learning Objective *The overall learning goal of this module is to:*	Learning Outcome *After completing this module, a student will be able to:*	Learning Category 1	2	3	4	5	6
Module 1: To understand the basic principles of analog and digital systems.	**1.1:** Describe the fundamental differences between analog and digital systems.	x					
	1.2: Describe advantages of digital systems compared to analog systems.	x					
Module 2: To understand the basic principles of binary number systems.	**2.1:** Describe the formation and use of positional number systems.		x				
	2.2: Convert numbers between different bases.			x			
	2.3: Perform binary addition and subtraction by hand.			x			
	2.4: Use twos complement numbers to represent negative numbers.			x			
Module 3: To understand the basic electrical operation of digital circuits.	**3.1:** Describe the functional operation of a basic logic gate using truth tables, logic expressions, and logic waveforms.	x					
	3.2: Analyze the DC and AC behavior of a digital circuit to verify it is operating within specification.				x		
	3.3: Describe the meaning of a logic family and the operation of the most common technologies used today.	x					
	3.4: Determine the operating conditions of a logic circuit when driving various types of loads.				x		
Module 4: To understand the basic principles of combinational logic design.	**4.1:** Describe the fundamental principles and theorems of Boolean algebra and how to use them to manipulate logic expressions.		x				
	4.2: Analyze a combinational logic circuit to determine its logic expression, truth table, and timing information.				x		
	4.3: Synthesize a logic circuit in canonical form (Sum of Products or Product of Sums) from a functional description including a truth table, minterm list, or maxterm list.					x	
	4.4: Synthesize a logic circuit in minimized form (Sum of Products or Product of Sums) through algebraic manipulation or with a Karnaugh map.					x	

	4.5: Describe the causes of timing hazards in digital logic circuits and the approaches to mitigate them.		x				
Module 5: To understand the basic principles of hardware description languages.	**5.1:** Describe the role of hardware description languages in modern digital design.		x				
	5.2: Describe the fundamentals of design abstraction in modern digital design.		x				
	5.3: Describe the modern digital design flow based on hardware description languages.		x				
	5.4: Describe the fundamental constructs of VHDL.		x				
	5.5: Design a VHDL model for a combinational logic circuit using concurrent modeling techniques (signal assignments and logical operators, conditional signal assignments, and selected signal assignments).					x	
	5.6: Design a VHDL model for a combinational logic circuit using a structural design approach.					x	
	5.7: Describe the role of a VHDL test bench.		x				
Module 6: To understand the basic principles of medium scale integrated circuit logic.	**6.1:** Design a decoder circuit using both the classical digital design approach and the modern HDL-based approach.					x	
	6.2: Design an encoder circuit using both the classical digital design approach and the modern HDL-based approach.					x	
	6.3: Design a multiplexer circuit using both the classical digital design approach and the modern HDL-based approach.					x	
	6.4: Design a demultiplexer circuit using both the classical digital design approach and the modern HDL-based approach.					x	
Module 7: To understand the basic operation of sequential logic circuits.	**7.1:** Describe the operation of a sequential logic storage device.		x				
	7.2: Describe sequential logic timing considerations.		x				
	7.3: Design a variety of common circuits based on sequential storage devices (toggle flops, ripple counters, switch debouncers, and shift registers).					x	
	7.4: Design a finite state machine using the classical digital design approach.					x	
	7.5: Design a counter using the classical digital design approach and using an HDL-based, structural approach.					x	
	7.6: Describe the finite state machine reset condition.		x				
	7.7: Analyze a finite state machine to determine its functional operation and maximum clock frequency.				x		
Module 8: To understand the full capability of hardware description languages.	**8.1:** Describe the behavior of a VHDL process and how it is used to model sequential logic circuits.		x				
	8.2: Model combinational logic circuits using a process and conditional programming constructs.					x	

	8.3: Describe how and why signal attributes are used in VHDL models.		x				
	8.4: Design a finite state machine using the classical digital design approach.					x	
	8.5: Describe the capabilities provided by the most common VHDL packages.		x				
Module 9: To understand how hardware description languages can be used to create behavioral models of synchronous digital systems.	**9.1:** Design a VHDL behavioral model for a sequential logic storage device.					x	
	9.2: Describe the process for creating a VHDL behavioral model for a finite state machine.		x				
	9.3: Design a VHDL behavioral model for a finite state machine.					x	
	9.4: Design a VHDL behavioral model for a counter.					x	
	9.5: Design a VHDL register transfer level (RTL) model of a synchronous digital system.					x	
Module 10: To understand the basic principles of semiconductor-based memory systems.	**10.1:** Describe the basic architecture and terminology for semiconductor-based memory systems.		x				
	10.2: Describe the basic architecture of non-volatile memory systems.		x				
	10.3: Describe the basic architecture of volatile memory systems.		x				
	10.4: Design a VHDL behavioral model of a memory system.					x	
Module 11: To understand the basic principles of programmable logic devices.	**11.1:** Describe the basic architecture and evolution of programmable logic devices.		x				
	11.2: Describe the basic architecture of Field Programmable Gate Arrays (FPGAs).		x				
Module 12: To understand the basic principles of binary arithmetic circuits.	**12.1:** Design a binary adder using both the classical digital design approach and the modern HDL-based approach.					x	
	12.2: Design a binary subtractor using both the classical digital design approach and the modern HDL-based approach.					x	
	12.3: Design a binary multiplier using both the classical digital design approach and the modern HDL-based approach.					x	
	12.4: Design a binary divider using both the classical digital design approach and the modern HDL-based approach.					x	
Module 13: To understand the basic principles of a computer system.	**13.1:** Describe the basic components and operation of computer hardware.		x				
	13.2: Describe the basic components and operation of computer software.		x				

Table 1. Detailed Learning Outcomes for the Digital Logic Course

Course Material

Two textbooks were authored to support this course, one using the VHDL language [7] and the other using Verilog [8]. Figure 1 shows the two textbooks published by Springer International in 2016 and 2017. These books currently have a price of ~$60 through amazon.com.

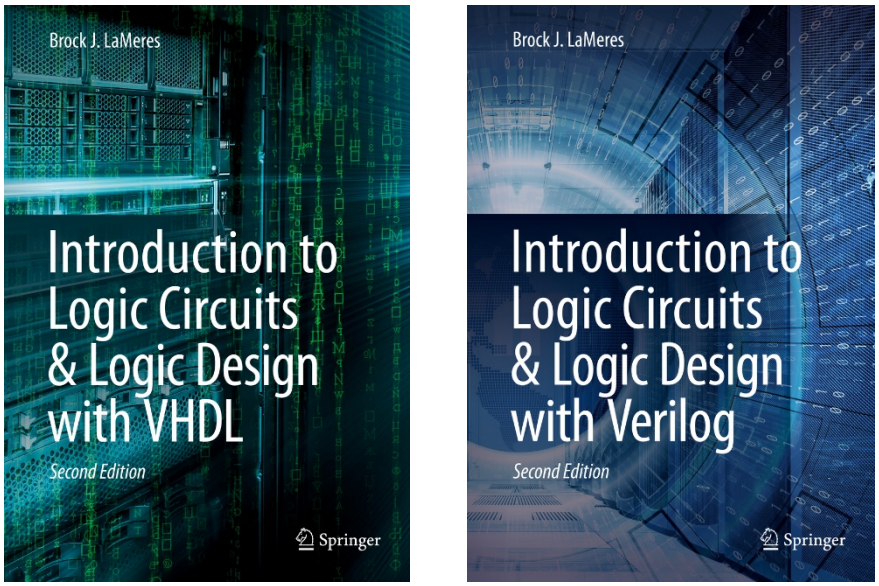


Figure 1. Textbooks Developed for the Digital Logic Course (left = VHDL, right = Verilog).

A series of lecture videos were created to support this sequence using the VHDL language (Verilog videos are under development. These videos consist of pen/paper instruction in addition to HDL coding examples. Figure 2 shows a sample of the video format. These videos are provided for free on online at (http://www.montana.edu/blameres/book_content_vhdl.html).

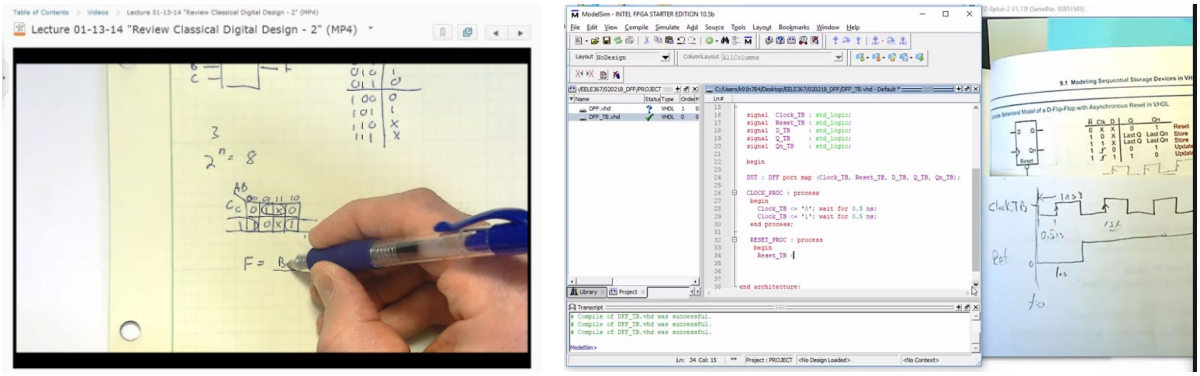


Figure 2. Lecture Videos Developed for the Digital Logic Course (left = pen/paper, right = HDL).

Over 600 assessment tools were developed for the lecture portion of this course. These consisted of questions that could be either worked out by hand or put into a multiple-choice form for online administration. They also included several HDL design/simulation problems. All problems are listed at the end of each chapter in the textbooks. The electronic format of these questions is available through the textbook publisher as an instructor resource. All VHDL solutions and test benches are also available through the publisher. Examples of these problems are shown in Figure 3.

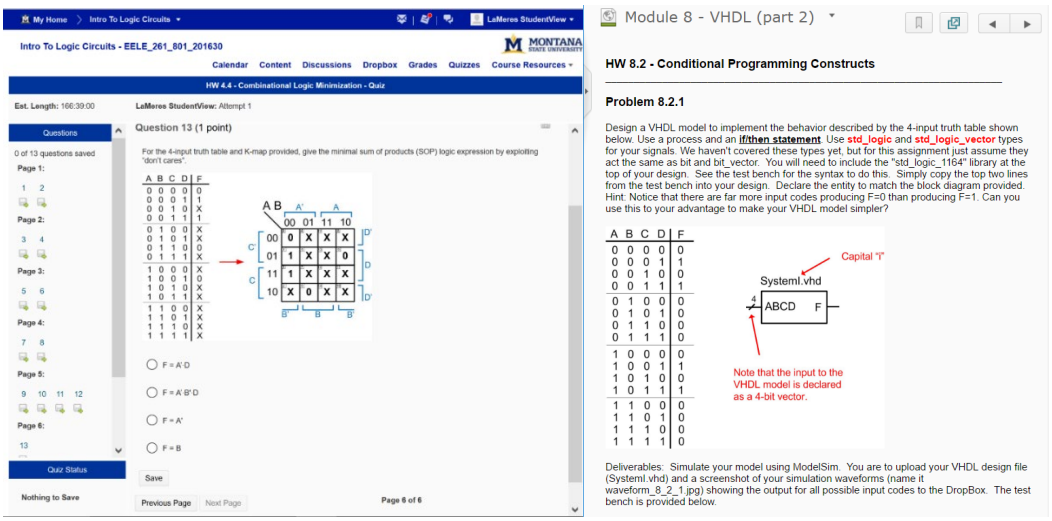


Figure 3. Assessment Tools Developed for the Digital Logic Course

Portable Lab Kit

In order to facilitate the hands-on component of the digital logic course, a portable lab kit was created. The portable lab uses all off-the-shelf components and equipment. The kit consists of a breadboard and discrete logic gates in order to support a hands-on experience with the classical digital design flow. An Altera DE0-CV FPGA board is used to facilitate a hands-on experience with the modern digital design flow using an HDL [9]. The Analog Discovery 2 portable lab system is used to provide the instrumentation for the labs [10]. The material list for the portable lab kit is given in Appendix B. The total cost of this kit is $340 that includes academic pricing for the DE0-CV FPGA board ($99) and for the Analog Discovery 2 ($179). For pilot offerings of this course, a set of these kits were purchased and checked out to the students. This allows the cost to be covered using program fees instead of needing to be purchased by the students. To date the kits have been used in 4 course offerings with minimal damage. The kit fits within a United State Postal Service medium flat rate shipping box (11 1/4" x 8 3/4" x 6"). These boxes are available for free at the USPS and have shipping cost of $12.05 (as of February 2018). Administering the kits was done using a combination of students checking them out in person and having them shipped to their home location. Students were instructed to keep the box in order to return the kit, again either in person or by shipping it back to the instructor. Figures 4 and 5 show various lab configurations using the portable lab kit.

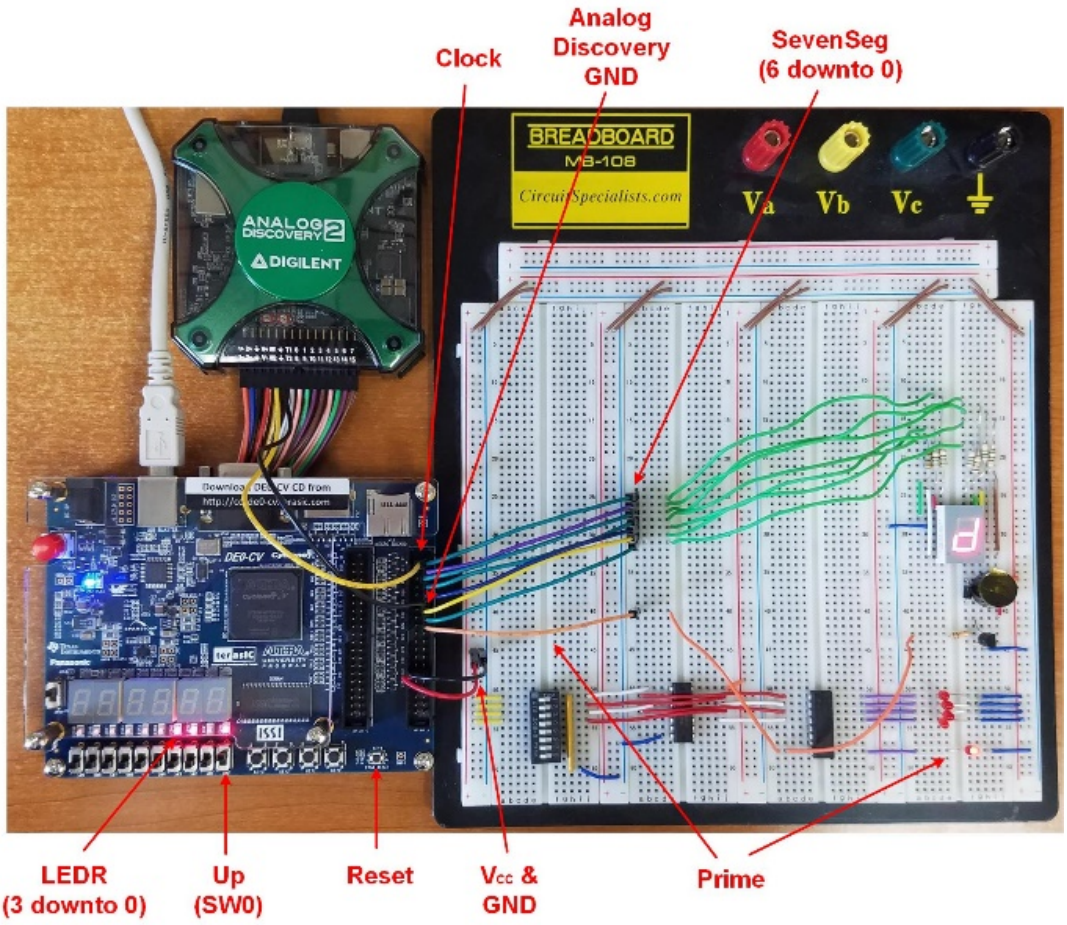


Figure 4. The Portable Lab Kit Showing an Interface between the FPGA board and Discrete Logic.

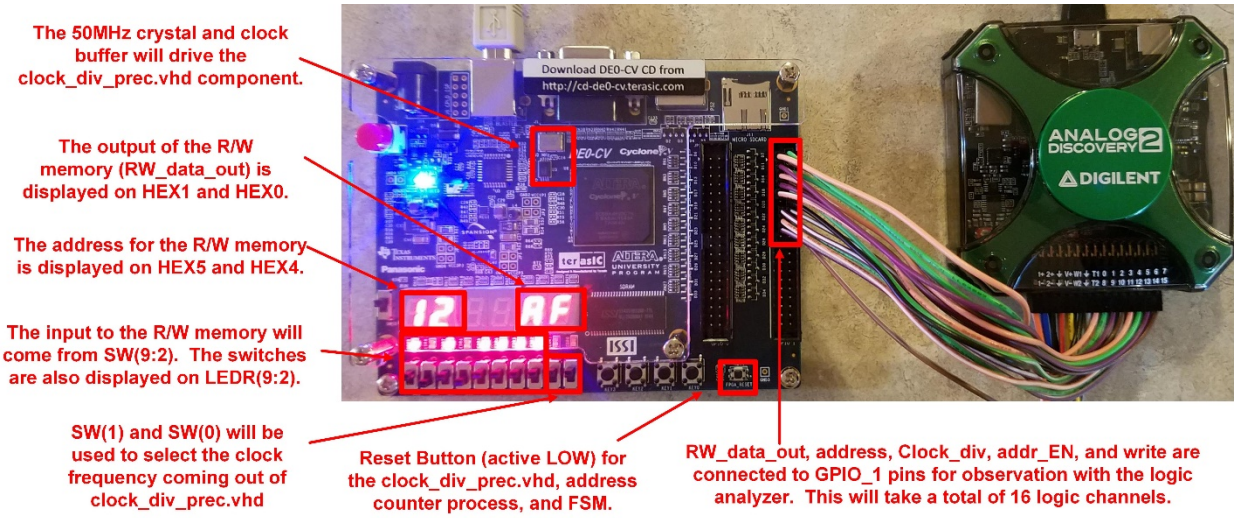


Figure 5. The Portable Lab Kit Showing an Interface between the FPGA board and the Analog Discovery 2.

Student Performance Data

The course was offered in a variety of instructional modes at a 4-year, land grant university in the Pacific Northwest. At this university, the implementation of the course was split across two, 4-credit semester-based courses. The first course was a 200-level (sophomore) class that covered learning modules 1-7. The second course was a 300-level (junior) class that covered learning modules 8-13. Performance data on the learning outcomes was collected across 4 terms of course offerings in different instructional modes. Student demographic information and transcript data was collected for students given consent and the data was analyzed for patterns between student variables and performance. Figure 6 shows one example of how the data was analyzed. This figure shows the overall performance score on each of the learning outcomes for the course of those students that participated.

Figure 7 shows a graphical breakdown of student performance on a specific learning outcome showing the different variables that were considered in the analysis. Variables included major, year in school, semester the course was taken, mode of delivery, gender, age, ethnicity, GPA, SAT scores, ACT scores, credits earned at time of taking the course, transfer vs. non-transfer, and for transfer students, how many credits were transferred.

To evaluate whether the portable lab kit had any impact on student performance in the courses, the student grades for the classes using the portable lab kit was compared to prior courses that used traditional benchtop equipment. The course grade was used as it encompassed the entire learning experience for the students [11]. Figure 8 shows the course grades for four semesters of the 200-level offering that covers modules 1-7. This plot compares a variety of delivery modes for both the lecture and lab of this course including: face-to-face lecture + traditional benchtop equipment for the lab (Fall 2016 & Spring 2017); online lecture + portable lab kit (Summer 2017); and face-to-face lecture + portable lab kit (Fall 2017). This figure shows that there is no statistical difference in student performance in the course across all modes of delivery.

Figure 9 shows the course grades for the three semesters of the 300-level offering that covers modules 8-13. This plot compares a variety of delivery modes for both the lecture and lab of this course including: face-to-face lecture + traditional benchtop equipment for the lab (Spring 2015); and face-to-face lecture + portable lab kit (Spring 2016 & Spring 2017). This figure shows that there is no statistical difference in student performance in the course across all modes of delivery.

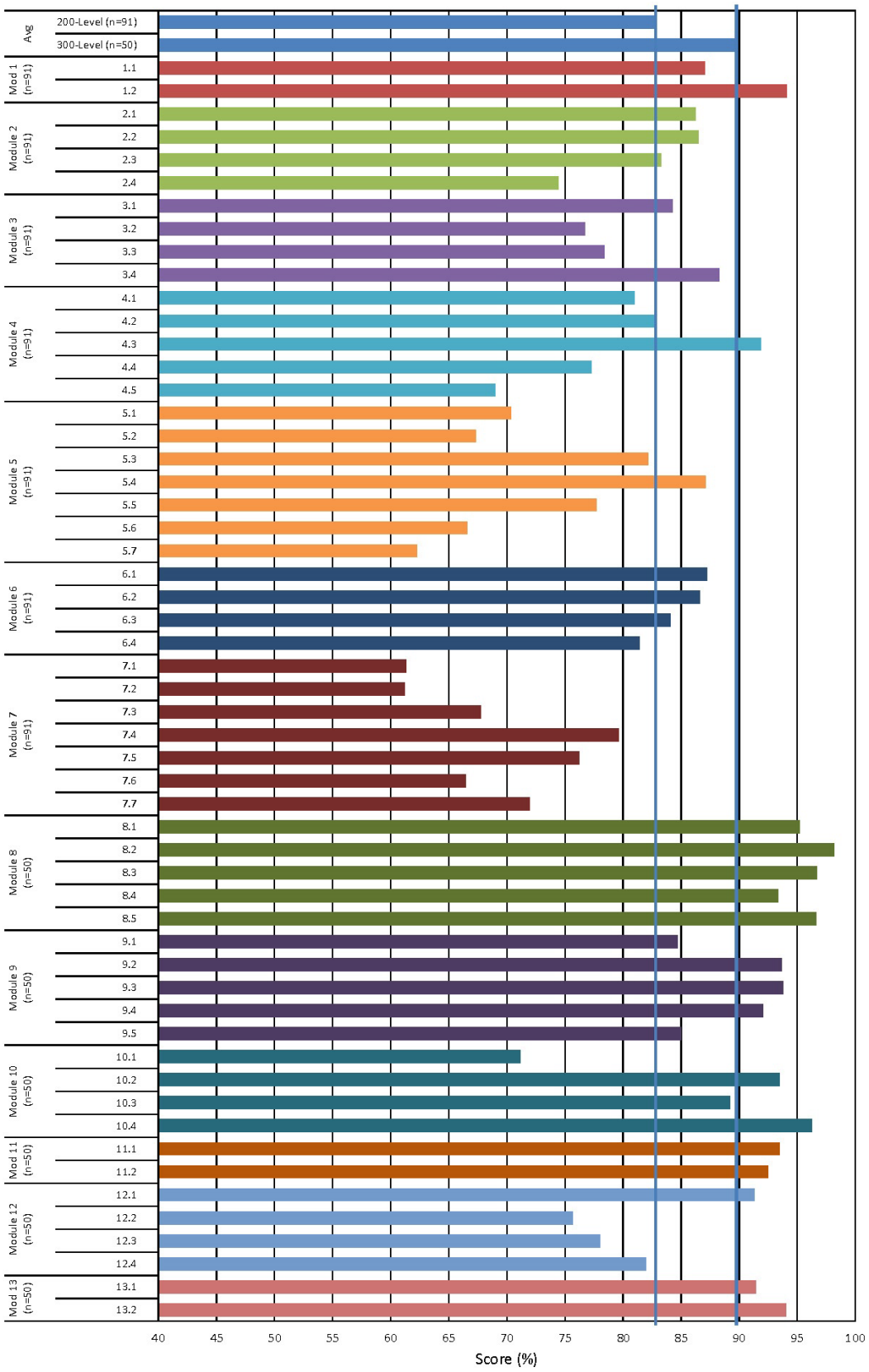


Figure 6. Aggregate Student Performance on Each Learning Outcome

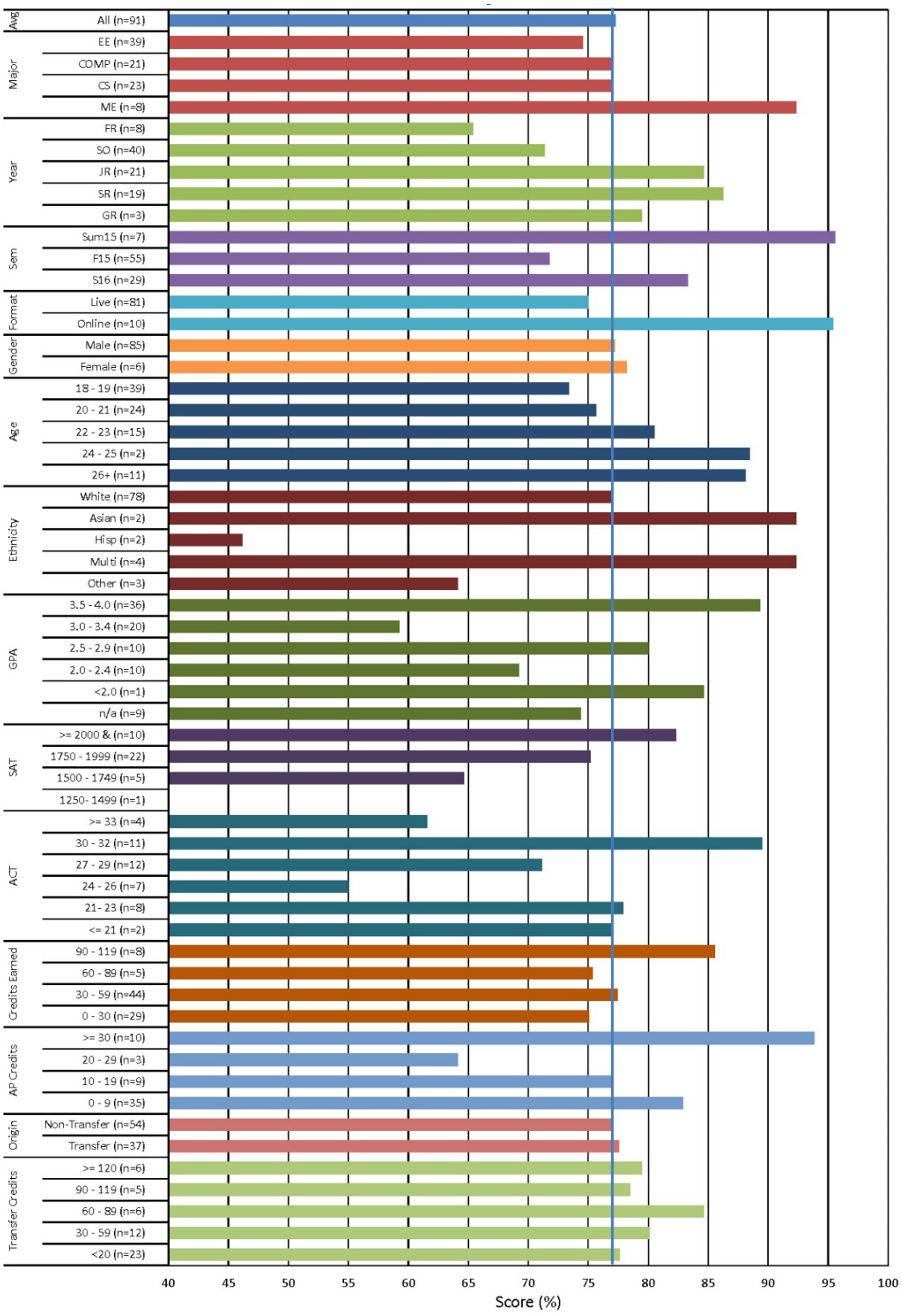
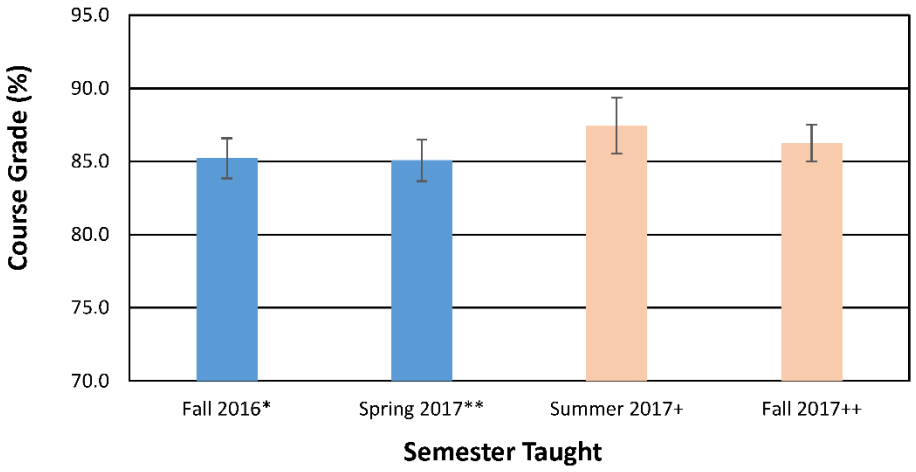
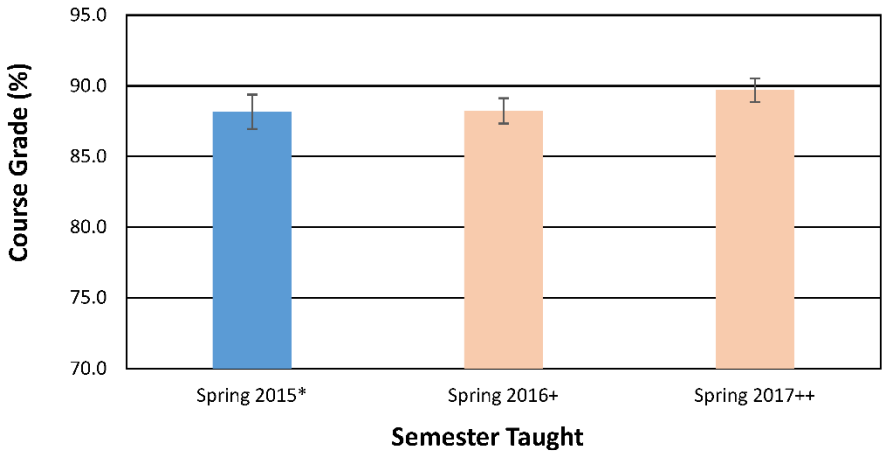


Figure 7. Student Performance on Outcome 4.4: Combinational Logic Synthesis



Note 1: Error bars are +/- 1x Standard Error
* Live Lecture / Benchtop Lab Equipment (N=91, M=85.2, SD=13.1)
** Live Lecture / Benchtop Lab Equipment (N=54, M=85.1, SD=10.5)
+ Online Lecture / Portable Lab Kit (N=25, M=87.5, SD=9.6)
++ Live Lecture / Portable Lab Kit (N=84, M=86.3, SD=11.6)

Figure 8. Student Performance Comparison vs. Delivery Mode for Course Covering Modules 1-7



Note 1: Error bars are +/- 1x Standard Error
* Live Lecture / Benchtop Lab Equipment (N=48, M=88.2, SD=8.4)
+ Live Lecture / Portable Lab Kit (N=50, M=88.1, SD=6.3)
++ Live Lecture / Portable Lab Kit (N=57, M=89.7, SD=6.4)

Figure 9. Student Performance Comparison vs. Delivery Mode for Course Covering Modules 8-13

Adaptive Learning Modules

Based on overall student performance, and time spent on the learning activities, the two most challenging learning outcomes from modules 1-7 were identified. These were:

- 4.4: Combinational Logic Synthesis
- 5.5: Concurrent Modeling of Logic in an HDL

Two adaptive learning activities were created and deployed in the fall semester of 2016 in the 200-level digital logic course. Figure 10 shows an example of the content developed.

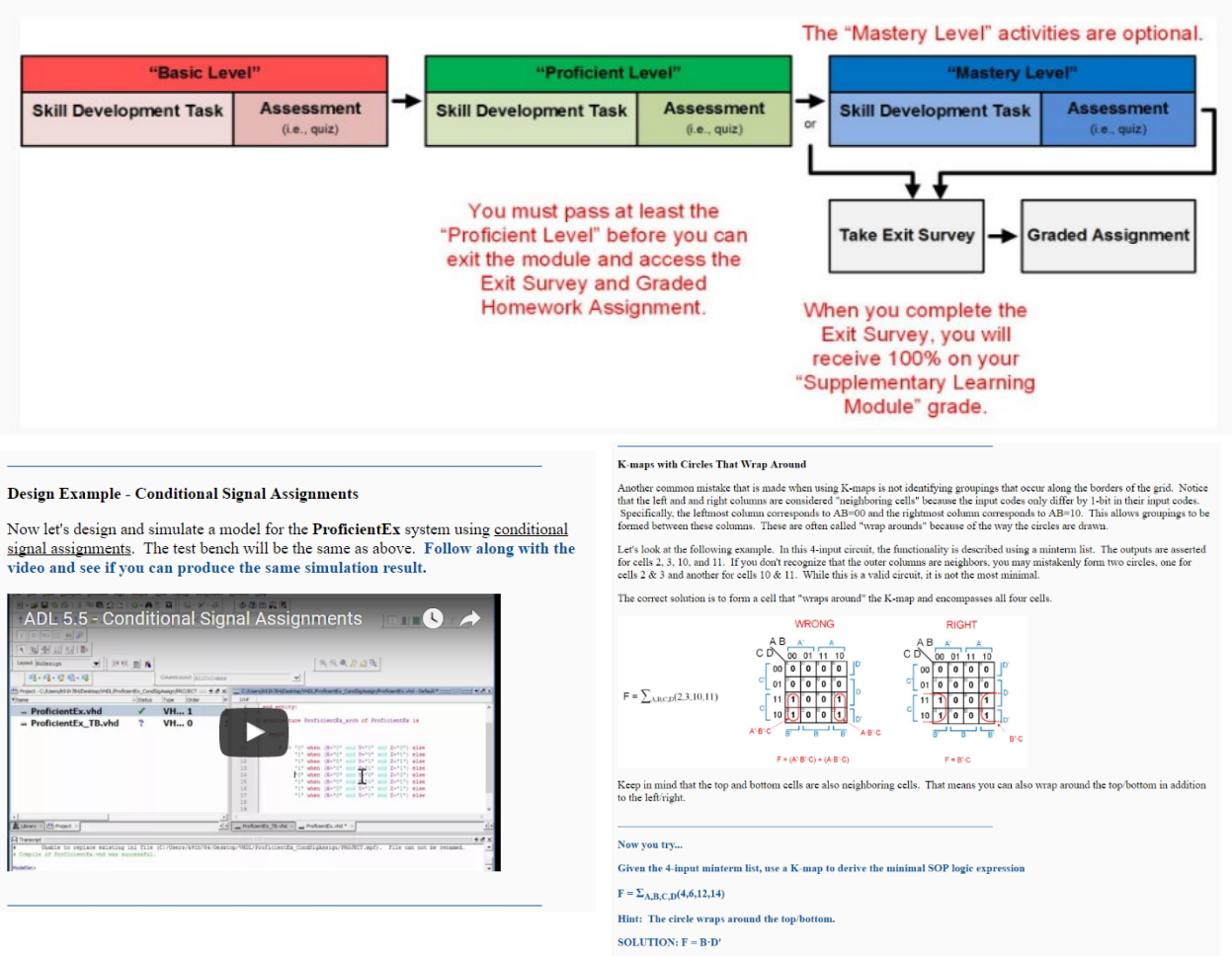


Figure 10. Adaptive Learning Material Developed.

Table 2 gives the average student performance of students that used the adaptive learning modules (EXP = experimental group) and those that did not (BL = baseline group). The Adaptive Learning Modules (ADL) improved the performance of some students on the two outcomes, 4.4 and 5.5. The effect of the intervention was dampened by an overall ceiling effect of the scores on the two homework assignments associated with the outcomes. The total number of points possible for both homework assignments was 100.

Outcome	Baseline Mean	Experimental Mean
4.4	89.86 (n=88)	91.98 (n=71)
5.5	95.29 (n= 81)	95.02 (n= 67)

Table 2. Mean Performance on Targeted Outcomes (Baseline vs. Experimental).

In regard to gender, there were too few female students to conduct any statistical tests. The means for males and females for outcomes 4.4 and 5.5 both BL and EXP are shown in table 3. Females scored quite a bit lower than males on outcome 4.4, but slightly better than males on outcome 5.5.

Outcome	Gender	Baseline	Experimental
4.4	Male	90.60 (n= 81)	92.90 (n=65)
	Female	81.32 (n=7)	82.10 (n=6)
5.5	Male	95.20 (n=76)	94.91 (n=63
	Female	96.67 (n=5)	96.88 (n=4)

Table 3. Mean Grade vs. Gender on Targeted Outcomes (Baseline vs. Experimental).

Using the General Linear Model, which is an ANOVA procedure in which the calculations are performed using a least squares regression approach to describe the statistical relationship between one or more predictors and a continuous response variable, analysis was performed on the Baseline (BL) and Experimental (EXP) results to determine if the intervention affected lower-GPA students differently than the higher-GPA students. The students were grouped as follows:

Group 1: 3.5-4.0 GPA
Group 2: 3.0-3.4 GPA
Group 3: 2.5-2.9 GPA
Group 4: 2.0-2.4 GPA
Group 5: < 2.0 GPA

When these groups and BL/EXP were used as independent variables and the 4.4 outcome was used as the dependent variable, we found a significant interaction ($F = 2.89$; $p = .038$). See table 4 for detailed results.

Analysis of Variance for HW 4.4, using Adjusted SS for Tests

Source	DF	Seq SS	Adj SS	Adj MS	F	P
MSU GPA Group	3	581.2	604.5	201.5	1.72	0.165
BL or EXP	1	120.6	47.7	47.7	0.41	0.524
MSU GPA Group*BL or EXP	3	1013.5	1013.5	337.8	2.89	**0.038**
Error	131	15311.6	15311.6	116.9		
Total	138	17026.9				

S = 10.8112 R-Sq = 10.07% R-Sq(adj) = 5.27%

Table 4. ANOVA Results on Outcome 4.4 with GPA Groups as Independent Variables.

Table 5 shows the means and BL and EXP scores for all GPA groups. From these means, the source of the interaction is fairly clear: Group 2 scores actually went down from the BL to the EXP groups, and Group 3 scores went up.

GPA group	BASELINE	EXPERIMENTAL
1: 3.5-4.0	92.1 (n=37)	94.65 (n=23)
2: 3.0-3.4	92.79 (n=16)	87.63 (n=23)
3: 2.5-2.9	83.08 (n=15)	93.33 (n=15)
4: 2.0-2.4	89.42 (n=8)	88.46 (n=2)
5: < 2.0	85 (n=2)	85 (n=1)

Table 5. Mean Grade vs. GPA Groups on Outcome 4.4 (Baseline vs. Experimental).

Post hoc Tukey procedure tests of the difference of means produced no significant results. The Tukey tests were followed by independent sample t-tests, with no assumption of equal variance. The t-tests did produce a significant difference between the BL and EXP scores of GPA group 3 (t = -2.15; *p*= .044). The number of students in each of these groups was relatively small: 15 in the BL group and 8 in the EXP group. The mean score for 4.4 for the BL group was 83.08 (sd = 24.00), and the mean for the EXP group was 93.27 (sd = 8.66). Table 6 details these results.

```
Two-sample T for 4.4b

BL or
EXPER   N   Mean  StDev  SE Mean
1      15   83.1   14.0      3.6
2       8  93.27   8.66      3.1


Difference = mu (1) - mu (2)
Estimate for difference:  -10.19
95% CI for difference:  (-20.08, -0.31)
T-Test of difference = 0 (vs not =): T-Value = -2.15  P-Value = 0.044  DF = 20
```

Table 6. Two-Sample T-Test Results on Grade vs. GPA Groups on Outcome 4.4 (Baseline vs. Experimental).

The GPA groupings also showed a significant interaction in the same General Linear Model analysis for outcome 5.5 (*p* = .05). Table 7 shows the details of this analysis.

```
Analysis of Variance for HW 5.5, using Adjusted SS for Tests

Source                    DF   Seq SS   Adj SS  Adj MS     F      P
MSU GPA Group              3   2018.1   2041.0   680.3  4.54  0.005
BL or EXP                  1    103.5     25.5    25.5  0.17  0.681
MSU GPA Group*BL or EXP    3   1201.1   1201.1   400.4  2.67  0.051
Error                    119  17829.2  17829.2   149.8
Total                    126  21152.1


S = 12.2403   R-Sq = 15.71%   R-Sq(adj) = 10.75%
```

Table 7. ANOVA Results on Outcome 5.5 with GPA Groups as Independent Variables.

For outcome 5.5, the means for all GPA groups are given in table 8. Again the source of the interaction is fairly clear: GPA Group 2 had a positive gain from BL to EXP, and gpa Group 3 actually went down.

GPA group	BASELINE	EXPERIMENTAL
1: 3.5-4.0	99.02 (n=34)	98.48 (n=22)
2: 3.0-3.4	86.67 (n=15)	97.73 (n=22)
3: 2.5-2.9	92.01 (n=12)	86.22 (n=13)
4: 2.0-2.4	99.7 (n=7)	100 (n=2)
5: < 2.0	49 (n=2)	100 (n=1)

Table 8. Mean Grade vs. GPA Groups on Outcome 5.5 (Baseline vs. Experimental).

As with outcome 4.4, post hoc Tukey procedure tests of the difference of means produced no significant results. Follow-up independent sample t-tests, with no assumption of equal variance, also did not produce significant results. The results for Group 2 were t = -1.64 and p = .122. Table 9 shows these results.

```
Two-sample T for 5.5a

BL or
EXPE    N   Mean  StDev  SE Mean
1      15   86.7   25.4      6.5
2      22  97.73   7.79      1.7


Difference = mu (1) - mu (2)
Estimate for difference:  -11.06
95% CI for difference:  (-25.46, 3.34)
T-Test of difference = 0 (vs not =): T-Value = -1.64  P-Value = 0.122  DF = 15
```

Table 9. Two-Sample T-Test Results on Grade vs. GPA Groups on Outcome 5.5 (Baseline vs. Experimental).

Using the General Linear Model, analyses were also conducted to find out if the intervention affected non-white students differently than white students and non-transfer students differently than transfer students. No significant differences were found. We also analyzed the data by major grouping (electrical engineering, computer engineering, computer science, mechanical engineering, and other) and found no significant differences.

Conclusion

This paper presented the design and evaluation of a portable course for teaching digital logic. Course materials were created that included textbooks and videos that covered a set of detailed learning outcomes for the course. A portable lab kit was designed that allowed hands-on experience with the course material. Analysis was conducted that compared the student performance for those that took the course using traditional benchtop equipment versus those that used the portable lab kit. Not significant differences were found. Two adaptive learning modules were created and tested on two of the more challenging learning outcomes. It was found that the adaptive learning module for outcome 4.4 (combinational logic synthesis) had a significant impact on students with GPA's between 2.5-2.9 on a 4-point scale. No other impact was discovered.

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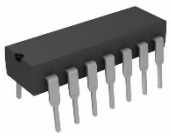
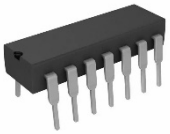
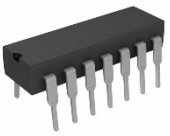
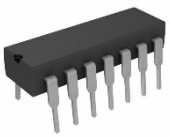
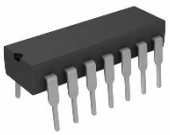
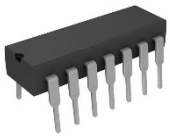
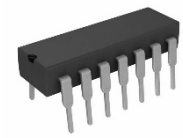
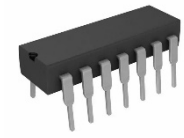
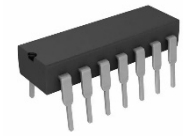
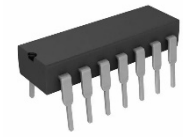
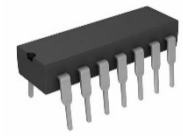
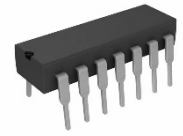
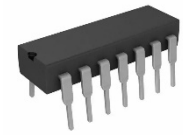
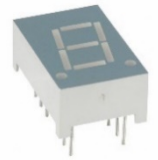
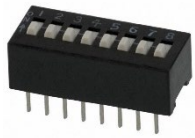
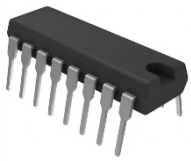
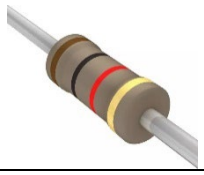
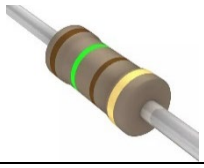
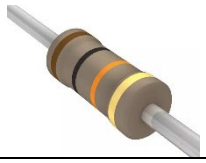
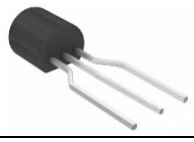
Appendix A. Portable Lab Kit Material List

Qty	Image	Description	Manufacturer (Mfn Part #)	Distributor (Distr. Part #)	Data Sheet
1		Solderless Breadboard	Digilent (340-002)	Digi-Key (1286-1062-ND)	
1		Wiring Kit for Solderless Breadboard	Global Specialties (WK-2)	Digi-Key (BKWK-2-ND)	
2		AND Gates, 2-Input, 4x per part	Texas Instruments (SN74HC08N)	Digi-Key (296-1570-5-ND)	Data Sheet
2		AND Gates, 3-Input, 3x per part	Texas Instruments (SN74HC11N)	Digi-Key (296-8217-5-ND)	Data Sheet
2		AND Gates, 4-Input, 2x per part	Texas Instruments (SN74HC21N)	Digi-Key (296-8266-5-ND)	Data Sheet
2		OR Gates, 2-Input, 4x per part	Texas Instruments (SN74HC32N)	Digi-Key (296-1589-5-ND)	Data Sheet
2		OR Gates, 3-Input, 3x per part	Texas Instruments (CD74HC4075E)	Digi-Key (296-33088-5-ND)	Data Sheet
2		Inverters, 6x per part	Texas Instruments (SN74HC04N)	Digi-Key (296-1566-5-ND)	Data Sheet

2		NAND Gates, 2-Input, 4x per part	Texas Instruments (SN74HC00N)	Digi-Key (296-1563-5-ND)	Data Sheet
2		NAND Gates, 3-Input, 3x per part	Texas Instruments (SN74HC10N)	Digi-Key (296-8214-5-ND)	Data Sheet
2		NAND Gates, 4-Input, 2x per part	Texas Instruments (SN74HC20N)	Digi-Key (296-12892-5-ND)	Data Sheet
2		NOR Gates, 2-Input, 4x per part	Texas Instruments (SN74HC02)	Digi-Key (296-1564-5-ND)	Data Sheet
2		NOR Gates, 3-Input, 3x per part	Texas Instruments (SN74HC27)	Digi-Key (296-12896-5-ND)	Data Sheet
2		NOR Gates, 4-Input, 2x per part	Texas Instruments (CD74HC4002)	Digi-Key (296-25987-5-ND)	Data Sheet
2		D-flip-flops, 2x per part	Texas Instruments (SN74HC74N)	Digi-Key (296-1602-5-ND)	Data Sheet
10		LED, Red, Discrete	Kingbright (WP710A10LSRD)	Digi-Key (754-1590-ND)	Data Sheet
1		LED, 7-Segment Display	Lumex Opto/Components Inc. (LDS-C416RI)	Digi-Key (67-1446-ND)	Data Sheet

1		Buzzer, Magnetic, DC, Single Tone	CUI Inc. (CEM-1205C)	Digi-Key (102-1124-ND)	Data Sheet
1		Switch, slider, SPST, 8-position	CTS Electrocomponents (208-8)	Digi-Key (CT2088-ND)	Data Sheet
1		Switch, push-button, SPDT	C&K (KS12R22CQD)	Digi-Key (CKN1595-ND)	Data Sheet
1		Resistor Network, 8x, DIP, 330 Ohm, Isolated	Bourns Inc (4116R-1-331LF)	Digi-Key (4116R-1-331LF-ND)	Data Sheet
1		Resistor Network, 9x, SIP, 10k Ohm, Bussed	Bourns Inc (4610X-101-103LF)	Digi-Key (4610X-1-103LF-ND)	Data Sheet
2		Resistor, Axial, 1k Ohm, 1/4 W, 5%	Yageo (CFR-25JB-52-1K)	Digi-Key (1.0KQBK-ND)	Data Sheet
12		Resistor, Axial, 150 Ohm, 1/4 W, 5%	Yageo (CFR-25JB-52-150R)	Digi-Key (150QBK-ND)	Data Sheet
2		Resistor, Axial, 10k Ohm, 1/4 W, 5%	Yageo (CFR-25JB-52-10K)	Digi-Key (10KQBK-ND)	Data Sheet
1		NPN Transistor, 2N3904, 200 mA	ON Semiconductor (2N3904TFR)	Digi-Key (2N3904D26ZCT-ND)	Data Sheet

1		Diode, 1N4002, 1A	ON Semiconductor (1N4002)	Digi-Key (1N4002FSCT-ND)	Data Sheet
1		Jumper Wires, Female-to-Female, 10-Pack	MikroElektronika (MIKROE-511)	Digi-Key (1471-1230-ND)	
1		Pin Header, 0.1", Single-Strip, 10-pos	3M (929834-02-10-RK)	Digi-Key (929834E-02-10-ND)	Data Sheet
1		DE0-CV, Cyclone V, FPGA Board	Terasic (P0192)	Digi-Key (P0192-ND) or Terasic (P0192)	User Manual
1		Analog Discovery 2 - Portable Oscilloscope/Logic Analyzer/Power Supply	Digilent (410-321)	Digi-Key (1286-1117-ND) or Digilent (410-321)	Reference Manual