Design & Evaluation of a Multipurpose Course Structure for Teaching Digital Logic

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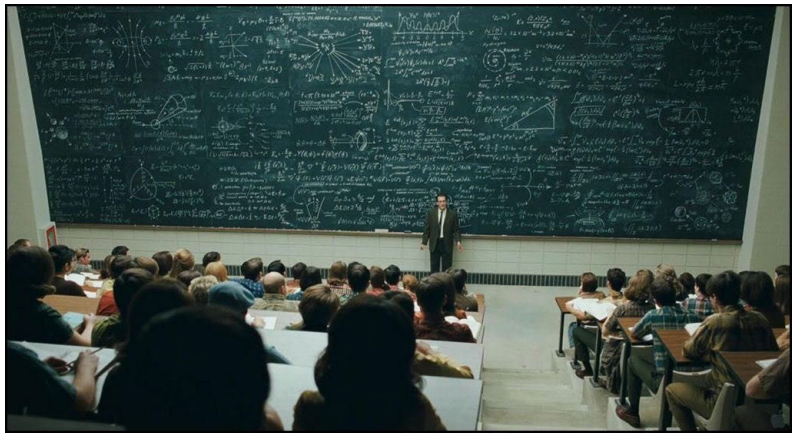
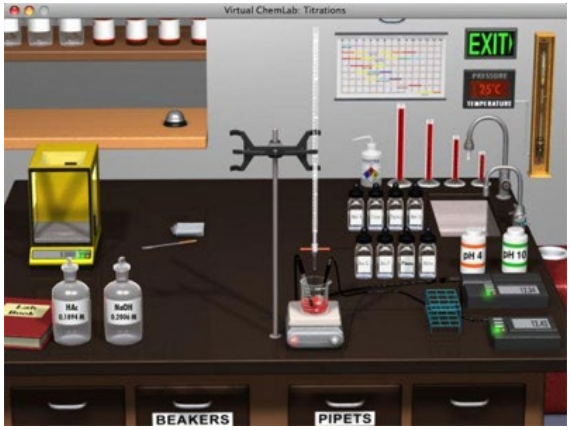
Students Increasingly Want a Breadth of Course Materials

- Videos, online simulations, online formative assessment
- It is becoming more and more difficult to effectively educate engineering students by writing on a white board.





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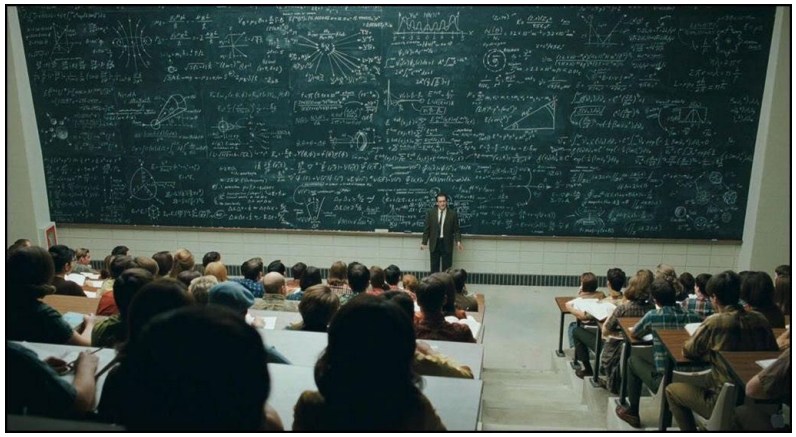
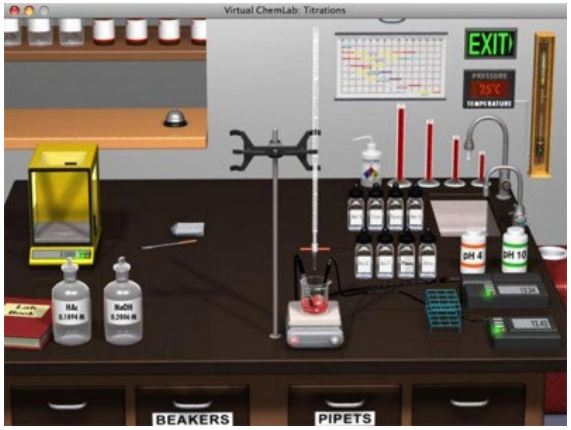


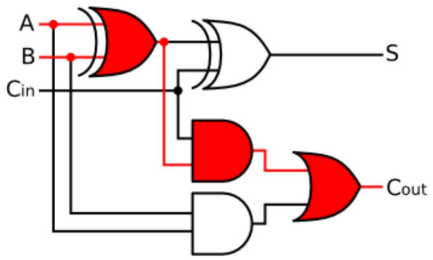


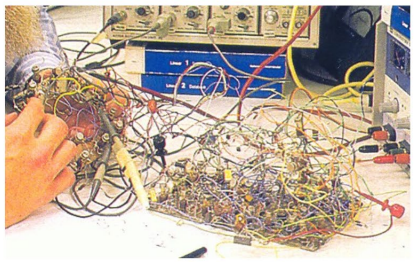
Supplementary e-Learning Materials Give Options

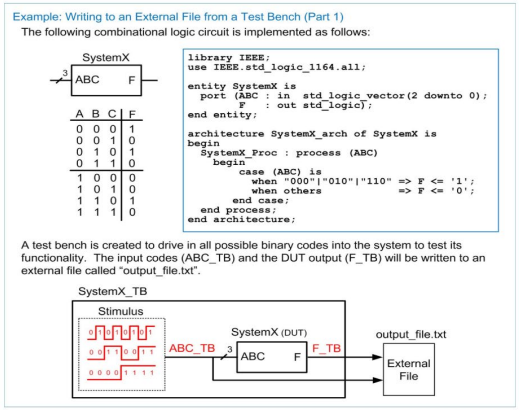
- Fully Online Course Delivery
- Flipped Course for Active Learning
- Supplementary Multi-Mode Course Materials to Support Students

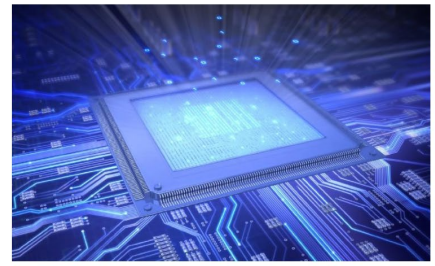
This Project Looks at a Digital Logic Circuits Course

- Traditional digital circuits (AND/OR gates, Finite State Machines, VHDL/Verilog)
- Present in every EE/CpE Program
- No Calculus pre-req (i.e., large class sizes, wide ranging capabilities of students)









The Research Questions

- R1: Can a fully online version of this course(s) achieve the same level of student learning as a traditional live-taught version?

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- R2: Can the laboratory component be effectively administered using a portable lab kit? (i.e., cost, logistics, student support).

- R3: Can adaptive e-learning modules aid student learning on more complex topics without instructor interaction?

If the online version can be as effective, it enables:

Remote Delivery May Improve Access

Personalized Learning

Increased Efficiency

When comparing two delivery modes, it starts with assessment

- The existing live-taught logic course(s) were assessed in the historical manner
  - *Hand worked homework problems out of the textbook (sometimes the same questions, sometimes different each semester)*
  - *Exams with questions made-up each semester by the instructor.*
  - *Lab exercises with a combination of demo-points and sometimes design journal grading (no rubric, just best guess grading by the TA).*

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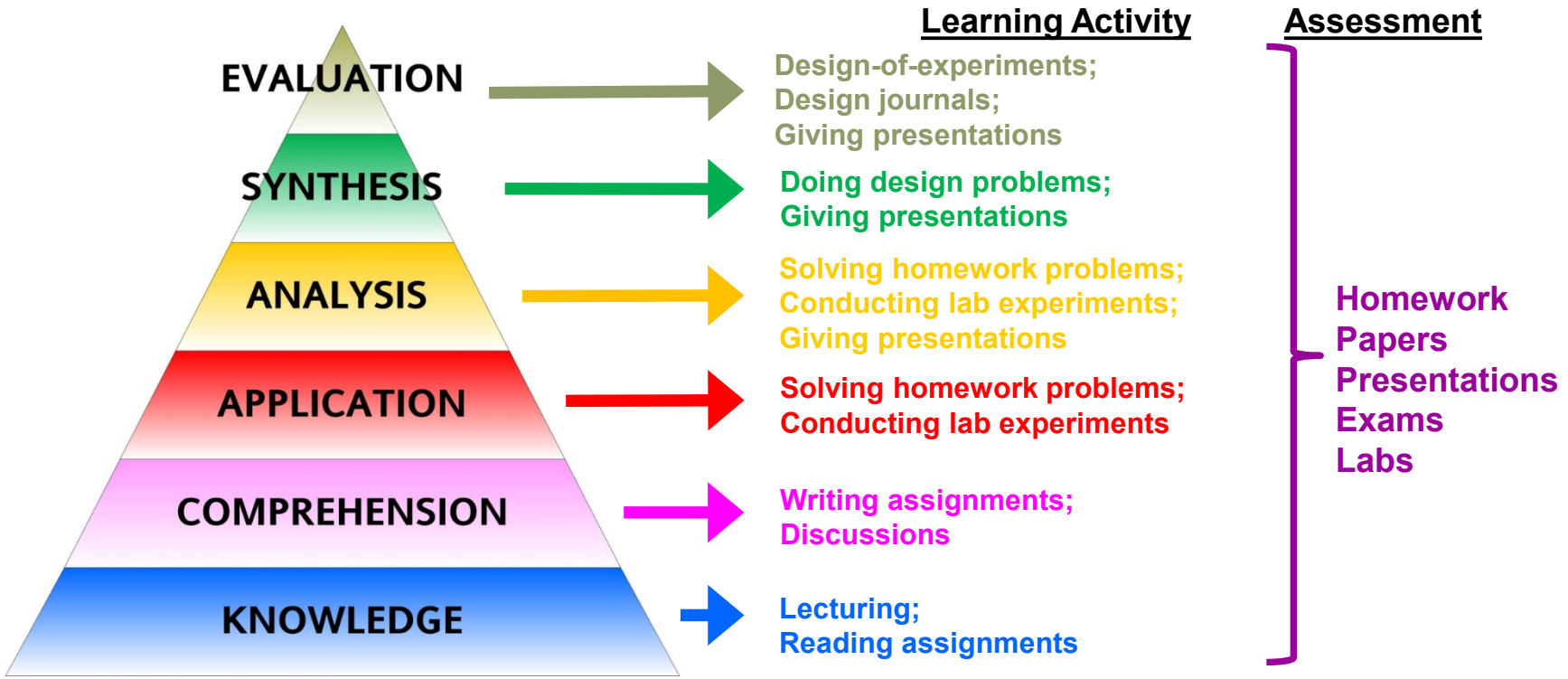
- Assessment tools were created that could be used in both live and online modes.
  - *Not that big of a deal with learning management systems capability.*
  - *Multiple-choice quizzes & simulation waveforms…*

First, the learning outcomes needed to be specified

It also is necessary to think about the learning level to inform the type of assessment used



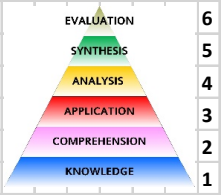
Learning Objectives

- General statement about type of content that will be learned.
- A book chapter is an example.
- When adding multi-mode material, it becomes a module.

Module Topic	Learning Objective
Module 1: Analog vs. Digital	To understand the basic principles of analog and digital systems.
Module 2: Number Systems	To understand the basic principles of binary number systems.
Module 3: Digital Circuits & Interfacing	To understand the basic electrical operation of digital circuits.
Module 4: Combinational Logic	To understand the basic principles of combinational logic design.
Module 5: VHDL (part 1)	To understand the basic principles of hardware description languages.
Module 6: MSI Logic	To understand the basic principles of medium scale integrated circuit logic.
Module 7: Sequential Logic	To understand the basic operation of sequential logic circuits.
Module 8: VHDL (part 2)	To understand the full capability of hardware description languages.
Module 9: Behavioral Modeling	To understand how hardware description languages can be used to create behavioral models of synchronous digital systems.
Module 10: Semiconductor Memory	To understand the basic principles of semiconductor-based memory
Module 11: Programmable Logic	To understand the basic principles of programmable logic devices.
Module 12: Arithmetic Circuits	To understand the basic principles of binary arithmetic circuits.
Module 13: Computer Systems	To understand the basic principles of a computer system.

Then Outcomes are Stated, with the Level of Learning

- Something specific that the student can do after completing the section.
- Needs to be measurable.



Learning Objective	Learning Outcome	Learning Category					
The overall learning goal of this module is to:	*After completing this lab, a student will be able to:*	1	2	3	4	5	6
Module 1: To understand the basic principles of analog and digital systems.	**L1.1(a):** Breadboard a simple LED-Resistor circuit.					x	
	L1.1(b): Use an AWG to output a signal with a specified type, amplitude, offset, and frequency.					x	
	L1.1(c): Use an oscilloscope to display a waveform on the screen.				x		
	L1.1(d): Describe the on/off behavior of a digital signal.		x				
	L1.1(e): Describe the impact that increasing the frequency has on a digital signal.		x				
Module 2: To understand the basic principles of binary number systems.	**2.1:** Describe the formation and use of positional number systems.		x				
	2.2: Convert numbers between different bases.			x			
	2.3: Perform binary addition and subtraction by hand.			x			
	2.4: Use two's complement numbers to represent negative numbers.			x			
Module 3: To understand the basic electrical operation of digital circuits.	**3.1:** Describe the functional operation of a basic logic gate using truth tables, logic expressions, and logic waveforms.	x					
	3.2: Analyze the DC and AC behavior of a digital circuit to verify it is operating within specification.				x		
	3.3: Describe the meaning of a logic family and the operation of the most common technologies used today.	x					
	3.4: Determine the operating conditions of a logic circuit when driving various types of loads.				x		

Outcomes cont…

Module 4: To understand the basic principles of combinational logic design.	**4.1:** Describe the fundamental principles and theorems of Boolean algebra and how to use them to manipulate logic expressions.		x				
	4.2: Analyze a combinational logic circuit to determine its logic expression, truth table, and timing information.				x		
	4.3: Synthesis a logic circuit in canonical form (Sum of Products or Product of Sums) from a functional description including a truth table, minterm list, or maxterm list.					x	
	4.4: Synthesize a logic circuit in minimized form (Sum of Products or Product of Sums) through algebraic manipulation or with a Karnaugh map.					x	
	4.5: Describe the causes of timing hazards in digital logic circuits and the approaches to mitigate them.		x				
Module 5: To understand the basic principles of hardware description languages.	**5.1:** Describe the role of hardware description languages in modern digital design.		x				
	5.2: Describe the fundamentals of design abstraction in modern digital design.		x				
	5.3: Describe the modern digital design flow based on hardware description languages.		x				
	5.4: Describe the fundamental constructs of VHDL.		x				
	5.5: Design a VHDL model for a combinational logic circuit using concurrent modeling techniques (signal assignments and logical operators, conditional signal assignments, and selected signal assignments).					x	
	5.6: Design a VHDL model for a combinational logic circuit using a structural design approach.					x	
	5.7: Describe the role of a VHDL test bench.		x				
Module 6: To understand the basic principles of medium scale integrated circuit logic.	**6.1:** Design a decoder circuit using both the classical digital design approach and the modern HDL-based approach.					x	
	6.2: Design an encoder circuit using both the classical digital design approach and the modern HDL-based approach.					x	
	6.3: Design a multiplexer circuit using both the classical digital design approach and the modern HDL-based approach.					x	
	6.4: Design a demultiplexer circuit using both the classical digital design approach and the modern HDL-based approach.					x	

Outcomes cont…

Module 7: To understand the basic operation of sequential logic circuits.	**7.1:** Describe the operation of a sequential logic storage device.		x				
	7.2: Describe sequential logic timing considerations.		x				
	7.3: Design a variety of common circuits based on sequential storage devices (toggle flops, ripple counters, switch debouncers, and shift registers).					x	
	7.4: Design a finite state machine using the classical digital design approach.					x	
	7.5: Design a counter using the classical digital design approach and using an HDL-based, structural approach.					x	
	7.6: Describe the finite state machine reset condition.		x				
	7.7: Analyze a finite state machine to determine its functional operation and maximum clock frequency.				x		
Module 8: To understand the full capability of hardware description languages.	**8.1:** Describe the behavior of a VHDL process and how it is used to model sequential logic circuits.		x				
	8.2: Model combinational logic circuits using a process and conditional programming constructs.					x	
	8.3: Describe how and why signal attributes are used in VHDL models.		x				
	8.4: Design a finite state machine using the classical digital design approach.					x	
	8.5: Describe the capabilities provided by the most common VHDL packages.		x				
Module 9: To understand how hardware description languages can be used to create behavioral models of synchronous digital systems.	**9.1:** Design a VHDL behavioral model for a sequential logic storage device.					x	
	9.2: Describe the process for creating a VHDL behavioral model for a finite state machine.		x				
	9.3: Design a VHDL behavioral model for a finite state machine.					x	
	9.4: Design a VHDL behavioral model for a counter.					x	
	9.5: Design a VHDL register transfer level (RTL) model of a synchronous digital system.					x	
Module 10: To understand the basic principles of semiconductor-based memory systems.	**10.1:** Describe the basic architecture and terminology for semiconductor-based memory systems.		x				
	10.2: Describe the basic architecture of non-volatile memory systems.		x				
	10.3: Describe the basic architecture of volatile memory systems.		x				
	10.4: Design a VHDL behavioral model of a memory system.					x	

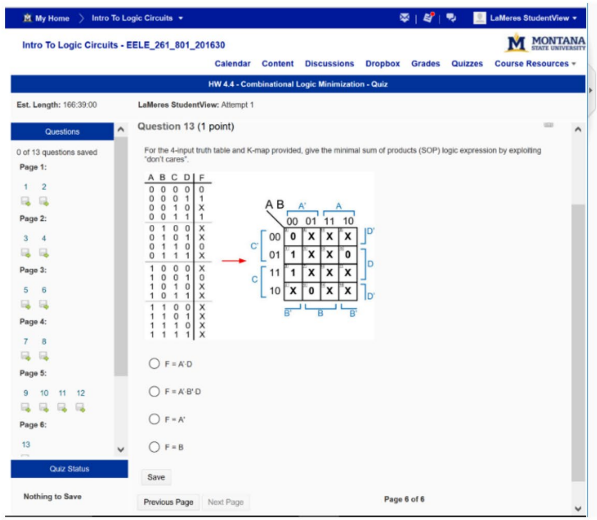
Outcomes cont…

Module 11: To understand the basic principles of programmable logic devices.	**11.1:** Describe the basic architecture and evolution of programmable logic devices.		x				
	11.2: Describe the basic architecture of Field Programmable Gate Arrays (FPGAs).		x				
Module 12: To understand the basic principles of binary arithmetic circuits.	**12.1:** Design a binary adder using both the classical digital design approach and the modern HDL-based approach.					x	
	12.2: Design a binary subtractor using both the classical digital design approach and the modern HDL-based approach.					x	
	12.3: Design a binary multiplier using both the classical digital design approach and the modern HDL-based approach.					x	
	12.4: Design a binary divider using both the classical digital design approach and the modern HDL-based approach.					x	
Module 13: To understand the basic principles of a computer system.	**13.1:** Describe the basic components and operation of computer hardware.		x				
	13.2: Describe the basic components and operation of computer software.		x				

- 58 Learning Outcomes Defined

Over 1000 assessment tools were developed

- i.e., homework/quiz/exam problems + lab exercises.
- MC format + VHDL design/simulations + concept checks
- Focused on assessing at the same level of learning.
- Focused on developing numerous questions per outcome, grouped into levels of difficulty. (difficulty ≠ level of learning)



Concept Check

CC7.5 What characteristic of a counter makes it a special case of a finite state machine?

A) The state transitions are mostly linear, which reduces the implementation complexity.

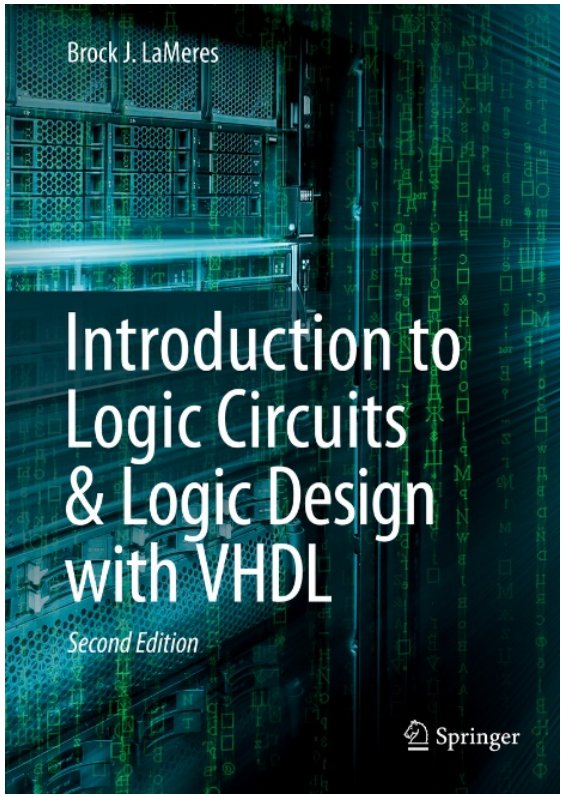
B) The outputs are always a gray code.

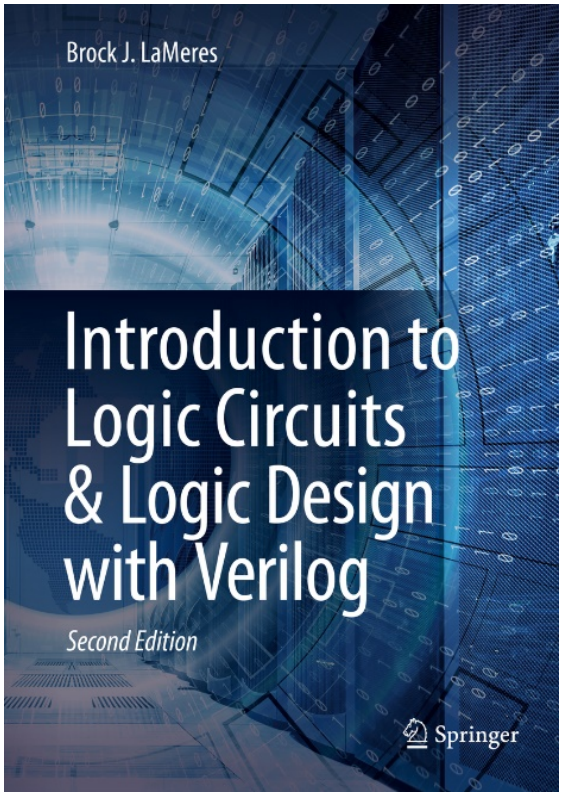
C) The next state logic circuitry is typically just sum terms.

D) There is never a situation where a counter could be a Mealy machine.

Two New Textbooks Authored

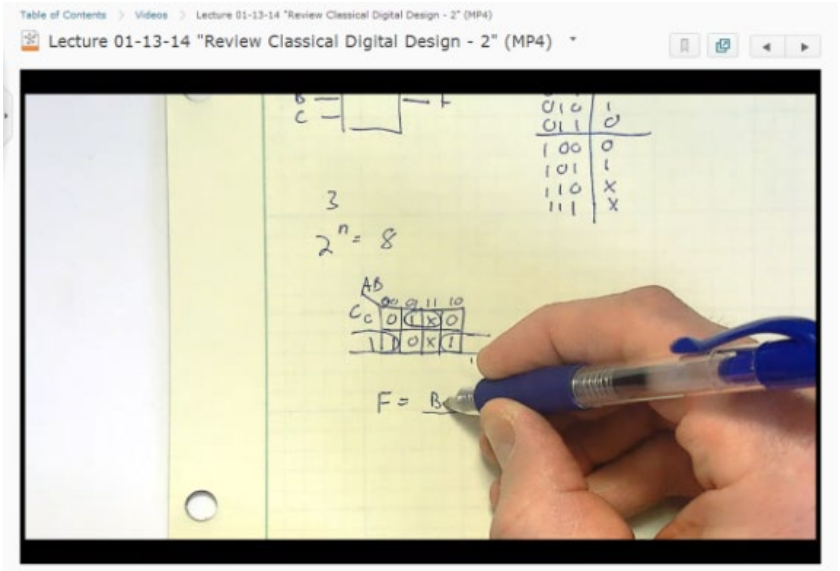
- to support both HDL languages (VHDL & Verilog)
- designed to teach the students how to achieve the learning outcomes.

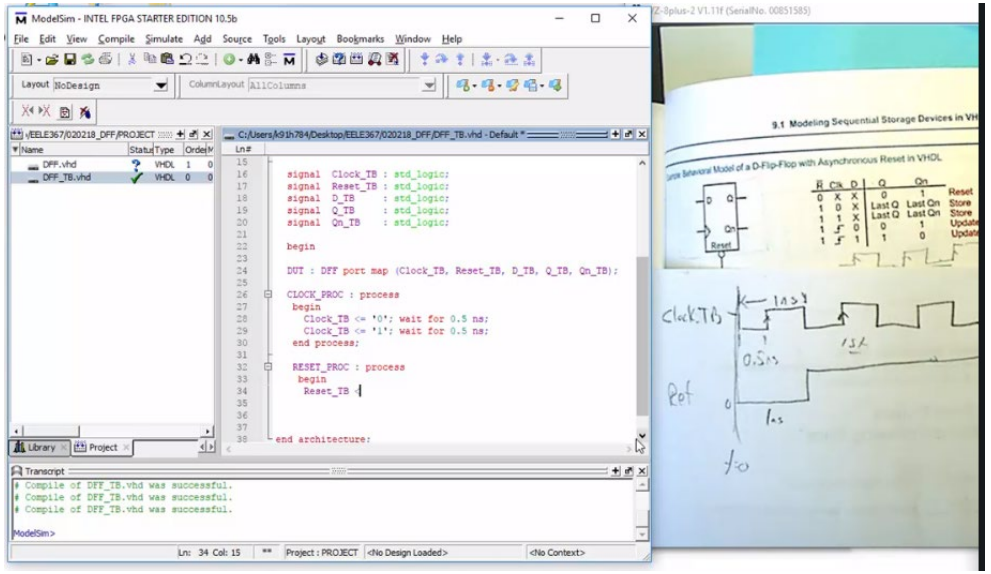




149 mini-lecture YouTube videos created

- 5-15 minutes each, outcome specific



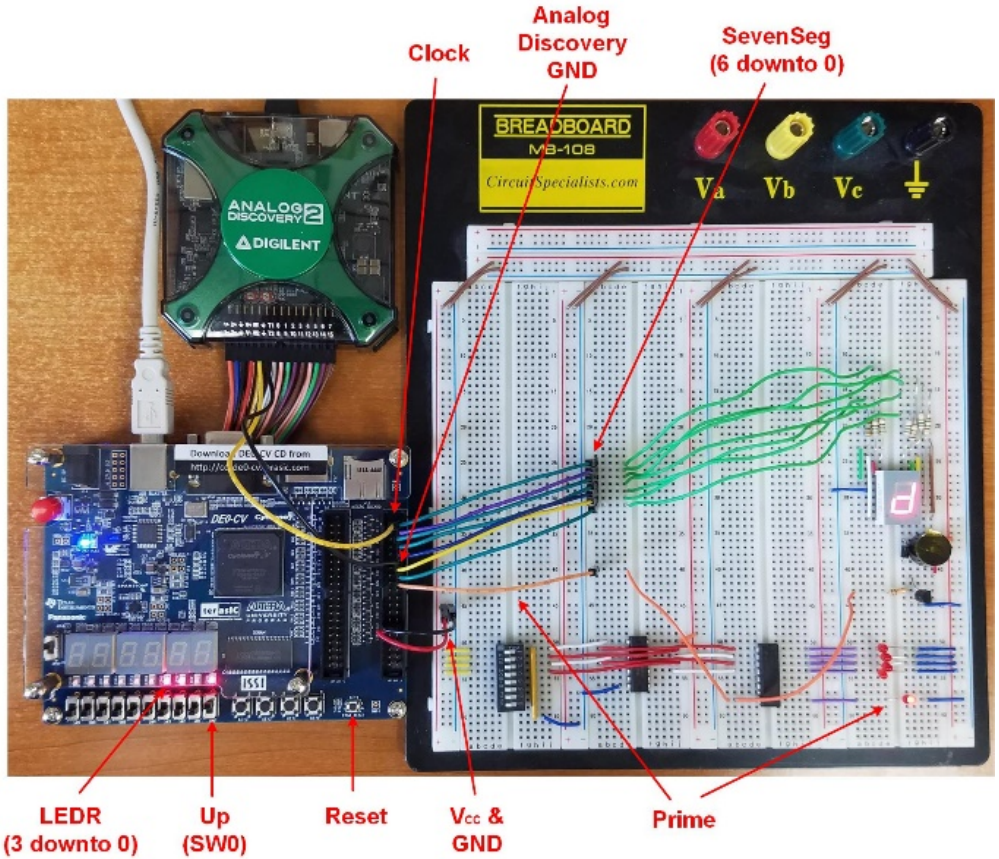


A Portable Lab Kit was Assembled

- This kit can be used in the live-taught lab in a traditional lab bench setting.
- It can also be used completely remotely using a laptop and USB power

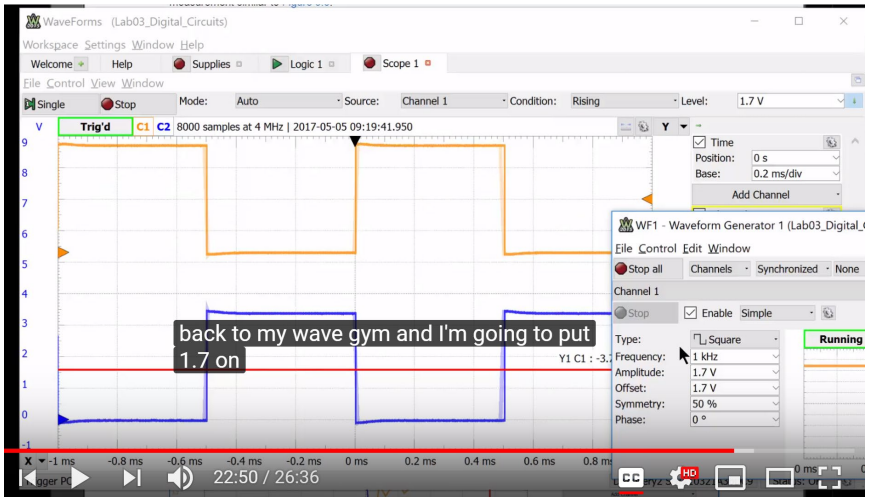
Key Features

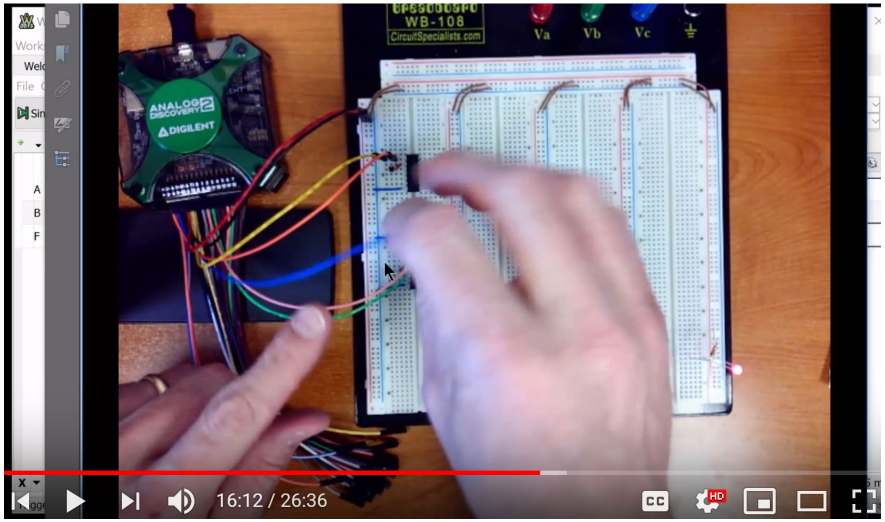
- Analog Discovery 2 ($180)
  - power supply
  - waveform generator
  - oscilloscope
  - logic analyzer
- DE0-CV FPGA Board ($100)
- Discrete Logic Parts ($20)
- Large Breadboard ($20)
- Total Cost = $320
- Live: 12 stations/room
- Remove: Student check-out



27 lab tutorial YouTube videos created

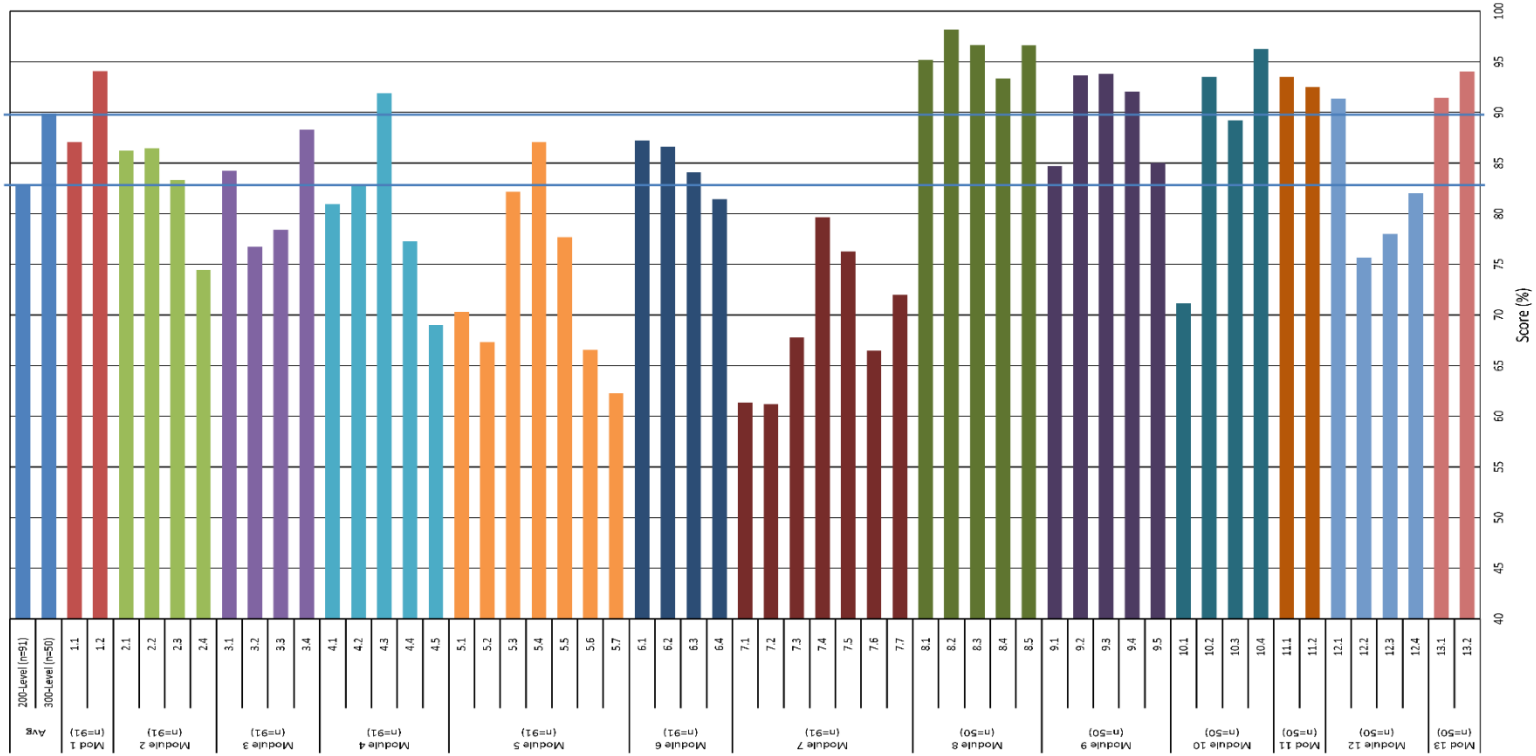
- introducing the lab assignment, walking through some basic steps.



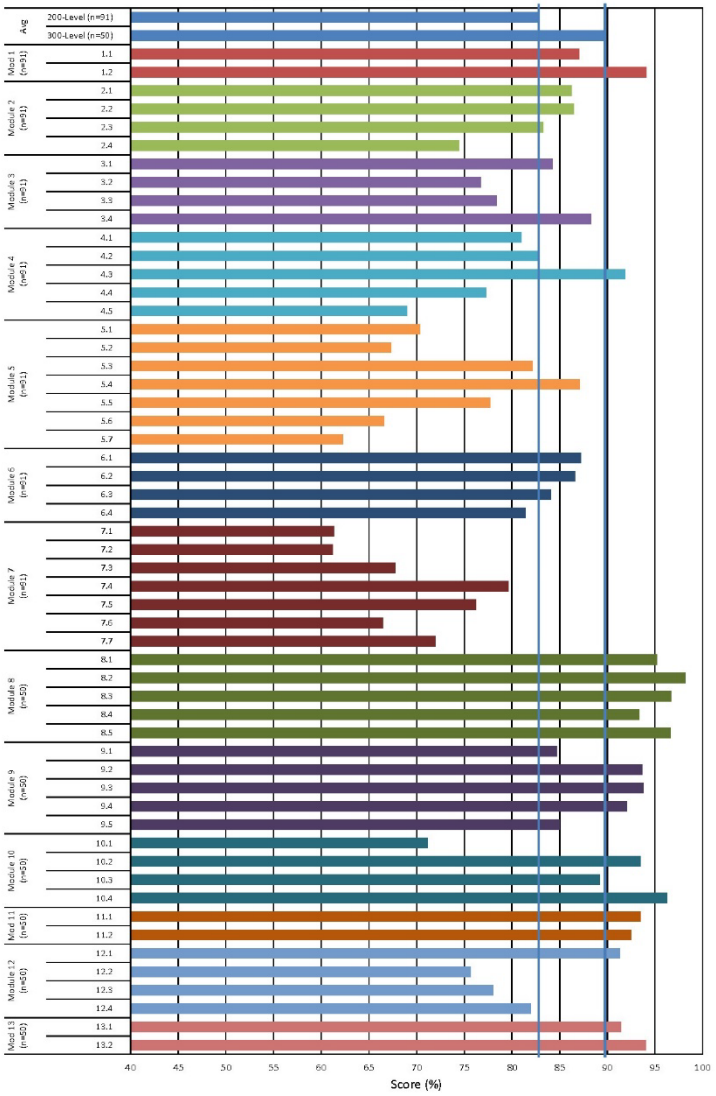


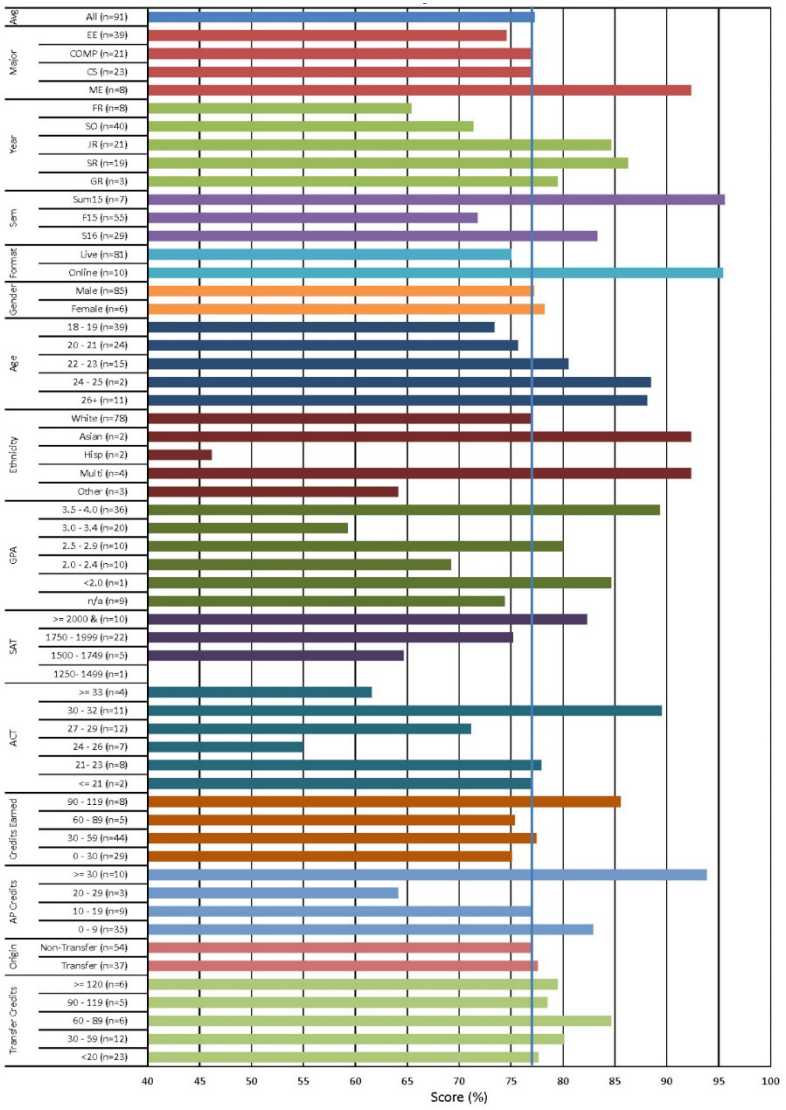
Data was collected for 2 years across a variety of delivery modes

- Live taught Lecture + Traditional Bench Top Equipment (2 semesters).
- Live taught lecture + portable lab kit (1 semester).
- Video lecture + portable lab kit (1 semester).
- Student demographics were collected (consent forms signed)

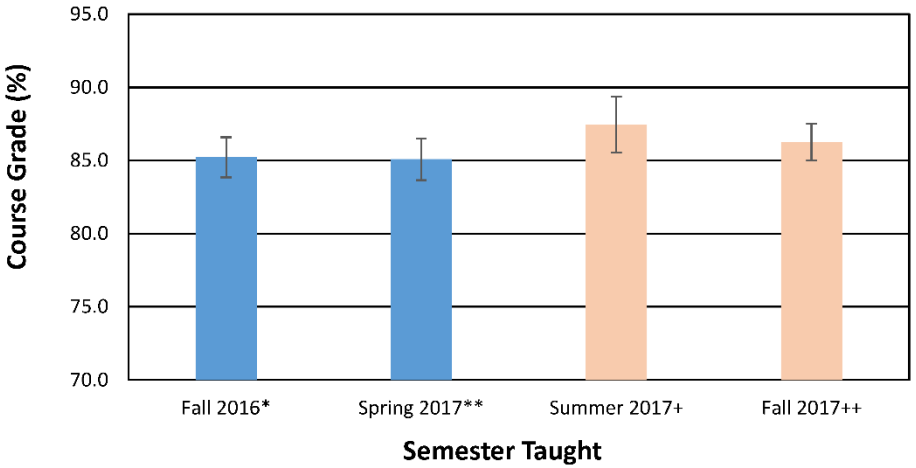


Data Analysis – Outcome vs. Demo

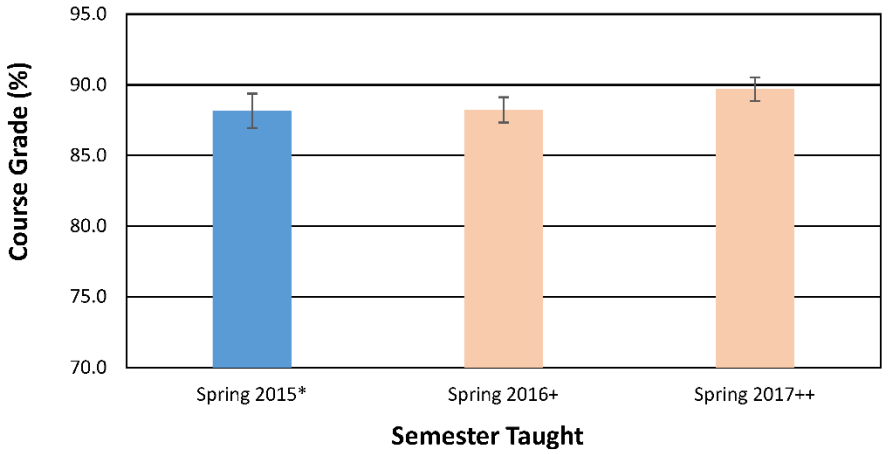




Student Performance Didn't Show Significant Variation Between Delivery Modes (lecture or lab)



Note 1: Error bars are +/- 1x Standard Error
* Live Lecture / Benchtop Lab Equipment (N=91, M=85.2, SD=13.1)
** Live Lecture / Benchtop Lab Equipment (N=54, M=85.1, SD=10.5)
+ Online Lecture / Portable Lab Kit (N=25, M=87.5, SD=9.6)
++ Live Lecture / Portable Lab Kit (N=84, M=86.3, SD=11.6)

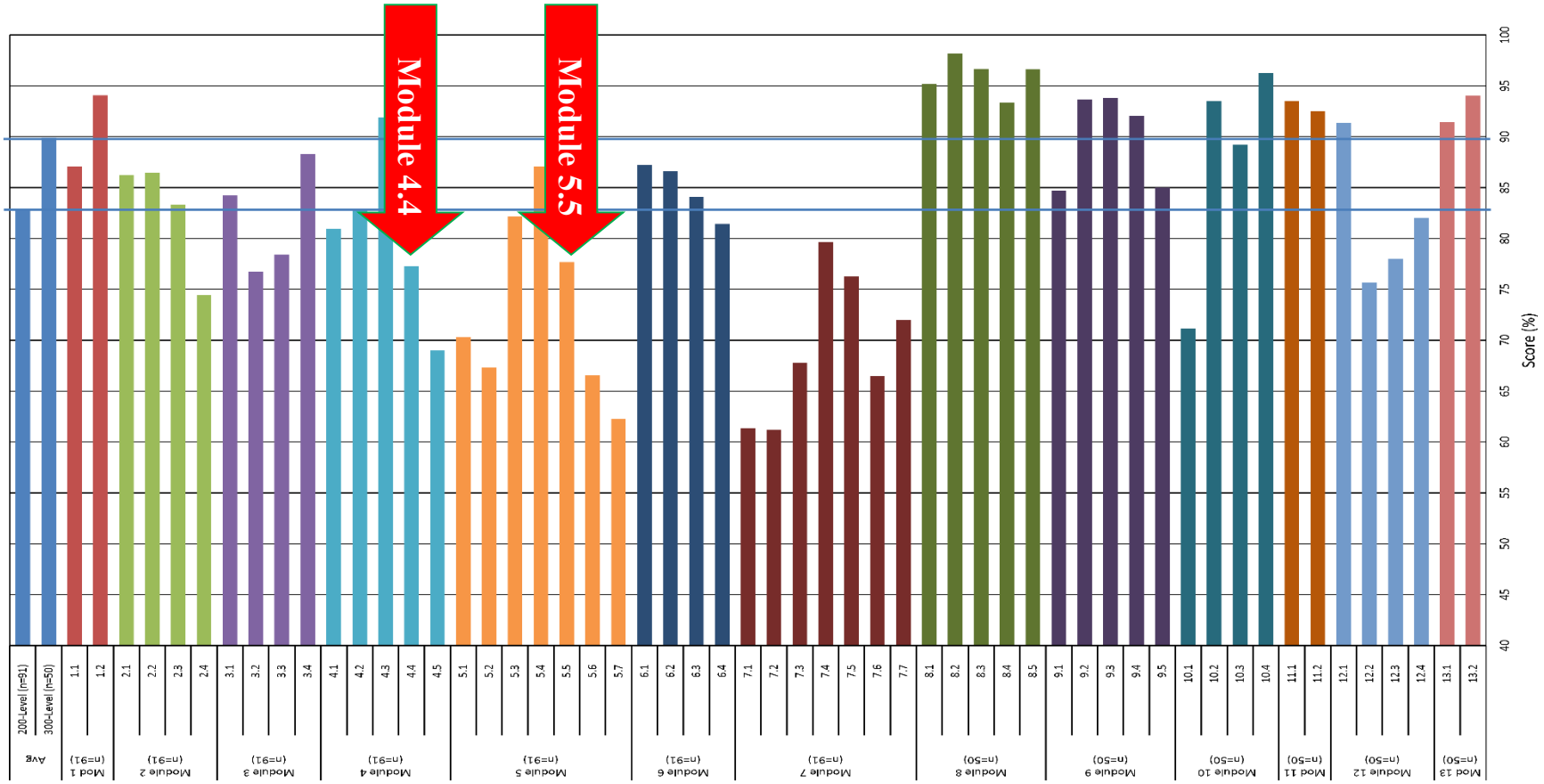


Note 1: Error bars are +/- 1x Standard Error
* Live Lecture / Benchtop Lab Equipment (N=48, M=88.2, SD=8.4)
+ Live Lecture / Portable Lab Kit (N=50, M=88.1, SD=6.3)
++ Live Lecture / Portable Lab Kit (N=57, M=89.7, SD=6.4)

- Note: These plots show class average. But all outcomes were individually examined.

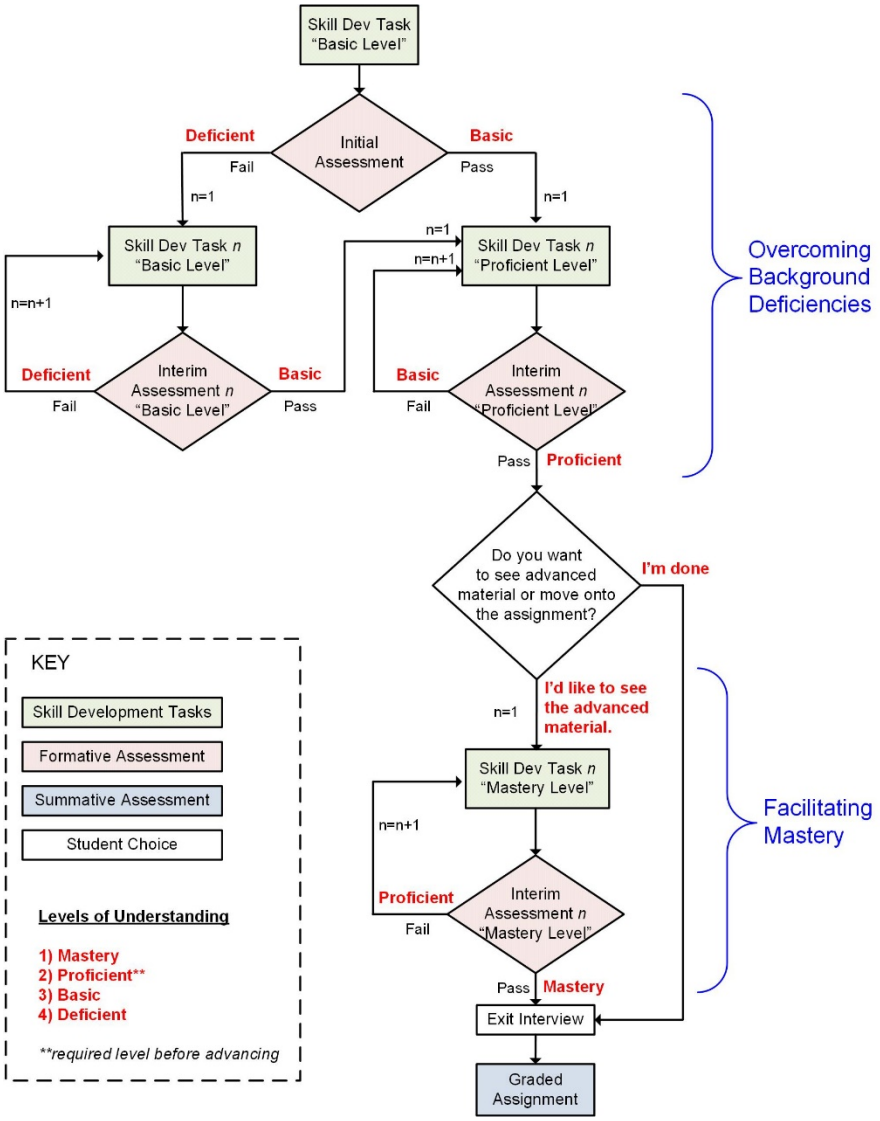
Now that R1 and R2 Have Supporting Data, Let's Take Advantage of the e-Learning Capability

- Step 1: Identify the Most Challenging Outcomes

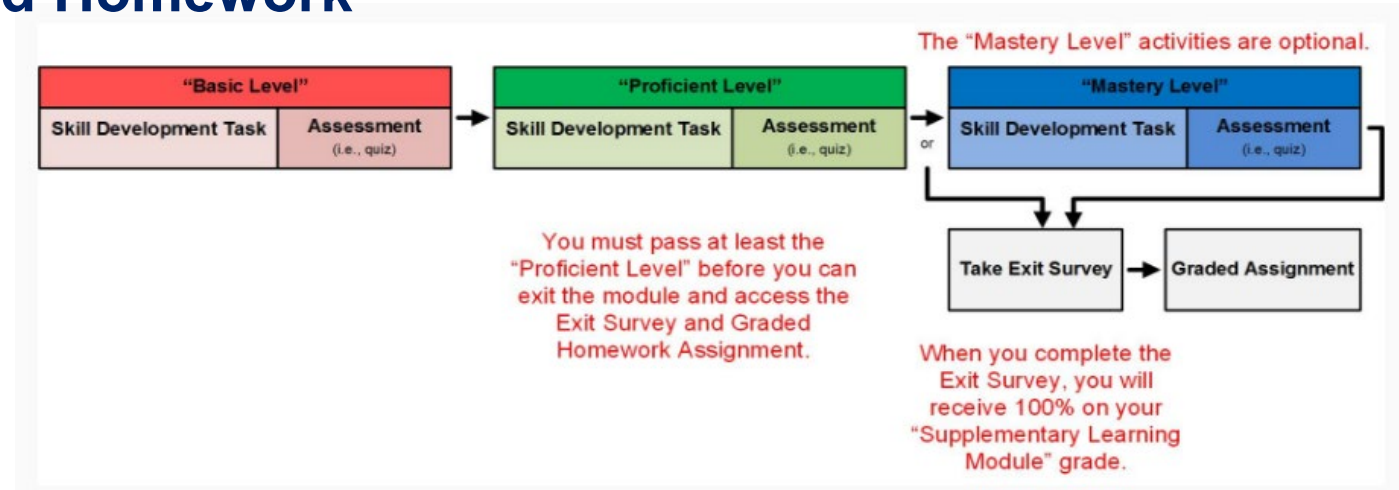


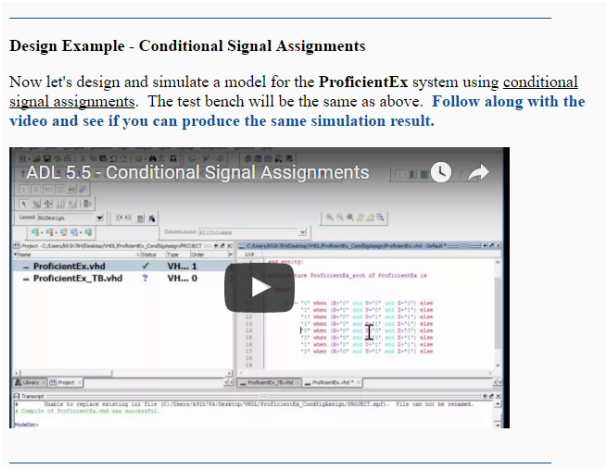
Supplementary Materials were Created for Module 4.4 and 5.5.

- 4.4 Combinational Logic Synthesis
- 5.5 Concurrent Modeling in VHDL



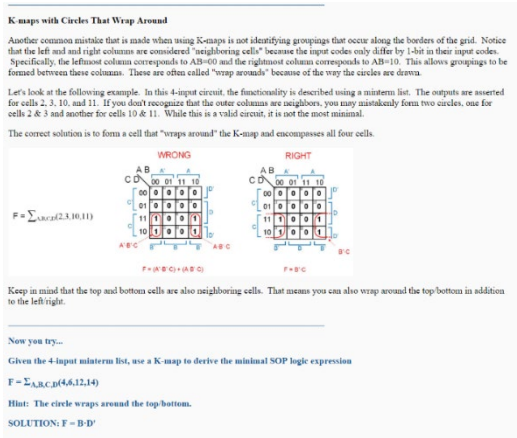
In Initial Offering, Student Had to Pass at Proficient to Access Graded Homework





Design Example - Conditional Signal Assignments

Now let's design and simulate a model for the **ProficientEx** system using conditional signal assignments. The test bench will be the same as above. **Follow along with the video and see if you can produce the same simulation result.**



K-maps with Circles That Wrap Around

Another common mistake that is made when using K-maps is not identifying groupings that occur along the borders of the grid. Notice that the left and and right columns are considered "neighboring cells" because the input codes only differ by 1-bit in their input codes. Specifically, the leftmost column corresponds to AB=00 and the rightmost column corresponds to AB=10. This allows groupings to be formed between these columns. These are often called "wrap arounds" because of the way the circles are drawn.

Let's look at the following example. In this 4-input circuit, the functionality is described using a minterm list. The outputs are asserted for cells 2, 3, 10, and 11. If you don't recognize that the outer columns are neighbors, you may mistakenly form two circles, one for cells 2 & 3 and another for cells 10 & 11. While this is a valid circuit, it is not the most minimal.

The correct solution is to form a cell that "wraps around" the K-map and encompasses all four cells.

Keep in mind that the top and bottom cells are also neighboring cells. That means you can also wrap around the top/bottom in addition to the left/right.

Now you try...

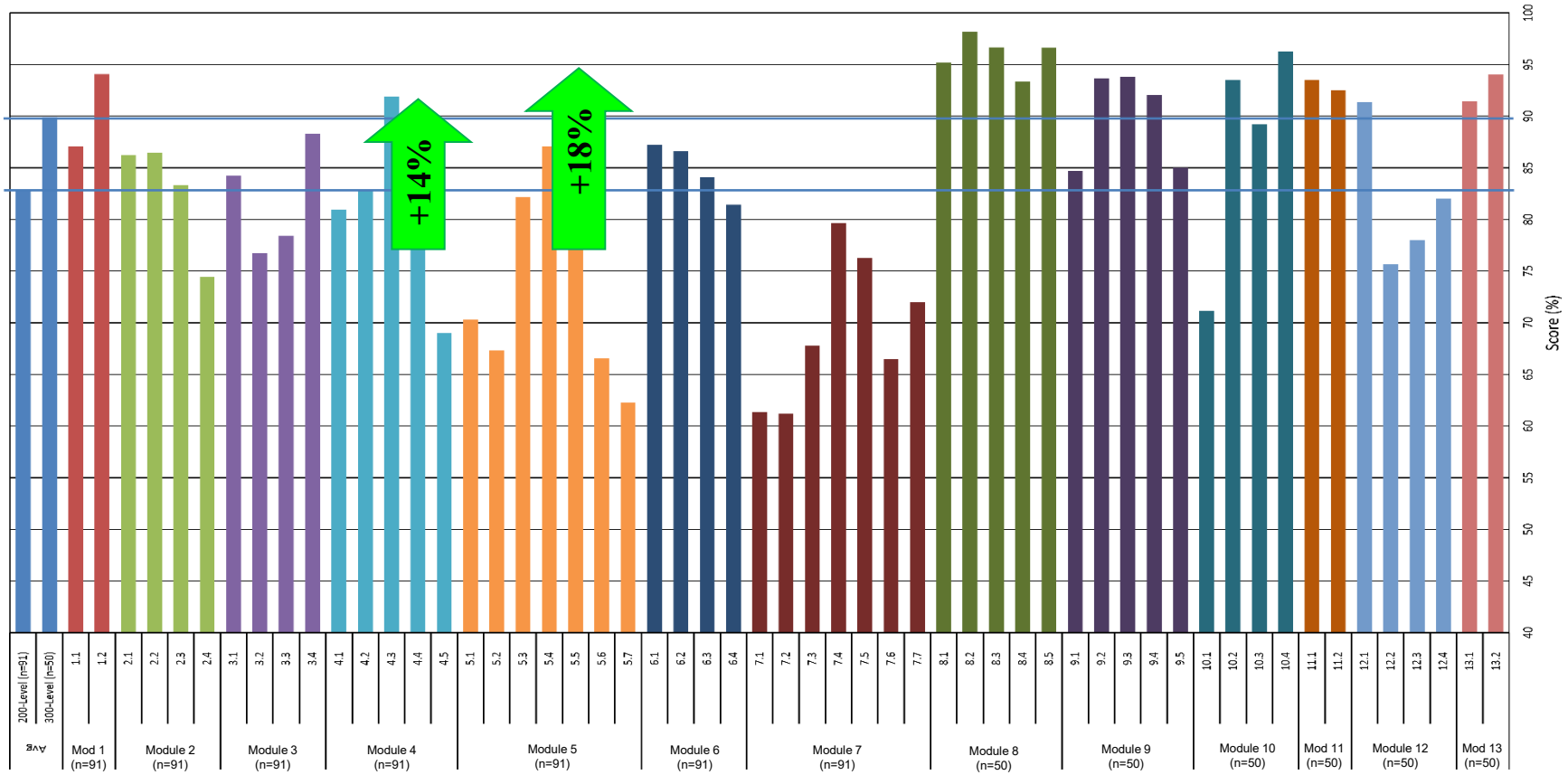
Given the 4-input minterm list, use a K-map to derive the minimal SOP logic expression

$F = \Sigma_{A,B,C,D}(4,6,12,14)$

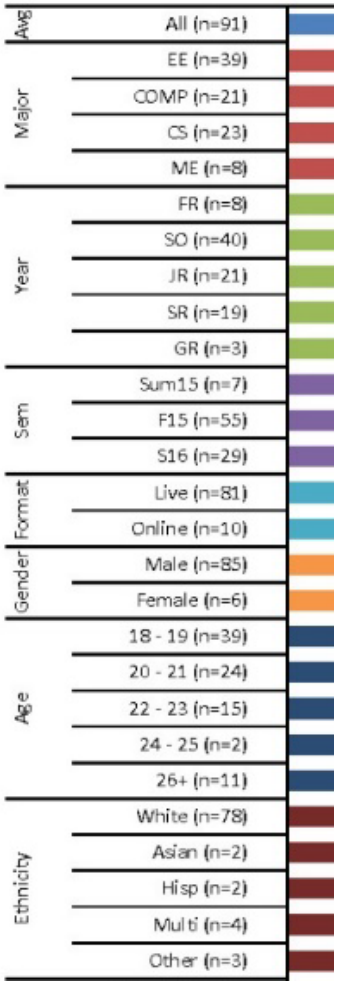
Hint: The circle wraps around the top/bottom.

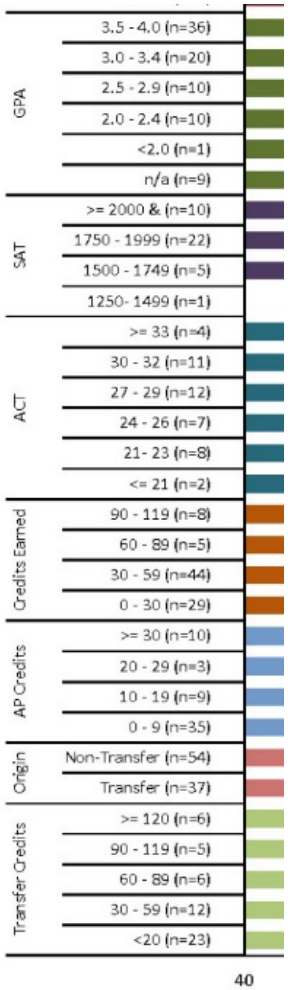
SOLUTION: $F = B \cdot D'$

The cohort that received the adaptive learning experience showed improved performance on outcome 4.4 and 5.5



The Data was Analyzed for Impact in Independent Variables





40

The only significant difference was seen on students with GPAs between 2.5-2.9 & 3.0-3.4.

GPA group	BASELINE	EXPERIMENTAL	
1: 3.5-4.0	92.1 (n=37)	94.65 (n=23)	
2: 3.0-3.4	92.79 (n=16)	87.63 (n=23)	
3: 2.5-2.9	83.08 (n=15)	93.33 (n=15)	**p=0.044**
4: 2.0-2.4	89.42 (n=8)	88.46 (n=2)	
5: < 2.0	85 (n=2)	85 (n=1)	

Table 5. Mean Grade vs. GPA Groups on Outcome 4.4 (Baseline vs. Experimental).

GPA group	BASELINE	EXPERIMENTAL	
1: 3.5-4.0	99.02 (n=34)	98.48 (n=22)	
2: 3.0-3.4	86.67 (n=15)	97.73 (n=22)	**p=0.01**
3: 2.5-2.9	92.01 (n=12)	86.22 (n=13)	
4: 2.0-2.4	99.7 (n=7)	100 (n=2)	
5: < 2.0	49 (n=2)	100 (n=1)	

Table 8. Mean Grade vs. GPA Groups on Outcome 5.5 (Baseline vs. Experimental).

Adaptive Learning Did Seem to Help Students with Lower GPAs.

- Data analysis showed that the grading ceiling effect may impact results.

R3 Conclusion

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A Focus Group was Held to Collect Qualitative Feedback (n=6).

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- Students thought the adaptive learning modules were useful.
- Students thought that they should exist for the more difficult outcomes.
- Students agreed they weren't needed on every outcome.
- Students did not like that they were mandatory.
  - *Students with high GPAs didn't like the extra work when it wasn't needed.*

Conclusion

The Digital Logic Course Materials Was Effective Across Multiple Delivery Modes

- Supports live, remote, or hydrid delivery.
- Portable lab kit enables a variety of opportunities (in-class labs, fully remote labs).
- Need better resolution on lab grading other than pass/fail demos.

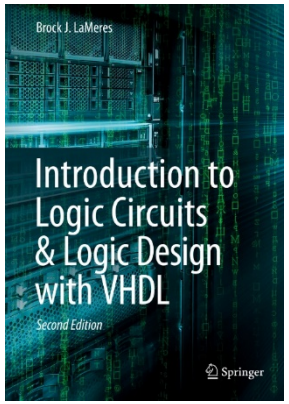
Adaptive Learning Helped Students with Lower GPAs

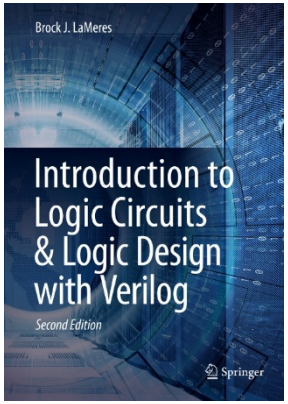
- Has potential to help struggling students with less instructor time.

Course Materials are Available to Other Instructors

- For Universities with Subscription to *SpringerLink*, e-textbooks are free to students.
- All lecture and lab videos are available on YouTube.
- Lab exercises and lab kit BOM available on my website.

Questions


Brock J. LaMeres
Introduction to Logic Circuits & Logic Design with VHDL
Second Edition
Springer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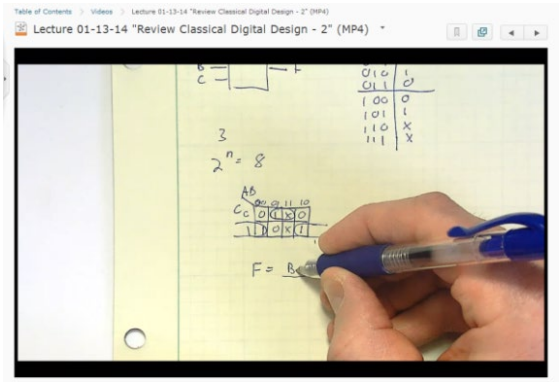
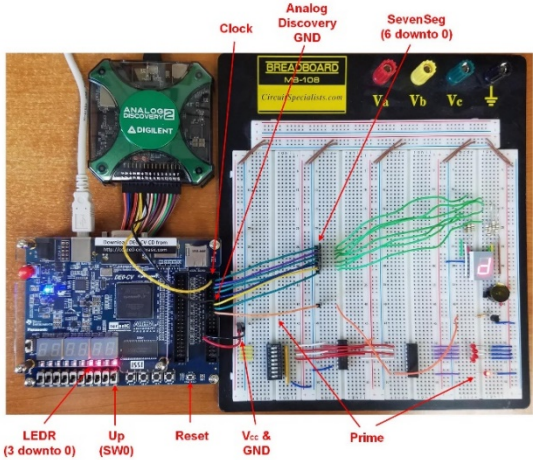

Lecture 01-13-14 "Review Classical Digital Design - 2" (MP4)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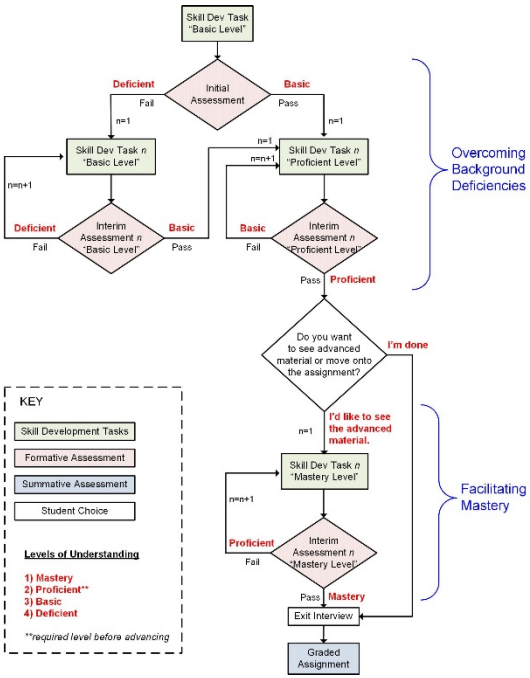
Analog Discovery GND
SevenSeg (6 downto 0)
LEDR (3 downto 0)
Up (SW0)
Reset
Vcc & GND
Prime


Skill Dev Task "Basic Level"
Initial Assessment
Deficient
Fail
Basic
Pass
Skill Dev Task n "Basic Level"
Interim Assessment n "Basic Level"
Skill Dev Task n "Proficient Level"
Interim Assessment n "Proficient Level"
Proficient
Overcoming Background Deficiencies
Do you want to see advanced material or move onto the assignment?
I'm done
I'd like to see the advanced material.
Skill Dev Task n "Mastery Level"
Interim Assessment n "Mastery Level"
Mastery
Exit Interview
Graded Assignment
Facilitating Mastery
KEY
Skill Development Tasks
Formative Assessment
Summative Assessment
Student Choice
Levels of Understanding
1) Mastery
2) Proficient**
3) Basic
4) Deficient
**required level before advancing