Fabrication Process For A Novel High Speed Coplanar-to-Coaxial Off-Chip Interconnect

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Abstract

In this paper, we present the design and fabrication of a novel chip-to-chip interconnect scheme for use in System-in-Package applications. The interconnect system uses an etched trench at the edge of a standard Silicon substrate to interface a miniature coaxial cable to the on-chip surface metal layers. This system delivers a shielded, matched impedance transmission path by using a coplanar structure on-chip and a coaxial structure between chips. This system is designed to be compatible with typical perimeter bonded pad sizing and spacing such that the coplanar-to-coaxial transition can be selectively added to a standard wire bond process on high-speed nets.

1. Introduction

The parasitic inductance and capacitance of off-chip interconnect significantly limits the speed of inter-chip communication links. This is due to the electrical noise caused from impedance discontinuities, return current cross-talk, and signal cross-talk [1,2]. The electrical noise is created by the mechanical construction of the structures making up the interconnect which yields an unshielded signal path and an uncontrolled return path. The most common types of off-chip interconnect are wire bonds and flip-chip bumping with wire bonding being the most widely used connection scheme [3].

System-in-Package (SiP) has been adopted as a way to increase the functionality of a packaged part by encapsulating multiple integrated circuits on a single package substrate. This reduces the total amount of interconnect that off-chip signals must traverse by eliminating the need to enter the system printed circuit board. This topology allows signals to travel between dice without leaving the package [4,5]. A traditional approach to SiP is to use either wire bonding or flip-chip bumping to attach the dice to a package substrate, typically a printed circuit board (PCB). The package PCB contains the signal paths that connect the multiple die. The flexibility of wire bonding has enabled an electrical connection directly between multiple die without the need for a connection to the package PCB. This type of connection has enabled vertical stacking of multiple die which reduces the area impact of the entire packaged part [4].

This new trend of directly connecting multiple die together with wire bonds has increased the integrated functionality of packaged parts. However, this approach uses an interconnect which has a host of electrical drawbacks [6]. The first is the unshielded nature of the wire bond leads to cross-talk between adjacent signal lines. Equations 1 and 2 give the forward and reverse cross-talk coefficients respectively for unshielded interconnect. In these expressions, C_M and L_M reflect the mutual capacitance and inductance between the two interconnects. C_L and L_L represent the self capacitance and inductance of the interconnect and *vel* represents the signal velocity of the signal. Anytime unshielded interconnect structures are used, there will be a non-zero mutual capacitance and mutual inductance which will lead to signal cross-talk.

$$k_f = \frac{1}{2 \cdot vel} \cdot \left(\frac{C_M}{C_L} - \frac{L_M}{L_L} \right) \quad (1)$$

$$k_b = \frac{1}{4} \cdot \left(\frac{C_M}{C_L} + \frac{L_M}{L_L} \right) \quad (2)$$

The second source of noise in a wire bonded system comes from the self inductance of the interconnect in the return path. This inductive nature of the wire bond becomes a problem when conducting return current for multiple signal nets. An $L \cdot (^{di}/_{dt})$ noise is induced on the wire bond which manifests itself as ground and power supply bounce. Equation 3 gives the amount of voltage bounce that will occur due to an inductive return path. In this equation, *N* signifies the number of signals that are sharing a common return path, L_{ret} is the self inductance of the wire bond providing the return path, t_{rise} is the 10-90 signal rise time, and Z_0 is the characteristic impedance of the system.

$$V_{bnc} = N \cdot L_{ret} \cdot \frac{dI_{sig}}{dt} = N \cdot L_{ret} \cdot \frac{0.8 \cdot V_{sig}}{t_{rise} \cdot Z_0} \quad (3)$$

Finally, the inductive nature of the wire bond leads to noise in the form of reflected energy due to impedance discontinuities. The inductive properties of the wire bond lead to a relatively high impedance compared to the system (typically 50Ω) following equation 4. In this equation, L and C are the total inductance and capacitance of the wire bond.

$$Z_{wb} = \sqrt{\frac{L_{wb}}{C_{wb}}} \quad (4)$$

Impedance mismatches lead to reflections which are described by the *reflection coefficient*, Γ (equation 5). Γ depends on the characteristic impedance that the wave is currently traveling in (Z_0) and the load impedance immediately in front of the incident wave (Z_L, or Z_{wb}).

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (5)$$

In this paper we present a method to reduce the noise sources described by equations 1-5 by replacing the wire bond with a novel interconnect scheme using a miniature coaxial cable to directly connect two dies. The miniature coaxial cable is designed to interface to coplanar transmission lines on each of the two dies it is connecting to yield a matched impedance system. The shielded nature of the coaxial interconnect will prevent any coupling between adjacent signal lines, thus eliminating forward and reverse traveling cross-talk (equations 1 and 2). In addition, since the coaxial structure inherently provides its own return current path through the low impedance outer shield, the power/ground bounce noise described in equation 3 will be reduced. And finally, since the coaxial and coplanar transmission lines are designed to be 50Ω, there will be considerably less impedance discontinuities as the signal travels through the interconnect so the noise due to reflected energy (equation 5) will be minimized.

2. Design Methodology

Our proposed technique involves using a miniature coaxial cable as a chip-to-chip interconnect. The coaxial cable is designed to interface to a coplanar (G-S-G) structure located on a Silicon (Si) substrate. A trench is etched within the coplanar structure adjacent to the edge of the die which accepts the coaxial cable. The outer shield of the coaxial cable makes electrical contact to the outer ground nets of the coplanar structure. The center conductor of the coaxial cable extends out of the shielded portion of the cable and makes contact with the center signal net of the coplanar structure. The etched trench provides 3 purposes in this system. The first is to mechanically strain relieve the interconnect structure that extends from the edge of the die. The second function is to align the center conductor of the coaxial cable to the signal net of the coplanar structure. This alignment is accomplished inherently as the coaxial cable is inserted into the trench. The third function of the trench is to position the outer shield of the coaxial cable to the two ground nets of the coplanar structure so that an electrical connection can be made. Figure 1 shows a side view of how this approach can be used to connect two adjacent dies within a single package. Figure 2 shows a 3D perspective of multiple coaxial connections extending from a single die.

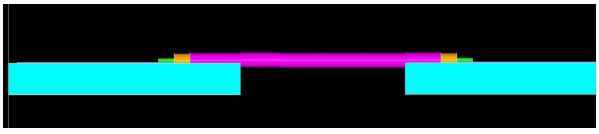

Figure 1. Side View of the Proposed Interconnect System Connecting Two Adjacent Dies.

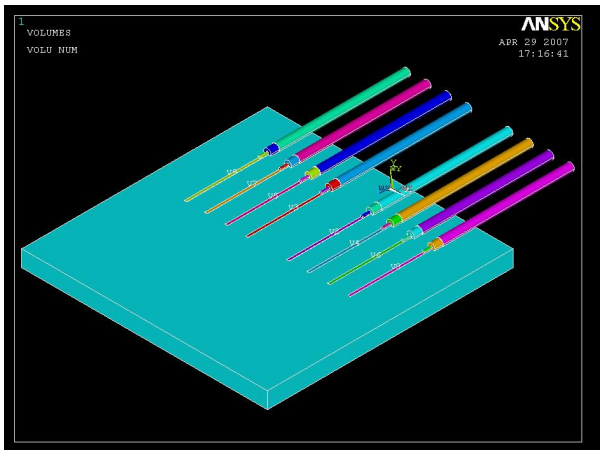

Figure 2. 3D Perspective of Multiple Coaxial Connections Extending from a Single Die.

2.1 Use-Model

The proposed technique is designed to be selectively added to high speed nets on a typical perimeter bonded IC. The bond pads are assumed to be 100µm x 100µm and have pad spacing of 100µm [4]. For high speed nets with bond pad signal assignments of G-S-G, an additional process step is added to the integrated circuit fabrication process in order to form a trench that will accept a miniature coaxial cable. This technique is intended for use in conjunction with traditional wire bond interconnect, which are still used on low speed and power supply nets.

The G-S-G signal assignment on the bond pads makes an ideal configuration for a controlled impedance, coplanar transmission line between the diffusion regions of the IC and the off-chip pads. In order for this technique to be feasible, the spatial requirements for the trench and mating coaxial cable must fit within the typical G-S-G bond pad geometries used on a perimeter bonded IC.

Figure 3 shows an example use-model for this technique showing both wire bonding and coplanar-to-coaxial interconnects in the same package.

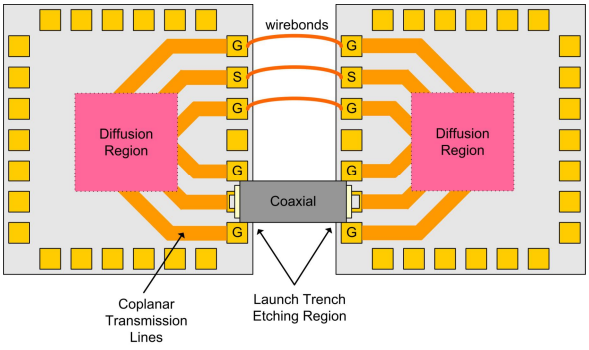

Figure 3. Example Use-Model of Proposed Technique.

2.2 Coaxial Dimensions

The key dimensions that drive the design of the interconnect system are the features of the miniature coaxial cable. In our design, we have evaluated two versions of a miniature, semi-rigid, 50Ω, coaxial cable from *Micro-Coax*© [7]. The coaxial cable consists of a silver-plated, copper clad steel (SPCW) center conductor covered with an insulating layer of Polytetrafluoroethylene (PTFE). The outer conductor is created with a solid tubular layer of copper. The two semi-rigid coaxial cables that were evaluated in this work were the *Micro-Coax*© UT-013 and the *Micro-Coax*© UT-020 with overall diameters of 330μm and 584μm respectively. Figure 4 shows the key dimensions for the coaxial cables used in our approach.

2.3 Coplanar Dimensions

A coplanar transmission line is created using 3 traces of metal residing on the same plane. The inner trace carries the signal wave while the two outer traces carry the ground or return current. The width and thickness of the traces (W_{sig}, W_{gnd}, and T_{sig}), the spacing between the traces (S_{copl}), and the materials of the structure (ε_{r1} and ε_{r2}) dictate the characteristic impedance of the transmission line. Figure 5 shows a cross-section of a coplanar transmission line fabricated on a p-type Silicon substrate. When constructing a coplanar structure on a p-type Silicon structure, a thin layer of Silicon Oxide (SiO_2) is inserted between the semiconductor substrate and the metal to provide a layer of insulation (T_{ox}). In our system, we used Aluminium to form the 3 traces used in the coplanar transmission line. The impedance of the structure was designed to be 50Ω to match the impedance of the coaxial cable and eliminate reflections due to the off-chip interconnect path.

2.4 Trench Dimensions.

A trench is formed within the coplanar structure such that the coaxial cable can be inserted and make electrical contact between the signal and ground conductors for both the coplanar and coaxial structures. The return path is accomplished by etching the trench within the coplanar structure but without removing any of the metal forming the two outer layer return traces. When the coaxial cable is laid in the trench, its outer shield will be adjacent to the ground lines of the coplanar transmission line.

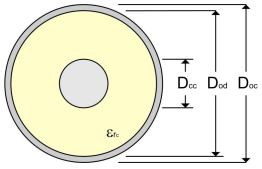

Figure 4. Critical Dimensions for the Miniature Coaxial Cable.

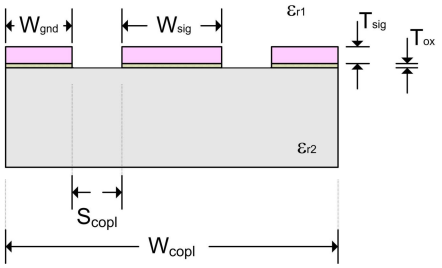

Figure 5. Cross-Section and Critical Dimensions of a Coplanar Transmission Line.

The signal path is formed by exposing the center conductor of the coaxial cable. When the coaxial cable is inserted into the trench, the center conductor will come to rest on top of the signal trace of the coplanar structure. The size of the coplanar transmission line (W_{sig}, W_{gnd}, and T_{sig}) and the size of the trench (W_{ttop}, W_{tbot}, H_{tsw}, and W_{tsw}) are designed to achieve both a 50Ω impedance and the proper alignment of the coplanar to coaxial transition. Figure 6 shows a cross-section of the trench formed within the coplanar structure annotating the critical dimensions. Figures 7 and 8 show side and top view of the assembled interconnect structure respectively.

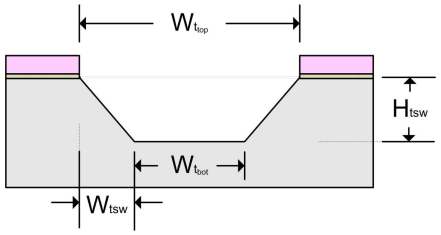

Figure 6. Cross-Section and Critical Dimensions of the Coplanar-to-Coaxial Trench.

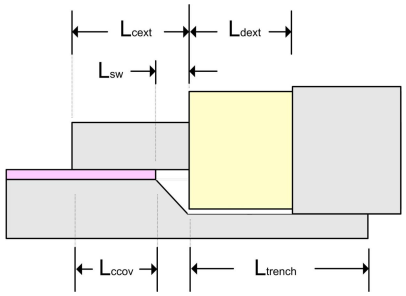

Figure 7. Side View of the Coplanar-to-Coaxial Transition with the Coaxial Cable Inserted into the Trench.

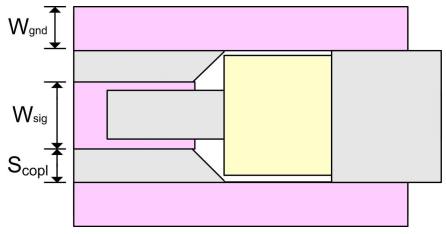

Figure 8. Top View of the Coplanar-to-Coaxial Transition with the Coaxial Cable Inserted into the Trench.

2.5 System Dimensions.

Adjacent coplanar-to-coaxial structures can be placed on a pitch defined by S_{SS} as shown in figure 9. Table 1 lists all of the dimensions for our proposed technique for two sizes of miniature, semi-rigid coaxial cable (UT-013 and UT-020).

This table illustrates the incremental area impact of our approach when compared to a typical wire bonded system. In a wire bonded system, a high speed net typically requires 3 bond pads in order to achieve a G-S-G configuration. The perimeter length required for this arrangement consists of the widths of the 3 wire bond pads (W_{pad}) plus the spacing between the pads (S_{pad}). Assuming a 100μm x 100μm bond pad (W_{pad}=100μm) with pad spacing of 100μm (S_{pad}=100μm), the total distance required is [3·Wpad + 2·S_{pad}] = 500μm along the perimeter. In our approach, when using the UT-013 coaxial cable the total distance needed consists of the width of the top of the trench (W_{ttop}=349μm) plus the width of the two ground pads (W_{pad}=100μm). This gives a total perimeter length of [W_{ttop} + 2·W_{pad}] = 549μm per signal. Our approach requires only a 9.8% increase in perimeter to accommodate the coplanar-to-coaxial transition.

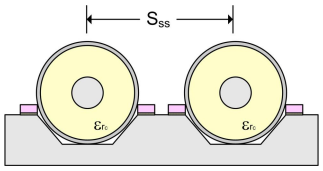

Figure 9. Cross-Section of the Multiple Coplanar-to-Coaxial Interconnect Structures.

Region	Parameter	Units	Coaxial Line	
			UT-013	UT-020
Coaxial	D_{oc}	μm	330	584
	D_{od}	μm	254	419
	D_{cc}	μm	79	127
Coplanar	T_{sig}	μm	1	1
	T_{ox}	μm	0.8	0.8
	W_{sig}	μm	239	446
	W_{gnd}	μm	100	100
	S_{copl}	μm	55	90
	W_{copl}	μm	549	826
	S_{ss}	μm	634	916
Trench	W_{ttop}	μm	349	626
	W_{tbot}	μm	150	228
	W_{tsw}	μm	100	199
	H_{tsw}	μm	126	229
Transition	L_{trench}	μm	900	801
	L_{dext}	μm	500	500
	L_{sw}	μm	100	199
	L_{cext}	μm	500	500
	L_{ccov}	μm	401	301

Table 1. Dimensions for Coplanar-to-Coaxial System.

3. Fabrication Process

This section lists the details of how the integrated circuit substrate is processed in order to create the trench and coplanar metal layers used for our interconnect system.

The process begins with a 100mm diameter, p-type Silicon wafer with a <100> crystal orientation. The Si wafer is cleaned to remove any contamination using a modified RCA process. The cleaning process involves submerging the wafer in a sequence of three solutions. The first solution used is a mixture of sulphuric acid and hydrogen peroxide to remove any organic material on the wafer. The second solution is a buffered oxide etch (BOE) consisting of a hydrofluoric acid diluted 10:1 with di-ionized (DI) water in order to remove any SiO_2. Finally a solution of hydrochloric acid, water, and hydrogen peroxide is used to remove any metal ions. In between each of these cleaning steps the wafer is rinsed in DI water. This step is reflected figure 10.a.

The next set of process steps will etch the trench into the Si substrate. First, a protective layer of SiO_2 is grown on the wafer. The wafer is put into an oxidation furnace for 3 hours at 1050 ºC. This produces a layer of SiO_2 1μm thick (figure 10.b). Next, a layer of *Shipley 1813* positive photo resist (PR) is spun onto the wafer. A 1μm layer of PR is applied by spin coating the wafer at 5000 RPMs for 30 seconds. The PR is then hardened by baking the wafer for 90 seconds at 115 ºC (figure 10.c). Photolithography is next performed using a dark field mask. The PR is exposed to UV light for 4.5 seconds at an intensity of 20 mW/cm^2 (figure 10.d). The PR is then developed by submersing the wafer in *MF 319 developer* solution for 60 seconds. The soluble PR is then removed using an acid wash. The remaining PR is hardened by a subsequent bake in order to make it resilient enough to withstand the forthcoming SiO_2 etch (figure 10.e). The SiO_2 is then etched using a BOE process (figure 10.f). The remaining PR is then stripped off using a sequence of acetone, isopropyl alcohol (IPA), methanol, and DI water (figure 10.g). The exposed Si substrate is etched using a Tetramethylammonium hydroxide (TMAH) solution at 25% weight (figure 10.h). This solution produces an anisotropic etch rate of 10.5μm/hr at 75 ºC for our <100> crystal orientation. TMAH also exhibited a 1/1000 selectability for SiO_2 at 75 ºC so our 1μm of SiO_2 is sufficient to protect the substrate for an etch depth up to 1000μm. Finally, all remaining SiO_2 is stripped using a BOE process (figure 10.i).

The next set of process steps deposit the metal used for the coplanar traces. First, the Si wafer is cleaned using the modified RCA process mentioned above. A 1μm layer of SiO_2 is grown on the substrate using the same oxidation process mentioned above (figure 10.j). Next, Aluminum (Al) is deposited on the topside of

the wafer using an evaporation process (figure 10.k). Photo resist is then applied (figure 10.l) and a light field photolithography step is performed to expose selected regions of the PR (figure 10.m). The PR is developed and the soluble photo resist is removed (figure 10.n). The remaining PR is hardened with a subsequent bake. Next, the exposed Aluminum is etched away using a sequence of Acetone, IPA, Methanol, and DI water (figure 10.o). Finally, all remaining SiO_2 is stripped using a BOE process (figure 10.p).

4. Experimental Results

Prototypes of the coplanar–to-coaxial interconnect system were fabricated at the Montana Microfabrication Facility (MMF) at Montana State University, Bozeman. The masks were designed using the Cadence *Virtuoso* layout system. The masks were fabricated at the University of Minnesota's Nanofabrication Center. Each die was designed to be 12mm x 12mm in size. On each die, features were included to experiment on a variety of design variables.

Figure 11.a shows the top view of our prototype die showing 3 adjacent coplanar transmission lines and 3 etched trenches. Figure 11.b shows a zoomed in view of the coplanar structures in our prototype. The dimensions in this figure correspond to the UT-013 row of table 1. Figure 11.c shows a single coplanar transmission line that did not undergo any trench etching. The square features along the top in this picture are 100µm x 100µm wire bond pads separated by 100µm.

5. Conclusion

In this paper we presented the design and fabrication of a novel coaxial-to-coplanar interconnect scheme for directly connecting multiple dies in a SiP application. By using a shielded interconnect with controlled impedance, noise from cross-talk and impedance discontinuities can be reduced or eliminated. Our approach was constructed to be selectively added to a perimeter bonded system for high speed nets using a G-S-G pad assignment. For this situation, we showed that our approach only adds an incremental 9.8% in linear distance along the perimeter compared to the traditional wire bond approach. We demonstrated the feasibility of creating the interconnect transition trench needed for our system using standard CMOS fabrication process steps.

6. Future Work

Work is currently underway on the electrical characterization of our approach in addition to the automated assembly of the interconnect connection.

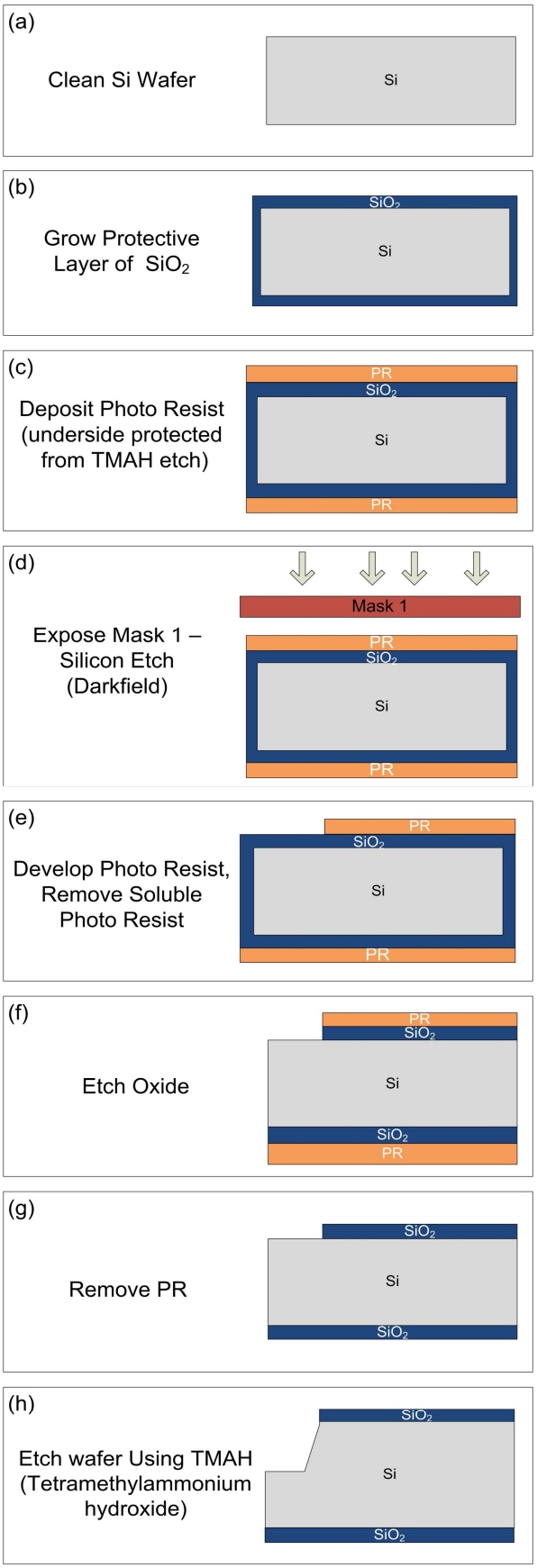

Figure 10. Process Steps for the Coplanar-to-Coaxial Transition.

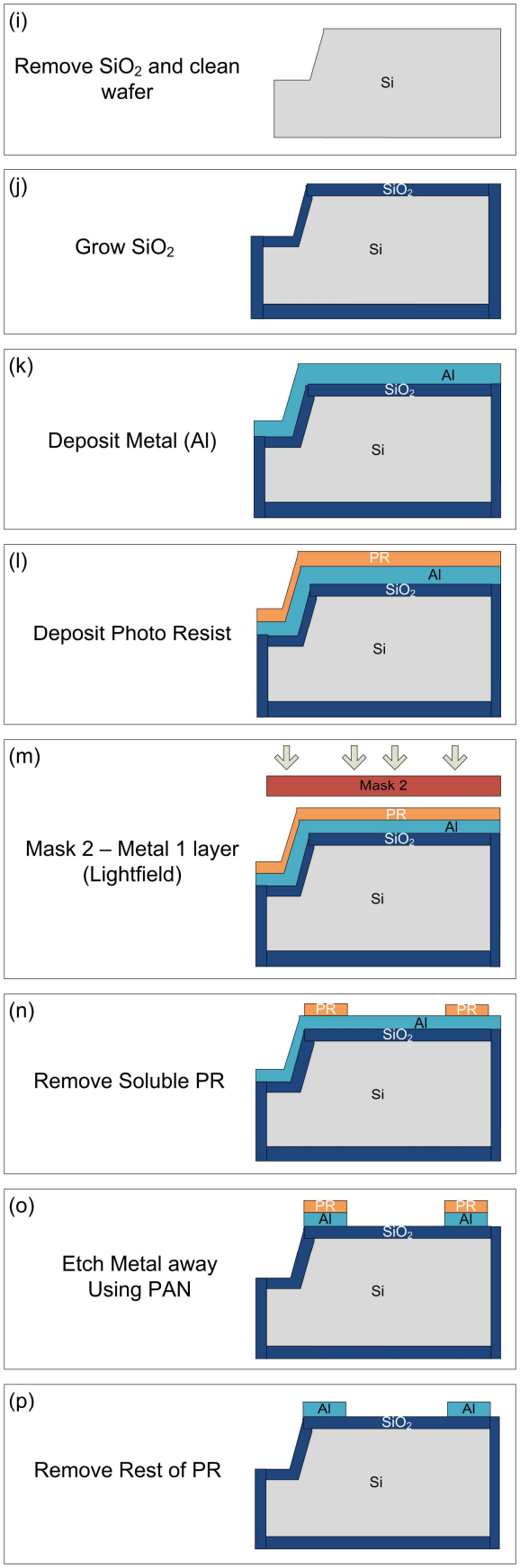

Figure 10 cont…. Process Steps for the Coplanar-to-Coaxial Transition.

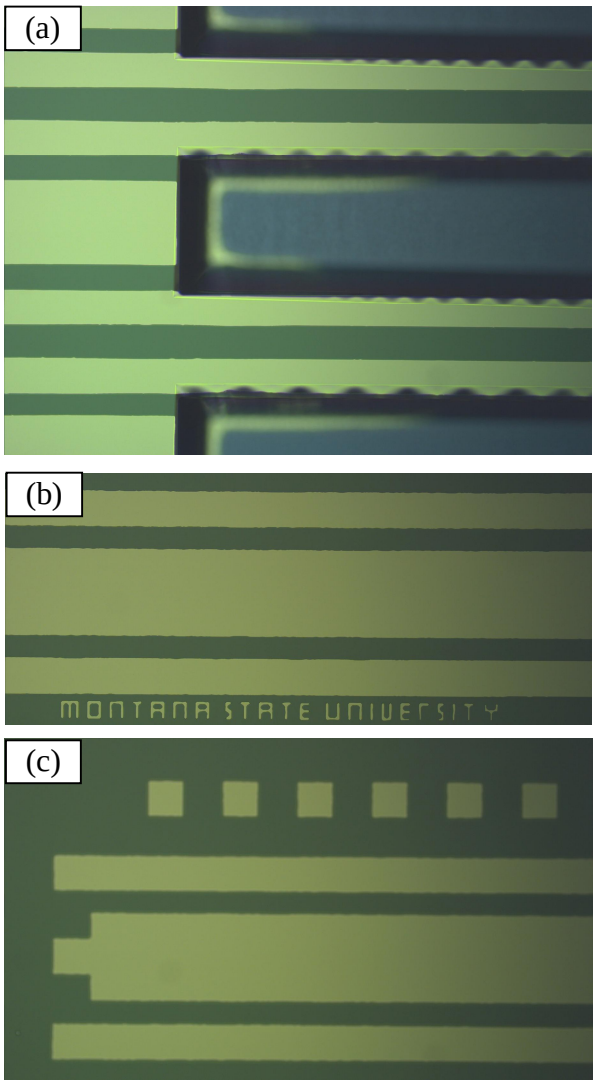

Figure 11. Prototypes of Coplanar-to-Coaxial Transition Fabricated at Montana State University.

References

[1] M. Miura, N. Hirano, Y. Hiruta, and T. Sudo, "Electrical Characterization and modeling of simultaneous switching noise for leadframe packages", *Proceedings of the 45th Electronic Components and Technology Conf*, pp. 857-864, May 1995.

[2] M. Miura, N. Hirano, Y. Hiruta, and T. Sudo, "Characterization and Reduction of SSN for a Multilayer Package", *Proceedings of the 44th Electronic Components and Technology Conference*, pp. 949-956, May 1994.

[3] B. Young, "Return path inductance in measurements of package inductance matrixes", *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, vol. 20, pp. 50-55, Feb 1997.

[4] "The International Technology Roadmap for Semiconductors", www.itrs.net, 2007.

[5] Hopkins, Edenfield, Hampton, & R. Roberts, "A New Coax to Troughguide Transition", *IEEE Microwave and Wireless Components Letters*, vol. 12, issue 8, pp. 299-301, Aug 2002.

[6] Y. Hao and D. Zhang, "Silicon-based MEMs process and standardization", *Proceedings of the 7th International Conference on Sold-State and Integrated circuits Technology*, vol. 3, pp. 1835-1838, 2004.

[7] Micro-Coax©, www.microcoax.com