
Advanced Packaging : Advanced Packaging I

Session We-A-2

September 3, 2008

Fabrication Process For A Novel High Speed CoPlanar-to-Coaxial Off-Chip Interconnect

Chris McIntosh & Brock J. LaMeres
Montana State University
Bozeman, MT, USA



“Fabrication Process For A Novel High Speed
CoPlanar-to-Coaxial Off-Chip Interconnect”

Introduction

- Drawback of wire bonds
- Use of coax cable to overcome drawbacks
- Use of cable of chip
- Fabrication process
- Early Results
- Future work



Wire Bonding

- Electrical Drawbacks
 - Unshielded nature
 - Generates considerable signal cross-talk

$$K_f = \frac{1}{2 \bullet vel} \bullet \left(\frac{C_M}{C_L} - \frac{L_M}{L_L} \right) \quad \longrightarrow \quad \text{Forward cross-talk (FEXT)}$$

$$K_b = \frac{1}{4} \bullet \left(\frac{C_M}{C_L} + \frac{L_M}{L_L} \right) \quad \longrightarrow \quad \text{Reverse cross-talk (NEXT)}$$

Where,

$$FEXT = \frac{V_f}{V_a} = \frac{L}{RT} * k_f \quad \quad \quad NEXT = \frac{V_b}{V_a} = k_b$$



Wire Bonding

- Electrical Drawbacks (cont)
 - Self Inductance of the return path

$$V_{bnc} = N \bullet L_{ret} \frac{0.8 \bullet V_{sig}}{\tau_{rise} \bullet Z_0} \quad \longrightarrow \quad \text{Voltage Bounce due to inductive return path}$$

N – number of signals sharing common return path

L_{ret} – self inductance of wire bond providing return path



Wire Bonding

- Electrical Drawbacks (cont)
 - Reflected energy due to impedance discontinuities

$$Z_{wb} = \sqrt{\frac{L_{wb}}{C_{wb}}} \quad \longrightarrow \quad \text{Impedance of wire bond}$$

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \quad \longrightarrow \quad \begin{array}{l} \text{Reflection coefficient} \\ \bullet Z_L - \text{Load impedance} \\ \bullet Z_0 - \text{Source side impedance} \end{array}$$



Coaxial cable

- Reasons for cable use

- Signal cross-talk is reduced by shielded cable

$$K_f = \frac{1}{2 \bullet vel} \bullet \left(\frac{C_M}{C_L} - \frac{L_M}{L_L} \right) \quad K_b = \frac{1}{4} \bullet \left(\frac{C_M}{C_L} + \frac{L_M}{L_L} \right)$$

- Self Inductance is significantly less due to number of signals sharing return path

$$V_{bnc} = N \bullet L_{ret} \frac{0.8 \bullet V_{sig}}{\tau_{rise} \bullet Z_0}$$

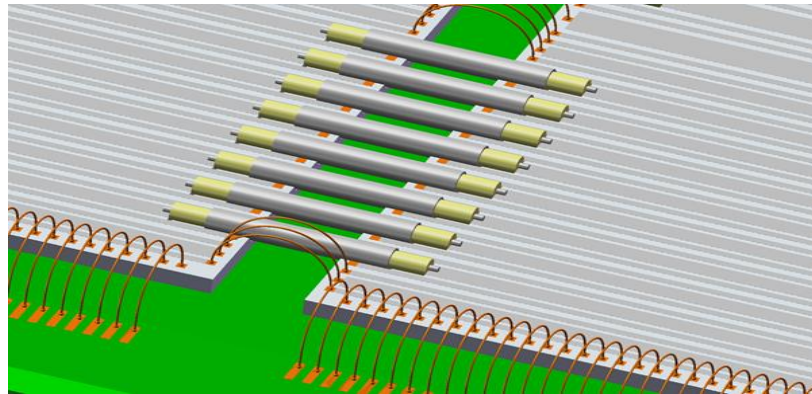
- Reflected energy is reduced by controlled impedance of the cable

$$Z_c = \sqrt{\frac{L_c}{C_c}} \quad \Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$



What's the Target Goal?

- Provide a chip-to-chip interconnect system
- Replace critical wire bond interconnect
- System will provide
 - Shielding (reducing cross talk)
 - Matched impedance transmissions
 - Increased signal transmission lengths
 - Increased speed



Major steps

- Cable selection
- Wafer selection
- Design waveguide dimensions
- Trench fabrication
- Waveguide fabrication
- Assembly and Testing



Cable selection

- Impedance equal to 50Ω
- Size less than $600\mu\text{m}$
- Bigger than $300\mu\text{m}$
- Type - Semi-rigid
- Outer shield is the ground path



Selected cable

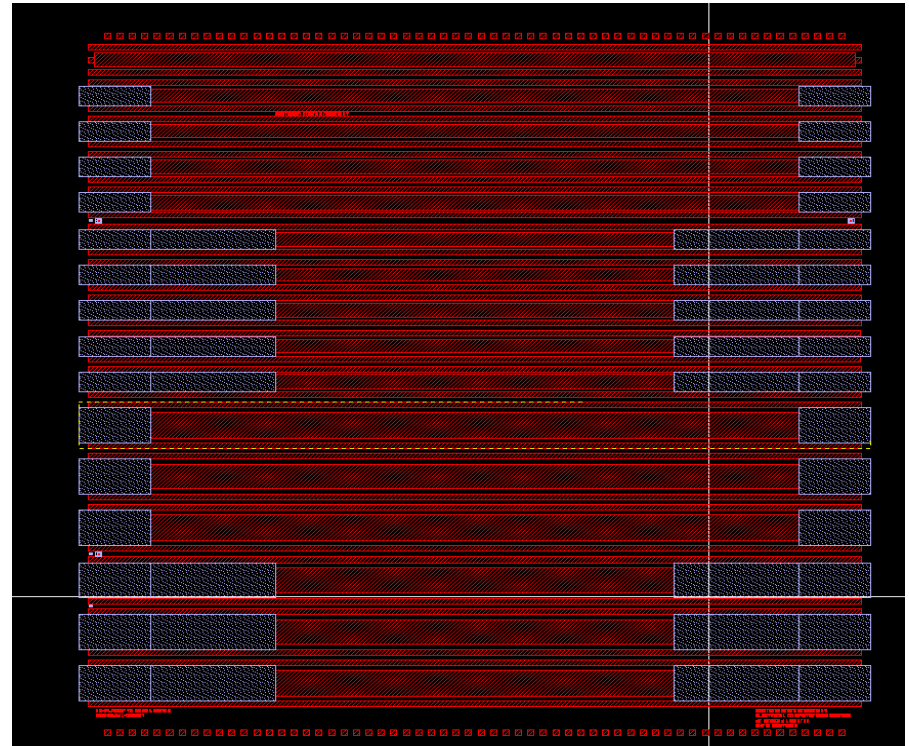
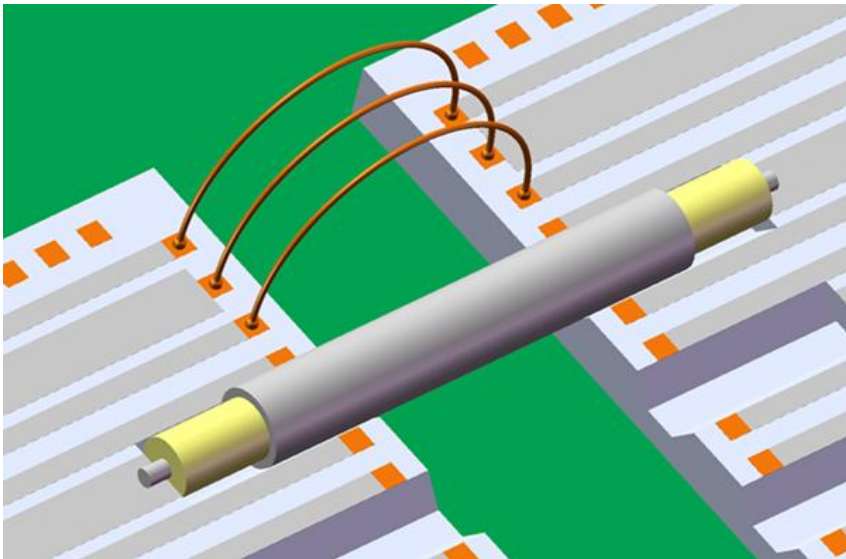
- MICRO– COAX
 - UT-020 & UT-013 semi-rigid cable

	UT – 013	UT – 020
Outer Dia (um)	330 (+/- 25.4)	584 (+/- 25.4)
Dielectric Dia (um)	254	419
Center Conductor Dia (um)	78.7 (+/- 12.7)	127 (+/- 12.7)
Impedance (ohms)	50 +/- 2.0	50 +/- 2.0
Material - Outer conductor	Copper	Copper
Material - Dielectric	PTFE	PTFE
Material - Center Conductor	SPCW	SPCW



Test Chip Layout

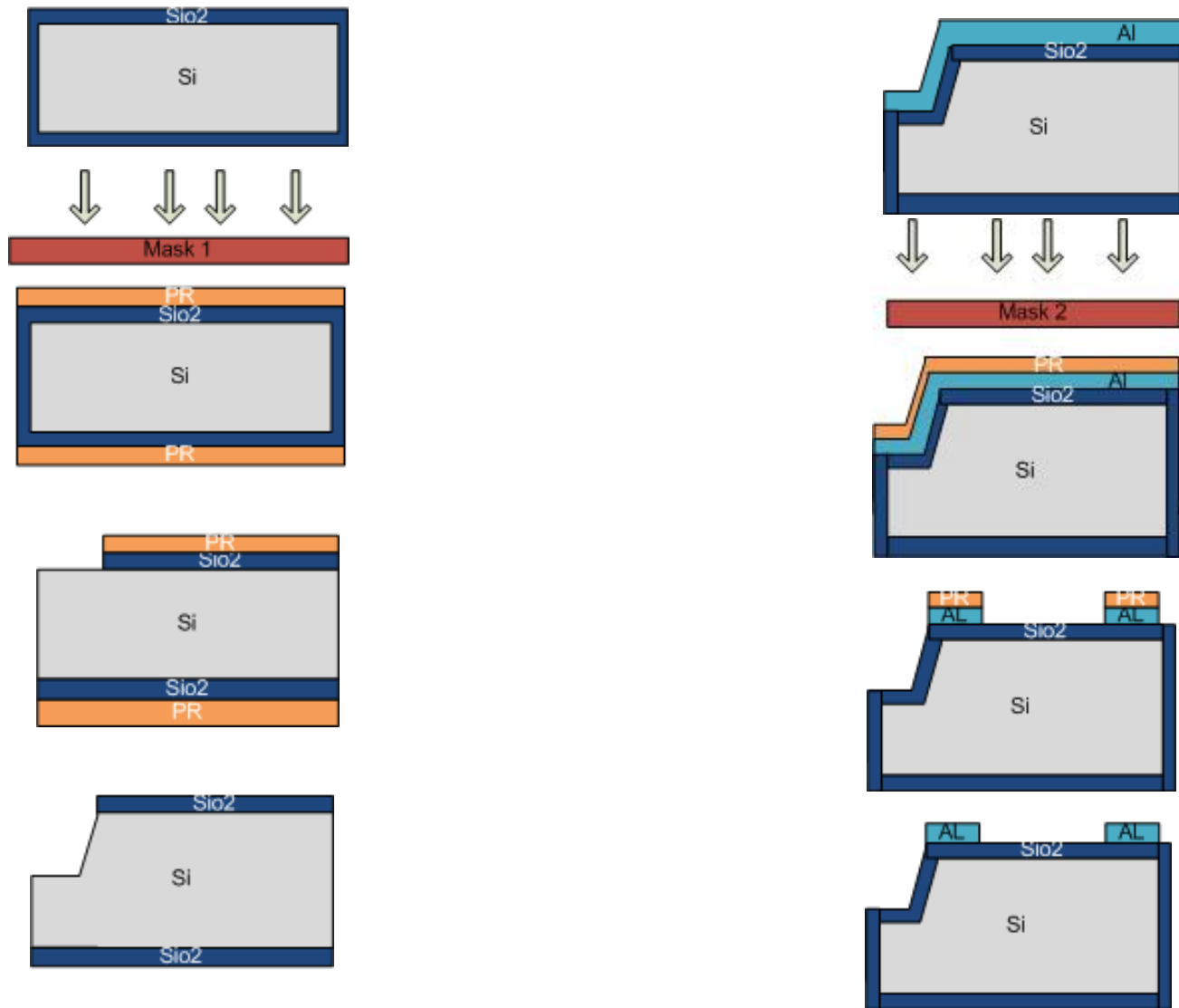
Test chip layout



3D model of Chip-to-Chip
interconnect



Process Steps

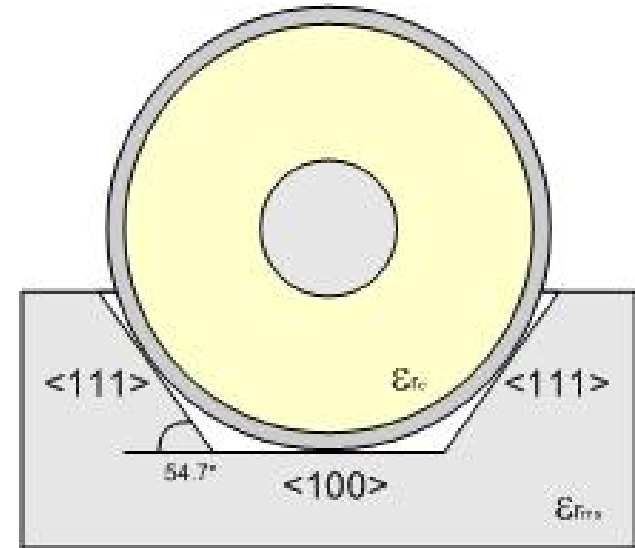


Trench Etching

- Anisotropic etch
 - TMAH
- SiO₂ as mask
- Depth of trench:

$$\frac{\text{Outer Cable Dia}}{2} - \frac{\text{Inner Cable Dia}}{2}$$

- Trench run from Gnd trace to Gnd trace

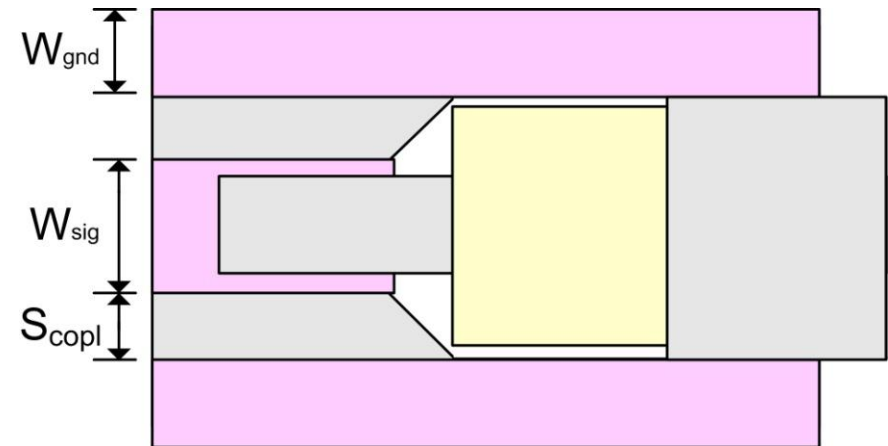


Co-Planar WaveGuides

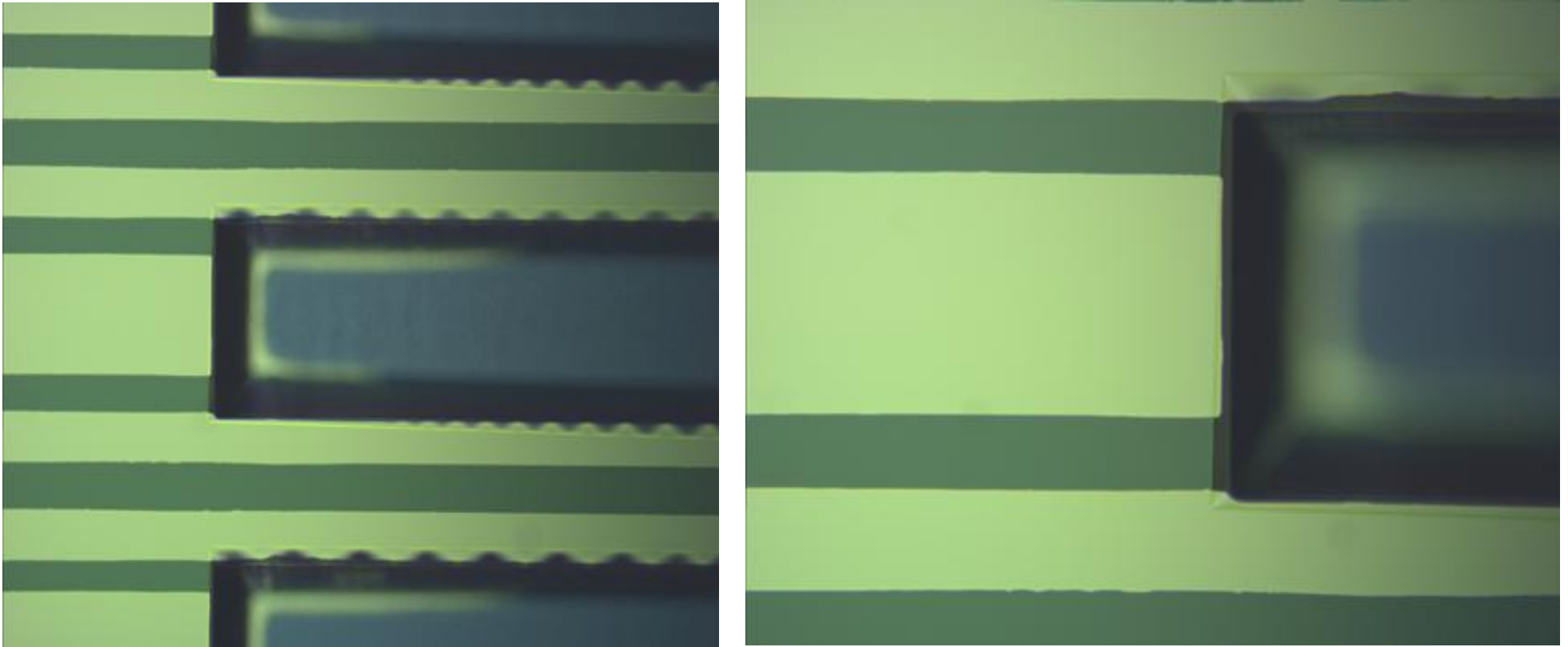
- Why was Co-Planar chosen?
- Overall structure size

$$2W_{\text{gnd}} + W_{\text{sig}} + 2S_{\text{copl}}$$

- W_{sig} , S_{copl} , & ϵ determine Z_0
- W_{gnd} set to 100um
- Cable striped in stages
 - Helps reduce edge affects



Etched Trenches & WaveGuides

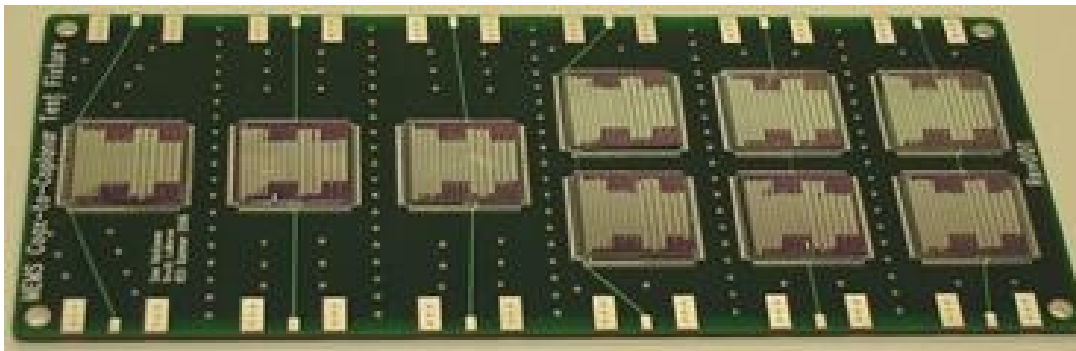
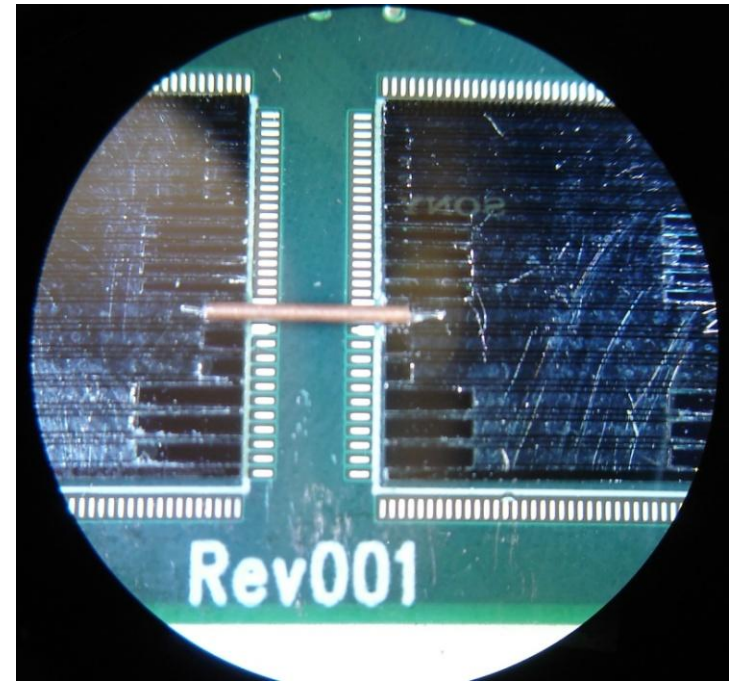


Figures show etched trenches with Aluminum traces deposited



PCB Test Fixture

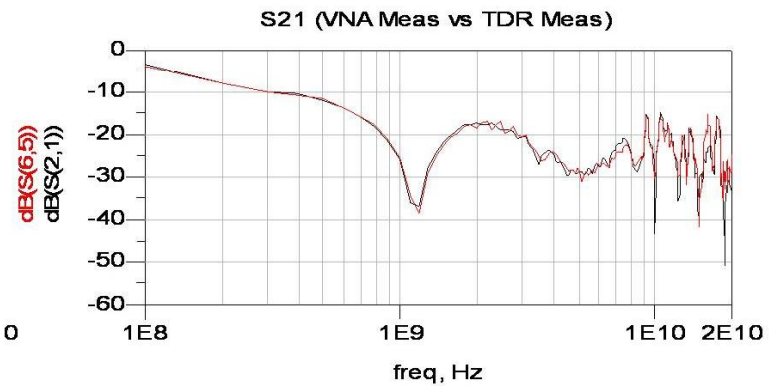
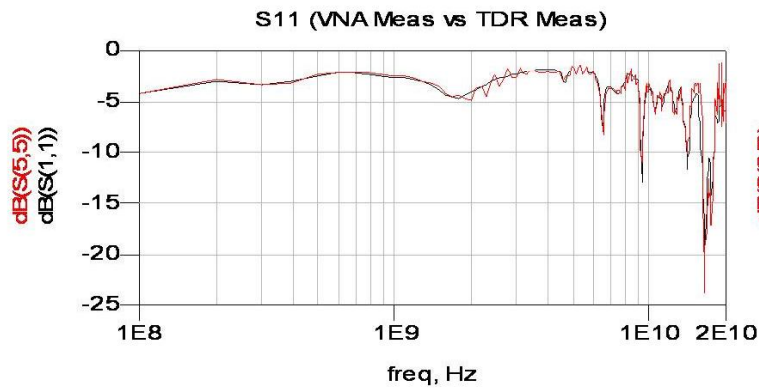
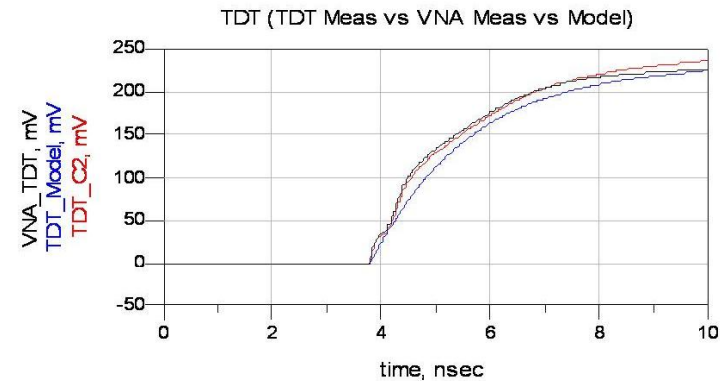
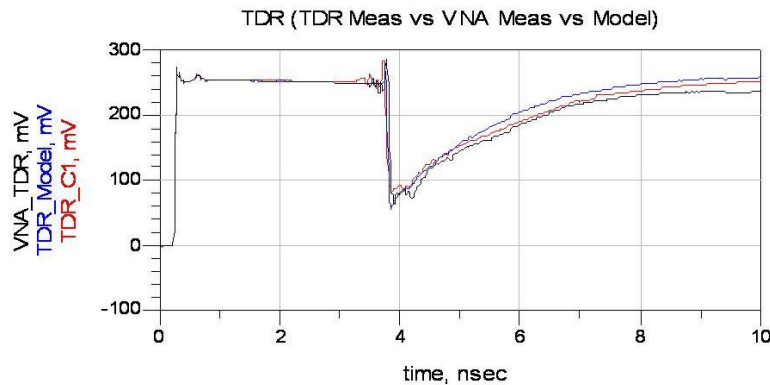
Two dies with Coaxial cable
embedded within the etched
trenches



Test PCB boarded used to
mount the dies, includes
wire bonding pads



Early Results



Possible Future Work

- Using UT-008 cable
 - Outer dia 203 μm
 - Gives the following Coplanar dimensions
 - $W_{\text{sig}} = 120\mu\text{m}$
 - $S_{\text{copl}} = 40\mu\text{m}$
 - $W_{\text{gnd}} = 50\mu\text{m}$
- Total structure footprint
 - 300 μm
 - Footprints 43% less compared to UT-013
- Use of thick dielectric for trench

