A Power Efficient Approach to Radiation Hardened Digital Circuitry Using Dynamically Selectable Triple Modulo Redundancy

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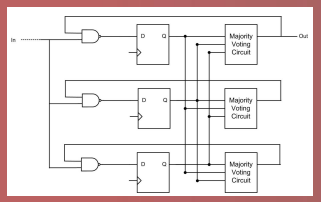
Abstract

Triple Modulo Redundancy (TMR) is one of the most common techniques for fault mitigation in digital systems. TMR-based computing has a natural application to mission critical systems for military and aerospace applications which are exposed to cosmic radiation and are susceptible to Single Event Upsets (SEUs). TMR's increased immunity to SEUs comes at the expense of increased power consumption and area. This paper presents a dynamically selectable TMR architecture which can be used to reduce power consumption when radiation levels are low. We apply this architecture to a test system in order to evaluate its power reduction and area overhead compared to a traditional static TMR approach. We show that the dynamically selectable TMR can be adopted with only a 2.2% increase in equivalent gates compared to a traditional static TMR approach for our test circuit. Dynamic TMR has the potential to lower power consumption by 66% in radiation free environments by disabling two of the three redundant circuits.

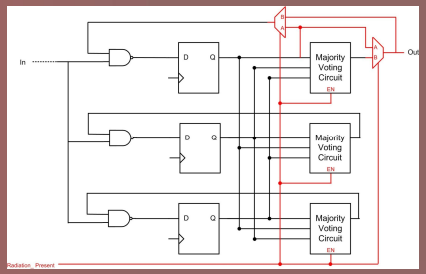
Static TMR

TMR achieves fault mitigation by using three identical circuits to perform each task. A voting machine then looks at the outputs of the three redundant circuits and selects the majority as the final output of the system. The assumption is that if a fault occurs, it will likely only occur in one of the circuits while the other two are unaffected. The voting machine also contains circuitry to reinitialize the corrupted circuit. This technique is ideal for radiation hardening of computer systems because radiation strikes tend to be localized. The drawback of this approach is the additional power and area consumption required by the redundant circuitry.



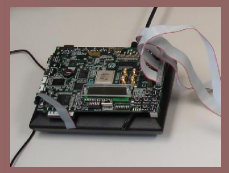
Dynamic TMR

In our approach, we propose a dynamically selectable TMR circuit that is under the control of an external radiation sensor that detects when radiation is present. Under normal operation (i.e., no radiation detected), the TMR circuitry is disconnected from the main logic path, thus consuming no extra power from the system. When the sensor detects radiation, the TMR circuitry is enabled and redundancy checking is performed. This approach allows the average power of the system to be reduced by not using TMR checking when the circuit resides in a radiation free environment. This approach uses slightly more area than a straight TMR approach; however, the power consumption is reduced considerably. This type of logical solution is ideal for implementation in commercial off-the-shelf FPGAs.



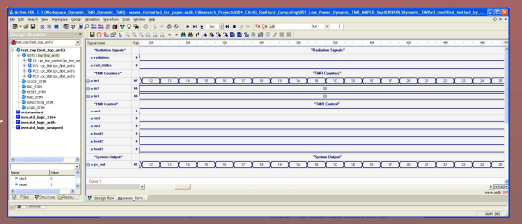
Implementation

We applied our dynamic TMR technique to an 8-bit Program Counter. The circuitry was designed and simulated using VHDL. The design was synthesized and implemented on a Xilinx Virtex-4 FPGA to examine the resource requirements.

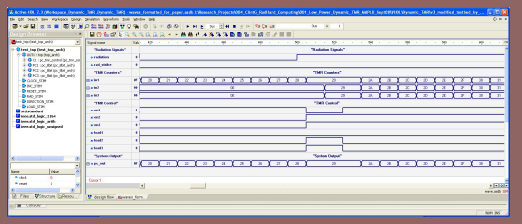


Logical Operation

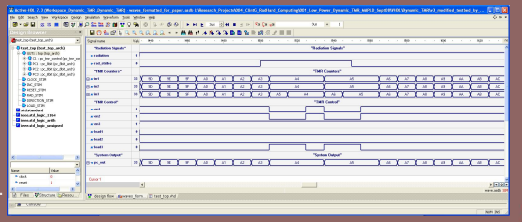
In a radiation free environment, the system disables two of the three redundant counters to reduce power (in2 & in3).



When radiation is detected by the external sensor (radiation), the system enables the two redundant counters (en2, en3) and loads them (load2, load3) with the current count value (in1). During this time, the system output pauses (pc_out) to accommodate the start-up time of the two redundant counters.



While in heavy radiation, the system performs traditional TMR. If a radiation strike occurs (rad_strike) that corrupts one of the counters, (in3) the system attempts to reload the effected counter with the majority value of the three counters.



Results

We compared our approach to a traditional static TMR design when implemented in the same FPGA. The following table shows the resources used for each design. Dynamic TMR can be implemented with only a 2.2% increase in equivalent gate count compared to a traditional static TMR approach yet has the functionality to achieve a power savings of up to 66% in low radiation environments.

FPGA Resources	Resources Used		
	Static TMR	Dynamic TMR	Area Increase
Total # of Slice Registers	39	41	5.1%
# used as Flip Flops	25	27	8.0%
# used as Latches	14	14	0.0%
Total # of 4 Input LUTs	139	143	2.9%
Total Equiv. Gate Count	1291	1319	2.2%