Design of a Radiation Tolerant Computing System Based on a Many-Core FPGA Architecture

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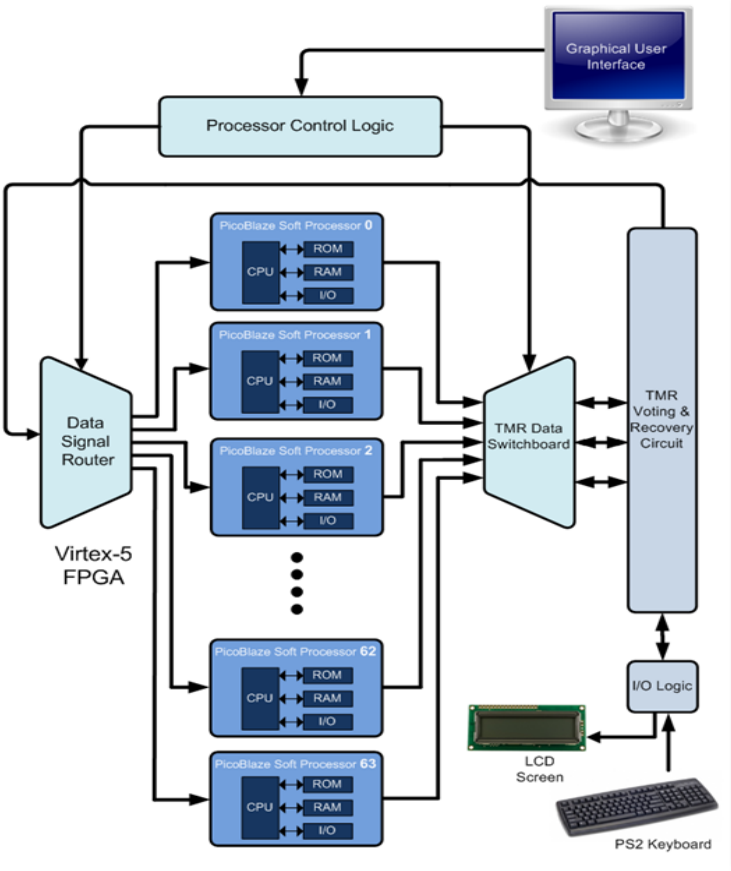
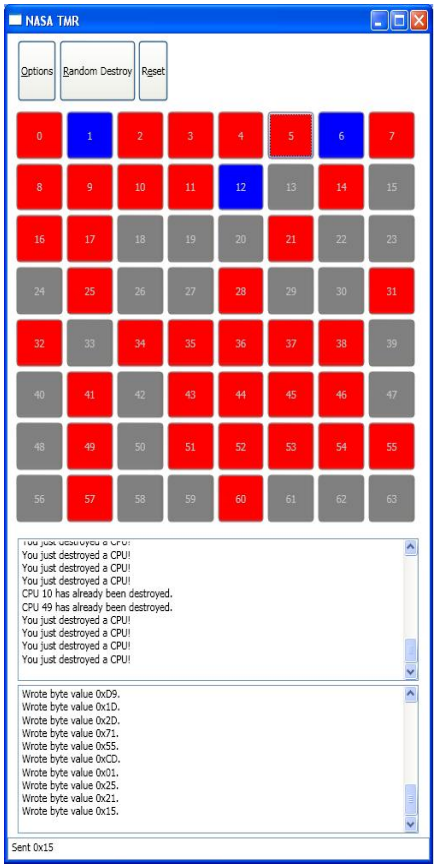
When high-energy cosmic particles strike integrated circuits, fault conditions called Single Event Phenomena's occur. Single Event Upsets (SEUs) occur when the particles create soft errors such as inadvertent logic level switching that is captured in a digital storage device. SEUs can typically be remedied using redundant circuitry and a voting system or with software resets. Single Event Damages (or hard faults) on the other hand, cause physical damage to the circuit and cannot be remedied by a simple system reset. Instead, other mitigation techniques, such as swapping in spare circuitry must be used to provide a robust computing system. In this paper, a redundant, many-core computing system is presented that was designed on a field programmable gate array (FPGA). The system design implements 64 PicoBlaze soft processors to provide spare circuitry in the event of a hard failure. Upon startup, three of the processors are activated and used in a Triple Modular Redundant (TMR) configuration in order to detect and recover from SEUs. The remaining 61 processors are inactive and used as spares in the event of a hardware failure. If a hardware failure is detected, the system automatically disables the effected processor and brings one of the spare processors online to complete the TMR configuration. The system is designed to initialize and synchronize the spare processor to the two active processors in a procedure that is invisible to the application software that is running in the foreground. This paper presents the design and prototyping of the many-core system. In the prototype system, SEUs are induced using a push button switch while hardware failures are created using a graphical user interface (GUI) running on a PC. The GUI indicates which processors are active, potential spares, or have undergone a hard failure and cannot be used in the future. A user can induce soft and hard failures arbitrarily to monitor the system's ability to recover from potential radiation strikes. The Xilinx *ChipScope* logic analyzer tool is used to observe the system operation as it recovers from soft and hard failures.





Many-core system overview showing the 64-uP block diagram (left) and the GUI to induce hard failures (right).