NOVEL DIE-TO-DIE COAXIAL INTERCONNECT SYSTEM FOR USE IN SYSTEM-IN-PACKAGE APPLICATIONS

by

Christopher Michael McIntosh

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Approved for the Department of Electrical and Computer Engineering

Dr. Robert C. Maher

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ABSTRACT

The electrical parasitics of traditional integrated circuit (IC) packaging methods are a known bottleneck to overall system performance. The parasitic inductance and capacitance of traditional package interconnect such as wire bonds, create noise sources which ultimately limit the speed at which a digital system can run. Recent advances in package interconnect have reduced these parasitics by moving to a System-in-Package (SiP) approach. In SiP, multiple IC dies are connect directly to each other and encapsulated within the same package. This improves performance by eliminating the need for board-level interconnect.

While SiP has made significant progress in reducing the interconnect parasitics, IC dies are still connected using traditional methods such as wire bonds. The unshielded nature of the wire bond leads to noise sources such as coupling, simultaneous switching noise, and reflections. This thesis presents a new interconnect methodology which aims at improving the signaling speeds between dies within SiP.

This new system uses a miniature coaxial cable that connects to on-chip coplanar waveguides on a silicon substrate. The coaxial-to-coplanar transition is accomplished using an anisotropic etch along the perimeter of the silicon substrate. This approach provides the electrical and mechanical mating of the on and off chip conductors. This system yields a fully shielded, matched impedance signal path in addition to a low impedance return path. This approach shows reduction of the three main sources of electrical noise in SiP and leads to a significant improvement in system performance.

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INTRODUCTION

Currently in today's integrated circuit market, there is a significant performance gap between on-chip performance and off-chip communication. This performance gap is an important area of interest when attempting to increase the computation power of a digital system. The off-chip package interconnect parasitics are a major contributor to this problem. The off-chip parasitics are due to the physical geometries of the structures that connect system-level signals to the IC substrate. Current packaging methods use wire bonding, flip chip bumping, lead frames, and ball grid arrays to connect external lines to the chip. These methods have significant parasitic inductance and capacitance which cause a bottleneck in performance when the entire system is analyzed.

The parasitic inductance and capacitance of off-chip interconnect causes electrical noise to be introduced into the system causing the performance problem. The noise is generated by signal cross-talk, inductive return path, and impedance discontinuities. To increase the performance of off-chip interconnect, elimination of parasitic capacitance and inductance on critical signals is important. To eliminate these parasitics caused by external packaging, the use of coaxial cables being mounted directly on-chip is explored. By launching the signal onto the IC substrate in the described method, current packaging limitations can be overcome. Coaxial cable launching of critical lines is a way of selectively avoiding traditional packaging interconnect problems. The critical paths selected are high speed signal lines. Non-critical, low speed signals, power, and ground lines continue to use traditional connection methods. This thesis presents the development of a coaxial-to-coplanar interconnect methodology for use on high speed signal lines. Figure 1.1 on the following page shows a 3 Dimensional(3-D) rendering of this system using a miniature coaxial cable to connect two dies together

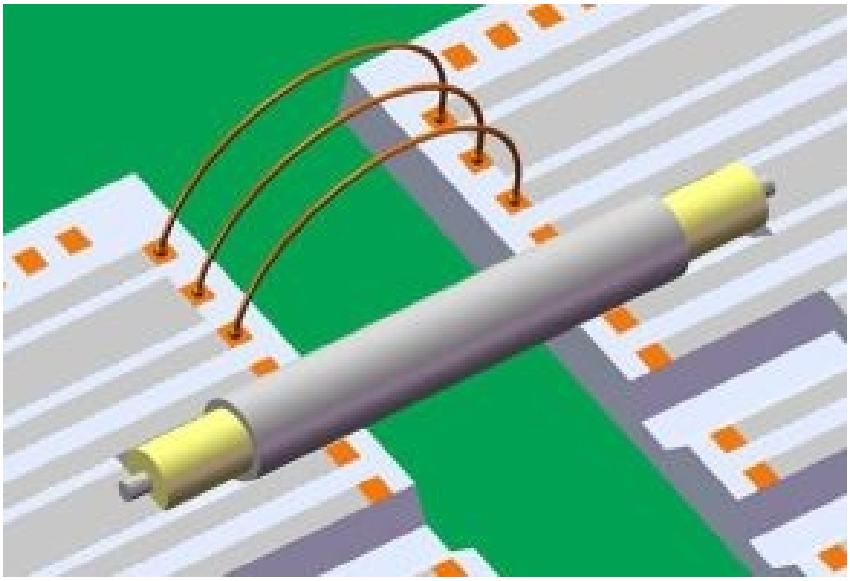


Figure 1.1: Shows 3 dimensional of how two dies could be connected by both wire bonds and coaxial cable.

while still employing wire bonds on non-critial nets. By using the coax cable launch methodology, all three major noise sources in SiP (crosstalk, SSN, and reflections) can be reduced[2]. Coaxial cable has two important features that make it applicable to high speed communication. These are the controlled impedance of the cable and its shielded structure.

To create the off-chip coaxial to coplanar launch, a combination of Microelectromechanical System (MEMS) and Complementary Metal Oxide Semiconductor (CMOS) fabrication techniques are employed. First, a trench is etched onto the IC substrate using a wet etch technique. Then, a controlled impedance, coplanar transmission line is fabricated on the outer metal layer of the IC. The coaxial cable is placed within the trench and secured in place using conductive epoxy. By securing the cable with epoxy, this also achieves an electrical connection for the return path between the outer traces of the coplanar waveguide and the outer shield of the cable. The cable's center conductor is connected directly to the center signal trace of the coplanar transmission

line. Both the on-chip coplanar transmission line and coax cable are designed for the same impedance and to operate at microwave frequencies. The process sequence is shown in Figure 4.2 and discussed in greater detail in Chapter 4.

This paper describes the design and implementation of a system which uses coaxial cable as a chip-to-chip transmission line interconnect for system-in-package. This paper details the steps involved in fabricating working test structures and the design issues that have arose regarding the project. It includes data gathered from fabricated test structures and the evaluation of replacing wire bonds with coaxial cable. The fabrication data shows the performance and efficiency of a coaxial cable launch. Each test chip includes the traditional wire bond interconnect in addition to the purposed coaxial cable launch in order to compare and contrast the performance of each method.

This work demonstrates that a coaxial cable chip-to-chip interconnect system can reduce reflections by 76% over a traditional wire bond approach when stimulated with a 35ps voltage step. The methodology presented in this thesis is ideal for deployment on select high-speed lines within SiP applications.

MOTIVATION

Noise Sources in IC Packaging

Typical package interconnect structures such as wire bonds can cause performance problems within the system[3]. These problems include signal crosstalk, simultaneous switching noise (SSN) and reflections from impedance mismatches. These performance problems arise from the parasitic inductance and capacitance of the interconnect, which ultimately limits the speed and bandwidth of the system. System-in-Package (SiP) was developed as a way to increase functionality and reduce the overall layout footprint of a package[4, 5]. SiP can achieve higher functionality than separately packaged systems by incorporating them together on the same package. By using a single package as opposed to individual packages, the reliance on board-level communication interconnect between the separate systems can be reduced. The most common SiP interconnect in use today is the wire bond.

The use of a traditional, unshielded interconnect such as a wire bond, has several electrical drawbacks. The first is the cross-talk between the signal lines. The cross-talk is a result of the unshielded nature of the structures. Equations 2.1 & 2.2 on the next page show the forward and reverse cross-talk coefficients respectably for an unshielded interconnect signal path. These coefficients represent what percentage of an incident signal will be coupled onto a neighboring line. C_L and L_L represent the self capacitance and self inductance of the interconnect system respectably. C_M and L_M represent the mutual capacitance and mutual inductance between adjacent signal lines respectably. Vel represents the propagation velocity of the signal[6]. These equations show the dependence the signal cross-talk has on the magnitude of the mutual capacitance and inductance.

$$k_f = \frac{1}{2 * vel} * [\frac{C_M}{C_L} - \frac{L_M}{L_L}] \tag{2.1}$$

$$k_b = \frac{1}{4} * [\frac{C_M}{C_L} + \frac{L_M}{L_L}] \tag{2.2}$$

The self inductance of the interconnect return path is another source of noise. Interconnect structures with high geometric aspect ratios (such as wire bonds) tend to have a higher self inductance than other forms of interconnect. This inductive nature of an interconnect such as a wire bond becomes a problem when the return current of multiple signal nets returns through a single interconnect. The voltage noise that is created by the return current is commonly referred to as simultaneous switching noise (SSN)[7, 6]. Equation 2.3 gives the magnitude of this voltage bounce that occurs due to an inductive return path. In this equation, N signifies the number of signals that share a common return path, L_r is the interconnect self inductance of the return path, t_{rise} is the 10-90% signal rise time, and Z_0 is the characteristic impedance of the system. This equation shows that SSN is directly related to both the inductance of the return path and the number of signal lines sharing that path.

$$V_{bc} = N * L_r * \frac{dI_{sig}}{dt} = N * L_r * \frac{0.8 * V_{sig}}{T_{rise} * Z_0} \tag{2.3}$$

The third source of noise in the package is generated from the reflected energy due to impedance mismatches within the system. A large portion of the impedance discontinuities occur at the package interconnect transitions. These impedance discontinuities are generated by fluctuations in the capacitance or inductance due to the changes in geometries of the interconnect structures. The capacitance and inductance

of the interconnect are related to the structures characteristic impedance (Z_0), which can be seen in equation 2.4[6, 8]. The transmission line looses are shown as $R\&G$ within equation 2.4. The characteristic impedance is a function of frequency.

$$Z_L = \sqrt{\frac{R + jwL_L}{G + jwC_L}} \tag{2.4}$$

As the signal propagates down a transmission line with an impedance of Z_0, (typically 50 Ω), it reaches the package interconnect which has an impedance of Z_L. Z_L has a relatively higher impedance compared to Z_0 due to the interconnects inductive properties. This impedance discontinuity at the interconnect junction causes energy to be reflected. The reflection coefficient, defined as Γ, depends on the difference in impedances between the load and the source impedance. The reflection coefficient, Γ, is given in equation 2.5. Equation 2.5 shows the reflection coefficient between two impedances, where Z_L is the impedance of the package interconnect and Z_0 is the impedance of the system[9].

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.5}$$

Proposed Technique

By selectively using coax cable instead of SiP interconnect (namely wire bonds) on high speed communication lines, the noise problems of IC packaging can be reduced. Avoiding these noise problems can result in a higher performing system. The advantage of using coaxial cable over wire bonds is the reduction in noise caused by the three previously discussed issues (crosstalk, SNN, and reflected energy). The shielded nature of a coaxial cable has several advantages over unshielded interconnect

lines. Crosstalk coefficients are reduced when the mutual capacitance and inductance terms, (C_M & L_M), are lowered by using shielded cable. The shielded cable drives the mutual capacitance and inductance terms between the signal lines to zero. This reduces both the forward and reverse traveling crosstalk.

SSN is reduced when using coaxial cable due to each cable having its own dedicated return path. In equation 2.3, N represents the number of signals sharing a return path. When this number decreases, the voltage bounce is directly reduced. Further, the lower aspect ratio of the coaxial shield results in a lower L_r compared to a wire bond.

The reflection coefficient, Γ, as seen in equation 2.5 depends on impedance discontinuities present in the transmission line. Wire bonds tend to have a higher impedance caused by the wire inductance, which leads to impedance changes along the signal transmission line. Coaxial cable has a matched characteristic impedance along its entire length. This matched impedance of the cable helps to reduce the difference between the system and package impedances, therefore reducing the reflections.

DESIGN OF THE INTERCONNECT SYSTEM

Structure Sizes

The interconnect system is accomplished by using miniature, semi-rigid coaxial cables that interface to on-chip coplanar transmission lines using etched trenches. To accomplish an electrical connection between the cable and the coplanar transmission line, the center conductor of the coaxial cable is exposed. The cable is striped in two places, exposing the center conductor and the inner dielectric. The outer shield of the coaxial cable makes contact with the two outer traces of the on-chip coplanar structure while the center conductor of the cable makes contact with the center trace of the coplanar structure. Figure 3.1 shows the interface trench on the silicon substrate used to hold the cable in place.

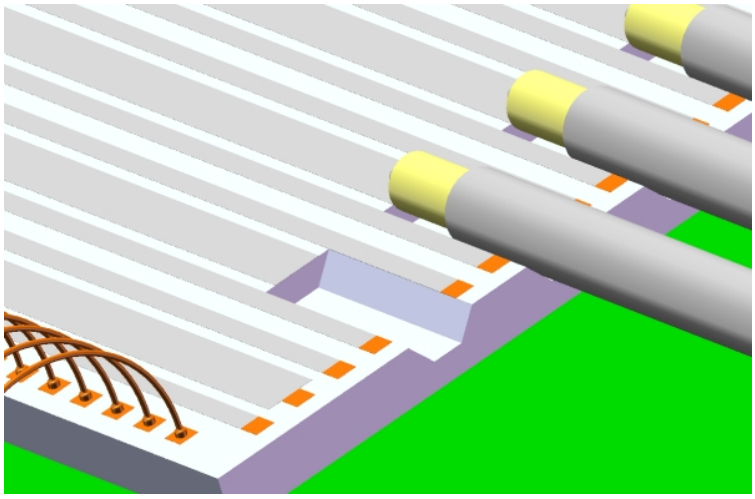


Figure 3.1: Magnified view of the etched transition trenches and coplanar waveguide structures. This figure shows trenches with and without cables.

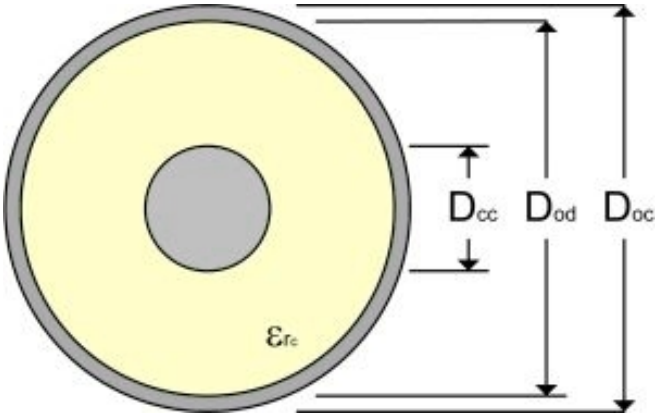
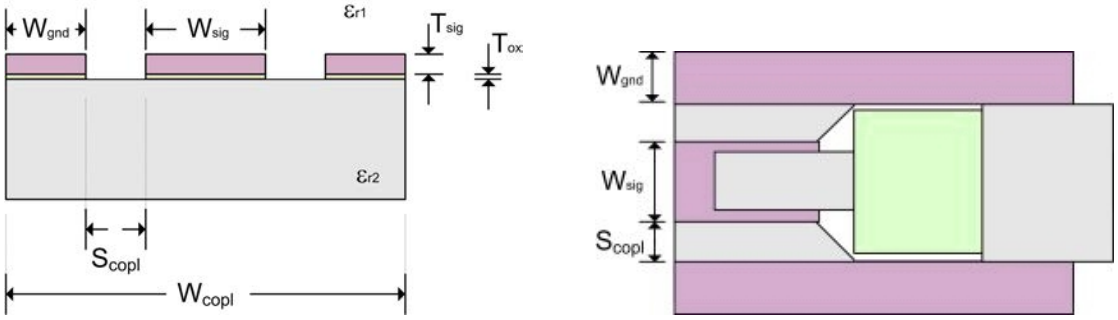


Figure 3.2: Coaxial Cable Dimensions

The key dimensions that drive the design of the interconnect system are from the miniature coaxial cable. The size of the coaxial cable dictates the size of the trench in addition to the dimensions of the coplanar ground spacing. The key cable dimensions are shown in Figure 3.2.

A coplanar transmission line is created using three traces of metal residing on the same plane on the outer layer of the silicon substrate. The inner trace carries the signal wave while the outer two traces carry the return currents. The geometry and materials of the coplanar transmission line determines its characteristic impedance (Z_0). The width and thickness of the traces (W_{sig}, W_{gnd}, T_{sig}), the spacing between the traces (S_{copl}), and the materials of the structure (ϵ_{r1}, ϵ_{r2}) are the major deciding factors of the transmission lines Z_o[8, 10, 11]. Figure 3.3(a) shows a cross-section of a coplanar transmission line. When constructing a coplanar structure on doped silicon, a thin layer of Silicon Oxide (SiO_2) is inserted between the semiconductor substrate and the metal to provide a layer of adhesion and insulation (Tox). The impedance of the coplanar structure is designed match the impedance of the coaxial cable to provide a fully matched system.



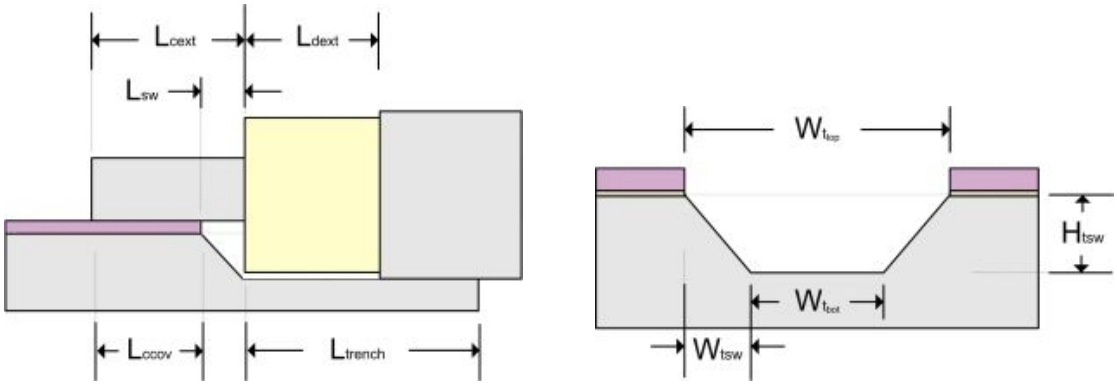
(a) Cross-section of a coplanar waveguide structure showing the critical dimensions.

(b) Coplanar waveguide structure from above.

Figure 3.3: The Coplanar transmission line dimensions

A trench is formed within the coplanar structure such that the coaxial cable can be inserted and make electrical contact between the signal and ground conductors for both the coplanar and coaxial structures. The trench performs both electrical and mechanical functionality. It allows the cable to make electrical contact with the traces while giving the system structural stability. The return path is accomplished by etching the trench within the coplanar structure but without removing any of the metal forming the two outer return traces. When the coaxial cable is laid in the trench, its outer shield will be adjacent to the ground lines of the coplanar transmission line. Figure 3.3(b) shows the outer conductor of the cable resting directly next to the ground traces of the CPW once the cable has been set into the trench.

The signal path is formed by exposing the center conductor of the coaxial cable. When the coaxial cable is inserted into the trench, the center conductor will come to rest on top of the signal trace of the coplanar structure. The size of the coplanar transmission line (W_{sig}, W_{gnd}, and T_{sig}) and the size of the trench (W_{ttop}, W_{tbot}, H_{tsw}, and W_{tsw}) are both designed to achieve a matched impedance and a proper alignment of the coplanar to coaxial transition. Figure 3.4 shows the critical dimensions of the trench and the cable insertion.



(a) trench and cable, shows stripping lengths

(b) showing trench dimensions from front view

Figure 3.4: Trench and transition dimensions

Before the coaxial cable can be inserted into the trench, the cable needs to be stripped in stages. The transition lengths shows how much of the cable will be embedded into the silicon substrate. Several different transition lengths are defined Figure 3.4(a). The center conductor will extend out of the dielectric with a length of L_{cext}. Minimizing the length of the exposed center conductor helps to reduce undesired affects such as crosstalk. The length the cable's dielectric is exposed from the outer metal conductor,L_{dext}, should also be minimized to help avoid impedance reflections. Adjacent coplanar-to-coaxial structures can be placed on a pitch defined by S_{ss}, as shown in Figure 3.5. Figure 3.6 shows 3 dimensional images of the interconnect system in several variations of SiP including adjacently placed and stacked die configurations.

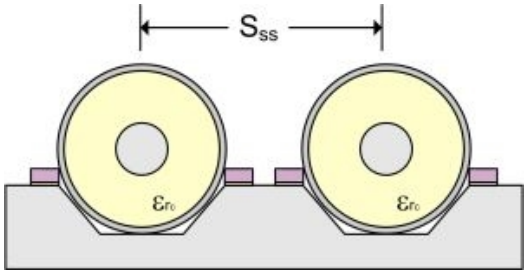
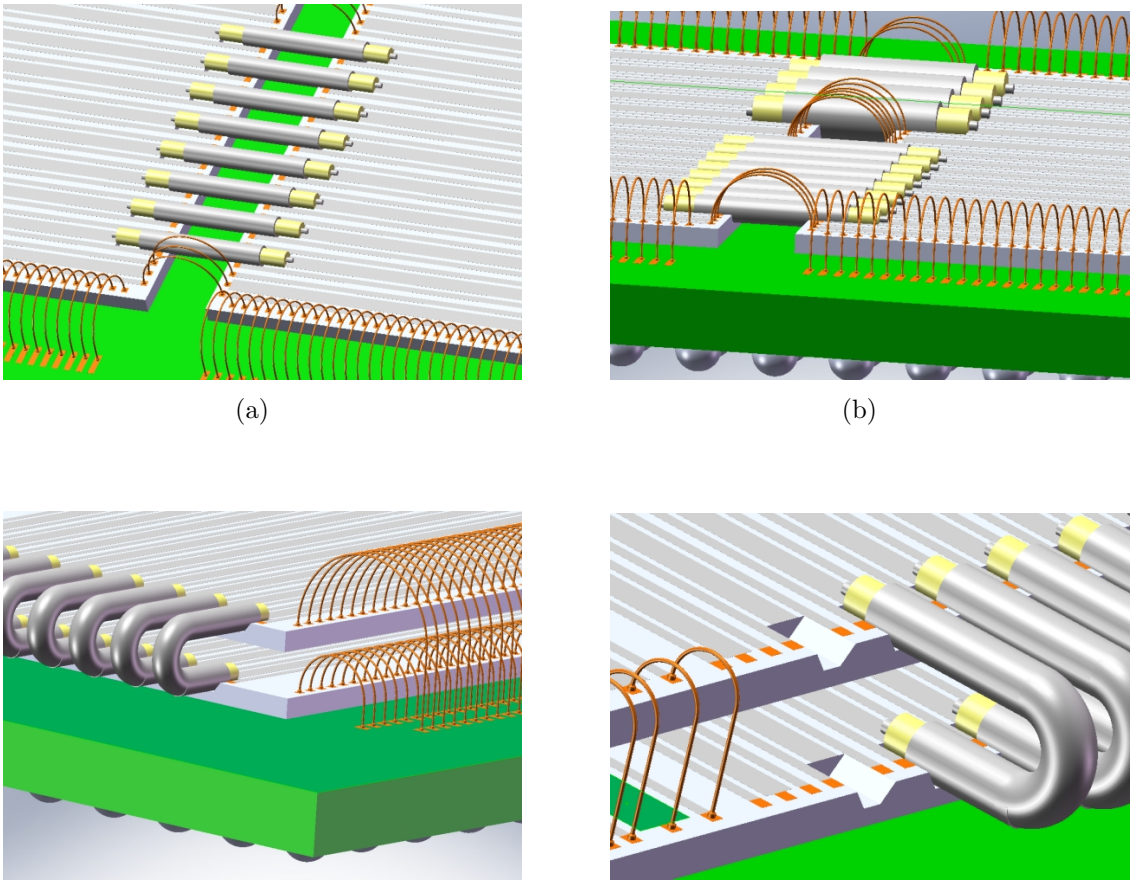


Figure 3.5: Dimension of two side by side coaxial cables mounted within separate trenches.



(a) (b)

(c) (d)

Figure 3.6: Three Dimensional renderings of coaxial cable interconnect used in different SiP applications.

FABRICATION OF THE INTERCONNECT SYSTEM

The selection of the coaxial cable dictates the fabricated structure sizes and procedure. Two different sizes of miniature coaxial cable were evaluated from $Micro-Coax^{®}$[12]. Both cables consist of a silver-plated, copper clad steel (SPCW) center conductor covered with an insulating layer of Polytetrafluoroethylene (PTFE). The outer conductor is created with a solid tubular layer of copper. The cables selected were the UT-013 and UT-020, both are semi-rigid, with a characteristic impedance of 50Ω. The UT-020 and UT-013 have outer diameters of 584μm and 330μm respectively. At this time, they are the smallest semi-rigid cables available from $Micro-Coax^{®}$[12]. Table 4.1 shows the dimensions of the coplanar transmission line and trench structures used based on the two cable sizes.

Table 4.1: Coplanar, Trench, and Cable Dimensions[12]

Region	Parameter	Coaxial Cable	
		UT-013 [μm]	UT-20 [μm]
Coplanar	T_{sig}	1	1
	T_{ox}	0.8	0.8
	W_{sig}	239	446
	W_{gnd}	100	100
	S_{copl}	55	90
	W_{copl}	549	826
	S_{ss}	634	916
Coaxial	D_{oc}	330	584
	D_{od}	254	419
	D_{cc}	79	127
Trench	W_{ttop}	349	626
	W_{tbot}	150	228
	W_{tsw}	100	199
	H_{tsw}	126	229
Transition	L_{trench}	900	801
	L_{dext}	500	500
	L_{sw}	100	199
	L_{cext}	500	500
	L_{ccov}	401	301

Mask Design

To make the coaxial cable transition in silicon, a process was designed to pattern both the coplanar structures and the trench etching locations. This methodology was developed and followed to fabricate working test structures using Montana Micro-Fabrication Facility (MMF) located at Montana State University, Bozeman Montana. The masks used to pattern the features on the silicon substrate were designed using the $Cadence^{®ICDesignSystem}$ and built by the University Of Minnesota Nanofabrication Center.

The fabrication process comprised of two masks. The first mask defined the etching regions used to create the trenches. The second mask defined the coplanar structures on the outer metal layer. The masks were applied in a specific order. If the metal mask had been first, the silicon etchant would have attacked the metal traces. To prevent this from happening, the silicon etching mask was chosen to be processed first followed by the metal mask. The layout of the mask design for a test die can be seen in Figure 4.1. This figure shows the two layers of a single die. The blue represents the silicon etching regions and red areas represent the metal regions. The test circuits created consisted of a wafer which had 32 identical dies separated by 200 μm of isolation. A die was 12.5 mm on each side.

The silicon etching regions extend from die to die. These regions extend through the isolation regions which were subsequently separated using wafer dicing. Each test die has several different structures. There are three types of coplanar waveguides, wire bonding pads, two sizes of trench lengths, and metal text. See Appendix A for more figures on the masks designs, die and wafer layouts.

There were three types of coplanar transmission line constructed on the test chip: (1)wire bond only, (2)small, and (3)large. The wire bond only coplanar waveguide

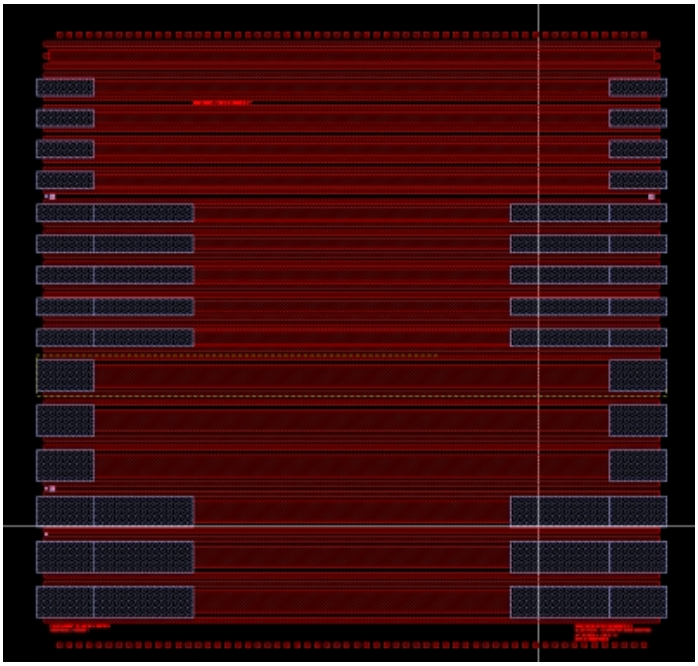


Figure 4.1: Cadence layout of a single die.

test structure has no trench for a cable to be embedded into. There is one of this CPW type per die and it is located on the very top as shown in Figure 4.1. This structure is used for testing wire bonding onto the CPW and using it as a reference for wire bond pad size. This test structure allows the signal trace to run to the edge of the die for easy wire bonding access. The dimensions of the wire bond only coplanar waveguide are based on the small CPW structure.

The second type of CPW on-chip is the small interconnect version. The small CPW's occupy the upper half of the die and are design to accept the UT-013 $Micro-Coax$® cable. The signal trace of the small CPW has a width measuring 239 μm. The third type of CPW is the large structure which occupies the bottom half of the die and is designed to accept the larger UT-020 coax cable. This CPW has the largest trace width of the three CPW types. The signal trace has a width measuring 446 μm. Both the large and small CPW structures have a ground traces width of 100

μm. The large CPW were mostly used in the testing due to their larger size making it simpler to work with. The dimensions of the coplanar waveguides can be seen in Table 4.1.

For both the large and small CPW, there are two different trench transition lengths. The shorter trench measures 1 mm and the longer trench measure 3 mm. Both measurements are from the end of die measured towards the center. Having more than one trench size gives more flexibility when attaching the cable, and more test data to compare.

Table 4.1 can be used to calculate the incremental area impact of our approach when compared to a typical wire bonded system. A wire bonded system using coplanar waveguide transmission lines requires 3 bond pads. The perimeter length required for this arrangement consists of the widths of the 3 wire bond pads (W_{pad}) plus the spacing between the pads (S_{pad}). Assuming a 100 μm x 100 μm bond pad (W_{pad}=100 μm) with pad spacing of 100 μm (S_{pad}=100 μm), the total distance required is [3*W_{pad} + 2*S_{pad}] = 500 μm along the perimeter. In the coaxial cable approach, when using the UT-013 coaxial cable the total distance needed consists of the width of the top of the trench (W_{ttop}=349 μm) plus the width of the two ground pads (W_{pad}=100 μm). This gives a total perimeter length of [W_{ttop} + 2*W_{pad}] = 549 μm per signal. Our approach requires only a 9.8% increase in perimeter to accommodate the coplanar-to-coaxial transition.

Trench Fabrication

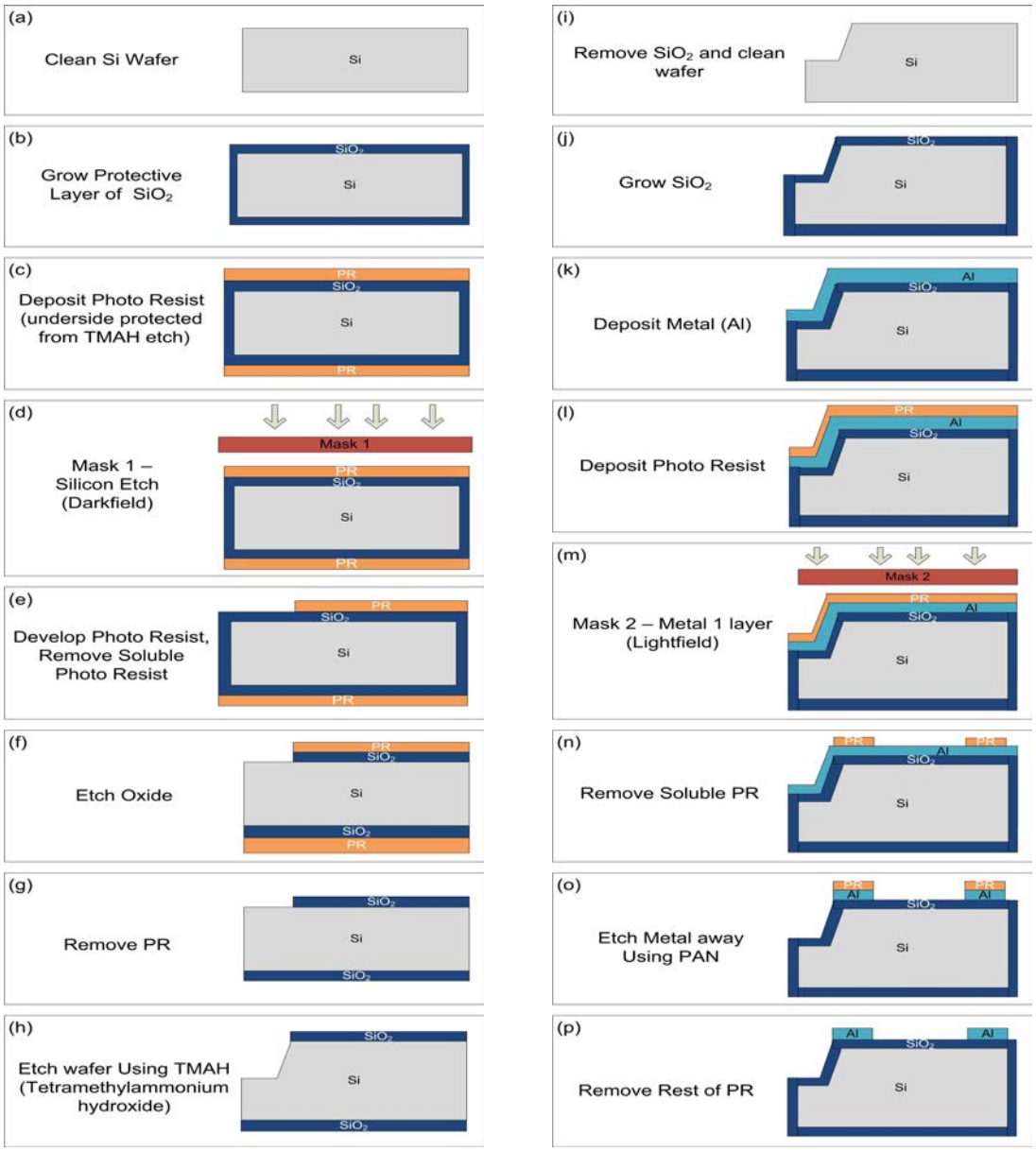
All the wafer processing was done using the Montana Micro-Fabrication Facility (MMF), with the exception of the die cutting. Using a two set mask, several different coplanar waveguide structures were fabricated. The test structures were built following the fabrication steps seen in Figure 4.2.

The silicon wafers used in this project were 100 mm in size and doped to be P-type. These wafers were Boron doped at a concentration level of $1.5e^{16}cm^{-3}$ to $1.2e^{20}cm^{-3}$. The wafers were university grade and purchased from $UniversityWafer$®[13]. The wafer parameters can be seen in table 4.2.

The first processing step was to clean the wafers. Cleaning the wafers was done using an RCA clean. The RCA clean consists of three process steps in which three different chemical solutions are used. The first step is a Piranha solution which is a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) at a concentration of 3:1 H_2O_2:H_2SO_4. This removes any organic material on the wafer. The Piranha solution causes a layer of oxide to form over the surface caused by a chemical reaction. To remove the oxide from the wafer surface, hydrofluoric acid (HF) is applied as the second step. The third cleaning solution consists of Hydrochloric acid (HCl). This is used to remove any ions from the surface of the wafer. This solution has a concentration of 6:1:1 of H2O:H2O2:HCl. The first and third cleaning solutions are heated to 80^oC.

Table 4.2: The Wafer parameters[13, 14, 15].

Resistivity	ρ	1 - 0.001 $\Omega - cm$
Conductivity	σ	1 - 1000 S/cm
Concentration		$1.2e^{20}$ - $1.5e^{16}cm^{-3}$
Mobility	μ_h	417 - 49.5 $cm^2/(Vs)$
Orientation		$< 100 >$



(a) (b)

Figure 4.2: The processing steps in order.

Before the trenches could be etched, a SiO_2 layer was grown. This SiO_2 layer was used as a masking layer to protect areas of the wafer from being etched undesirably. The SiO_2 is grown in a wet oxide furnace at a temperature of 1050^oC and for a length of 4 hours. Measuring the thickness of the oxide to be on average, 8900 $\mathring{A}$. The thickness of the oxide needed to be thick due to the etchants used in the following steps, which will slowly attack the oxide.

The photoresist (PR) used in the project was Shipley 1813, which is a positive photoresist. For the first processing mask, photoresist was applied to both sides of the wafer. This was to ensure the SiO_2 on the backside of the wafer was protected during the oxide mask etching. If the oxide on the backside of the wafer had been removed, the backside would not have been protected from the etchant used to create the silicon trenches. When the wafer was placed into the silicon etchant bath, it would have etched the entire backside of the wafer at the same rate as the front. After the wafer was soft baked at 115^oC for 90 seconds to harden the PR, the wafer was exposed for 4.5 seconds at an UV intensity of $30mW/cm^2$ and a UV does of about 135 J/cm^2. The developer used was the MF316 at a time of 45 seconds.

The SiO_2 mask layer was etched using a buffered oxide etch (BOE). This contains hydrofluoric acid (HF) and a buffing agent, ammonium fluoride (NH_4F). The buffered oxide etch is used instead of diluted hydrofluoric acid because as the SiO_2 begins dissolving into the solution, the concentration of free fluoride atoms are removed from the solution. The fluoride atoms have recombined with the silicon atoms causing the etch rates to decrease with time. The buffered oxide etch solution used was 6:1 and done at room temperature, 22^oC. The BOE attacked the SiO_2 at a rate of 600 $\mathring{A}/min$, under these conditions.

The etching of the trenches was done with Tetramethylammonium hydroxide (TMAH). TMAH is a silicon anisotropic etchant, meaning it is directional and does

not etch at the same speed in all directions. It has high selectability of Si to SiO_2, on the order of 1:100 - 1:1000[16, 17], As appose to other anisotropic etchants such as KOH, where the selectability is around the order of 1:100 [16, 17]. High selectability was required due to the depth of the trenches needed with respect to the masking layer thickness. Anisotropic etchants are directionally dependent causing an angle to form in the direction of etching. Using $< 100 >$ crystal oriented wafer, this angle becomes 54.7 degrees[15]. To achieve the greatest structural support for the cable, the trench needed to be sightly larger than the cables diameter. The trench width was increased to take the etching angle into account. After taking the trench's inward sloping angle into affect, the width of each trench was increased by 12 and 42 μm for the small and large CPW structures respectively. This increase in the trench width caused the cable to fit correctly in the trench, the final widths of the trenches are seen in table 4.1.

A fabricated trench can be seen in Figure 4.3. This trench has a depth of 120 μm and is used for the larger cable. The darker regions along the outer edge of the trench are the $< 111 >$ crystal planes of the trench. Depending on the silicon crystal lattice orientation, and the etchant chemical used, the silicon etch rates will differ [16, 15]. Using 25% TMAH at 80 °C, the silicon etch rates were 8 μm/Hr. The Si to SiO_2 etch ratio was greater than 500:1. The processing steps for silicon trench formation can be seen in Figure 4.2(a) - 4.2(h).

Figure 4.3 also shows thermal buckling of SiO_2. When silicon dioxide is thermally grown under high temperatures, compressive stress occurs as the oxide cools from this high temperature. The oxide compression is due to the difference between the coefficients of thermal expansion of the two materials. As the trenches are etched away, the compressive stress in the SiO_2 is relieved. Relieving this stress allows the

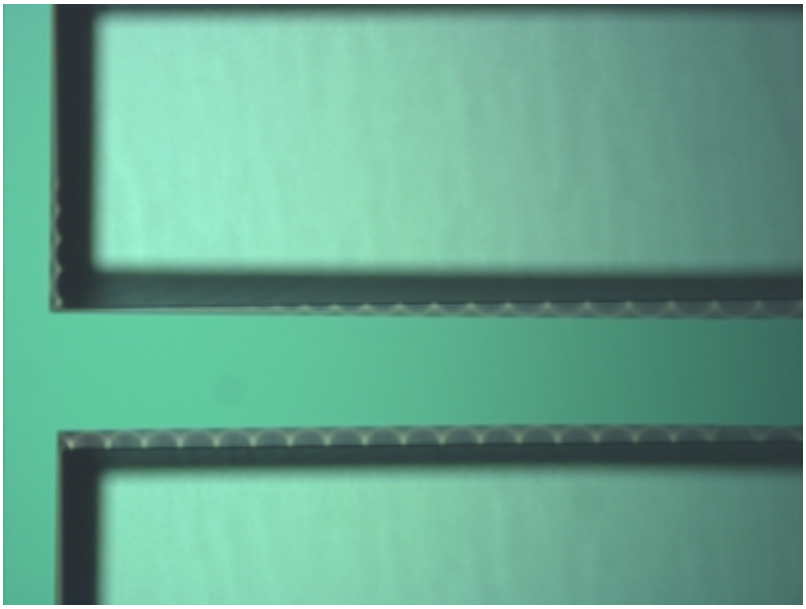


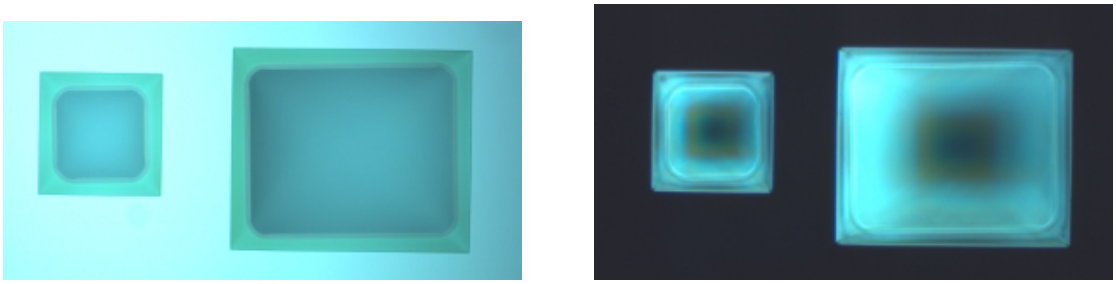
Figure 4.3: Large trench etched into silicon 120 μm deep

SiO_2 film to deform and bend. The thin film deformation is seen in the Figure as wavy fringes[18, 19, 20].

Alignment marks were needed in order to align the second mask to the first mask. The method used was a typical cross inside a rectangular box. The alignment marks can be seen in Figure 4.4. In this figure, you can see the inverted pyramid structure that is created due to the THAH etching angles. They show up as different shades of gray depending on depth.

Coplanar WaveGuide Fabrication

A layer of SiO_2 was grown over the entire wafer before any metal was deposited on the silicon. The oxide was created using a wet oxidation furnace at a temperature of 1050^oC for 3.5 hours. This layer of oxide, measured to be 8000 $\mathring{A}$, is used as a thin insulating dielectric layer between the substrate and the traces. SiO_2 has



(a) Lightfield image of alignment, misalignment seen marks

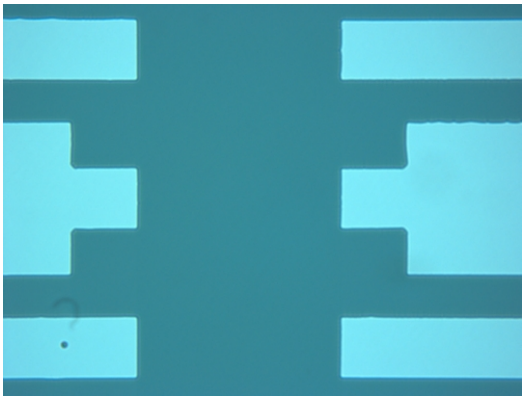
(b) Darkfield image of alignment marks, inverted pyramid shown p

Figure 4.4: Alignment marks showing the silicon crystal plane.

a relative permittivity (ϵ_r) of 3.97 and a loss tangent, δ, equal to 0.01[21, 22, 23]. The coplanar waveguides were fabricated using the second mask. Aluminium was used to create the coplanar waveguide traces. The aluminium was deposited using evaporative techniques using a MODU-LAB PVD system. The thickness of the metal was measured at 0.45μm using a AMBIOS Stylus Profilometer.

Once the aluminium was evaporated onto the wafer, the metal traces and text were created by etching away the rest of the metal. Shipley 1813 positive photoresist was once again used. Due to the depth of the trenches, more photoresist was used in order to cover the entire wafer. The spinner speed was also decreased to help reduce streaking while the spinning time was increased. Only one side of the wafer needed PR applied to it this time. After a 90 second soft bake at 115 ^oC to harden the PR, it was than exposed at the same settings as before. The wafer was developed using the same developer and process steps as before. The aluminium was etched using Phosphoric-Acetic-Nitric Acids (PAN etch 16:1:1:2 $H_3PO_4 : CH_3COOH : HNO_3 : H_2O$) at a temperature of 75$^oC$. The etch rate for the PAN etch was 350 $\mathring{A}/min$. Figure 4.5 shows finished etched CPW structure traces.

(a) Two small coplanar waveguides structures.



(b) Two fabricated wire bond only coplanar waveguide structures. The isolation between the adjacent dies can be seen.

Figure 4.5: Shows the details of the coplanar waveguide structures fabricated with aluminium.

Fixture Design

Once the dies had been individually separated from the wafer, a testing procedure was developed. This testing procedure would determine the feasibility of a coaxial cable to coplanar waveguide transition. In order to evaluate the results, both wire bond and coaxial cable data needed to be compared. This would be accomplished by using an external printed circuit board (PCB).

The PCB was used as a test platform to hold the dies securely in place during testing. Once the dies had been secured to the board, a comparison between the wire bond signal propagation and coax cable signal propagation was preformed. The board can be viewed as two separate testing devices. The fist half of the board, (seen as the left side of the board in Figure 4.6 on the next page), is used to test the CPW structures. A single die is placed onto the board. Wire bonds are attach from the on-chip coplanar structure to the wire bond pads on the PCB, which allow the signal to propagate onto and off the die. This data can be used to determine the efficiency

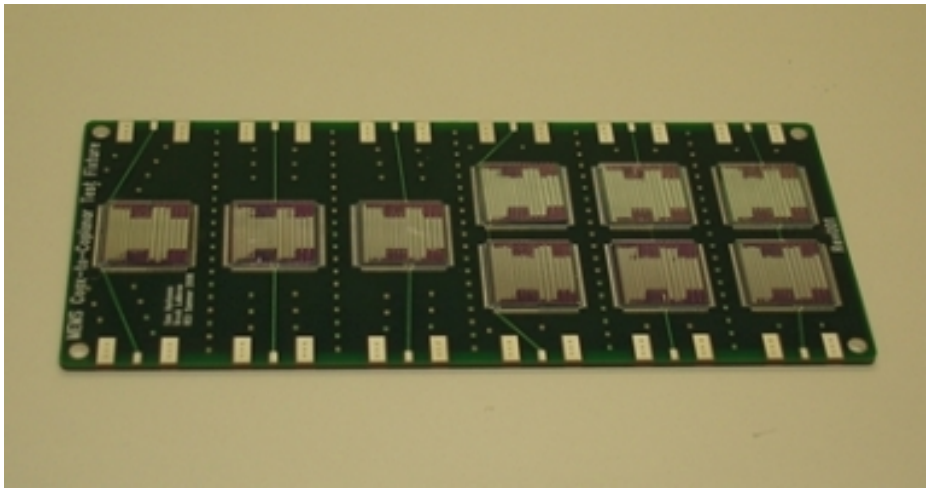


Figure 4.6: Test Fixure for test comparision between wire bond to coax cable launch.

of the CPW. The second part of the board, (seen as the right side of the board in Figure 4.6), is used to compare the results between wire bonds versus coaxial cable in a true die-to-die interconnect test.

The majority of the tests were done using the two adjacently placed dies. For this configuration, two dies are placed adjacent to each other and secured onto the test board. The board has SMA connectors which connect to 50Ω microstrip traces on the PCB. These traces lead to wire bonding pads next to the mounted dies. Wire bonds were then attached from the PCB pads to the bond pads on the dies. The wire bonds on each of the outer dies were used during both the wire bond and coaxial cable test. Only the inner wire bonds were removed during the coaxial test. The test PCB can be seen in Figure 4.6.

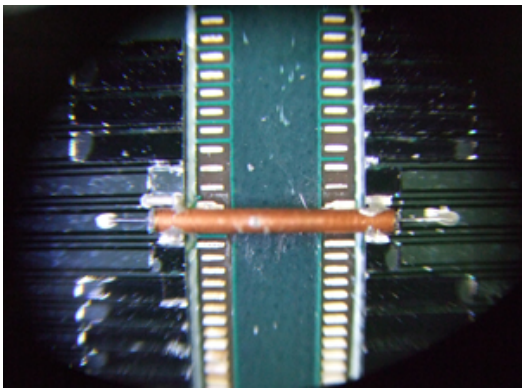
The first test involved testing only wire the bonds as a way for the signal to propagate across the dies. The signal entered the CPW traces through the outer wire bonds near the SMA connectors. Once the signal traveled down a single die to the end, wire bonds would transfer the signal onto another 50Ω trace taking the signal to the next die. The signal would travel through another set of wire bonds onto the

second CPW. After the signal traveled down the second CPW, it would then leave the CPW traces through the fourth and final set of wire bonds onto another 50Ωs microstrip transmission line. This would lead the signal to the end of the test board and exit through another SMA connector. This test data would represent how a traditional system-to-system using a wire bonding would operate. This method uses a total of 12 wire bonds for the signal to propagation down the entire test board. This includes the return currents.

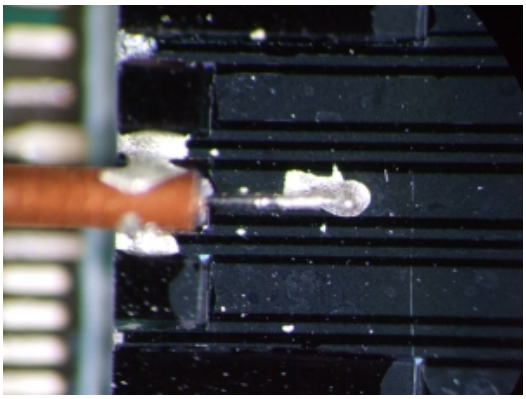
The second test used the coaxial cable to CPW launch method. The outer wire bonds were left intact, allowing the signal to propagate from the SMA connectors onto and off of the same dies as before. The inner wire bonds were removed and replaced with a miniature coaxial cable. By replacing the inner wire bonds with cable, this also removed the need for the 50Ω microstrip transmission line running between the dies. By replacing the inner wire bonds with cable, 6 wire bonds were eliminated. This method can be seen in Figure 4.7(a) on the following page.

Once the inner wire bonds were removed, the cable could be laid into the trenches. The cable was striped using a razor blade leaving about 1 mm of the center conductor showing. Electrically conductive silver epoxy was used to attach the cable to the CPW metal traces. The epoxy used was $EPO-TEK^{®}$ H20E which is a two component 100% solids silver-filled epoxy designed for microelectronic applications. The mixing ratio of the two parts was 1:1. The volume resistivity of H20E is less than 0.0004 Ohm-cm at 23^oC. H20E epoxy has a cure time of 15 minutes at 120^oC or 5 minutes at 150^oC[24]. The cable was attached to the dies by first using a small amount of epoxy within the trenches and then placing the cable on top of the epoxy. The epoxy was fully cured, causing the cable to be held firmly in place while the rest of the connections were made. The return paths of the CPW were connected to the cable's outer shielding using the epoxy. The last connections made were the two center

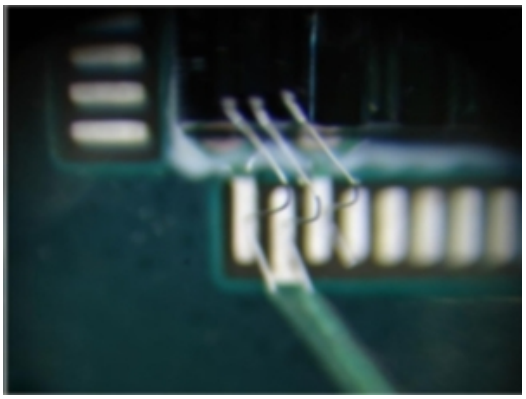
conductors. Due to the trench depth, the center conductors rested directly on top of the signal traces already. Only a small amount of epoxy was required for a connection. A close up image of the cable connections to the coplanar waveguide traces is shown in Figure 4.7.



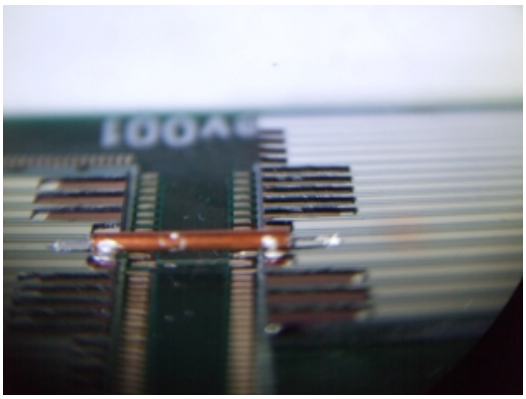
(a) Image shows the coaxial cable connecting the two dies together. The cable replaced the original wire bonds.



(b) Image shows the coaxial cable connections to the CPW for the signal path and return paths



(c) Wire bonds used for the Coplanar waveguide structure.



(d) Coax Cable connecting adjacent dies together.

Figure 4.7: Figures showing Coaxial cable hook up and wire bonds.

CHARACTERIZATION RESULTS

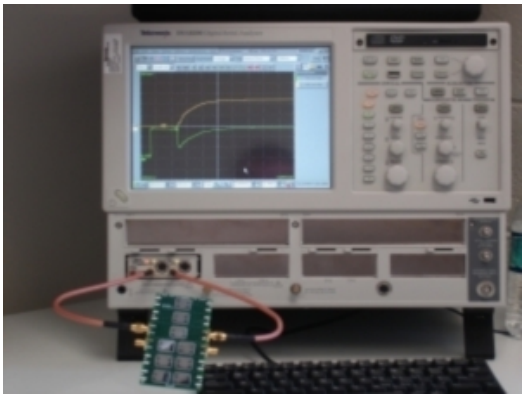
The test fixtures were tested in both the time domain and the frequency domain. For the time domain test, Time Domain Reflectrometry (TDR) and Time Domain Transmission (TDT) was used. This is a commonly used technique for measuring high speed performance of an interconnection system[25]. The TDR is a reflection measurement of the impedance discontinuities. A Tektronix DSA8200 sampling oscilloscope with an 80E04 TDR module was used for the measurements. This setup is capable of stimulating the system with a 35ps voltage step and acquiring a signal with 20GHz of bandwidth. The test setup for the electrical characterization using the TDR and TDT system can be seen in Figure 5.1(a) on the following page.

One consideration about using a TDR system for measurements is the minimum separation between discontinuities. This minimum resolution the scope can resolve is d_{min}, which can be seen in Equation 5.1[25]. In the equation, c is the speed of light, and ϵ_r is the relative dielectric constant. For SiO_2, this value is 3.97. The TDR rise time, t_r, was 35ps for the scope used. Using these values, d_{min} is approximately 1.3mm. This can be a drawback if the physical layout becomes very short. For this project, the spacing between major interconnect discontinuities was greater than 1.3 mm apart, making the TDR data relevant.

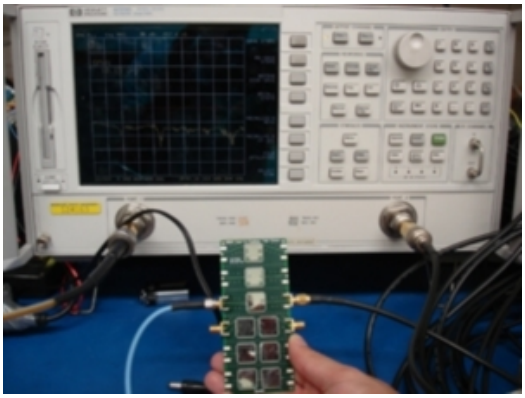
$$t_r = \frac{4 * d_{min} * \sqrt{\epsilon_r}}{c} \tag{5.1}$$

For the frequency domain tests performed on the test fixtures, a Vector Network Analyzer (VNA) was used as well as converting the time domain signals into the frequency domain. The VNA gives S_{11} and S_{21} port data, which are the port losses over a frequency range. The time domain signals were converted to S_{11} and S_{21} port data using the $IConnect$® S-parameters software package from $Tektronix$®[26].

The VNA setup can be seen in Figure 5.1(b). Measurements were taken on both the wire bond setup and the coaxial cable setup. The results were overladed to compare system-to-system performance.



(a) The setup for TDR/TDT Test.



(b) The setup for VNA Test.

Figure 5.1: The setup for the two types of test, The Time Domain and The Frequency Domain.

Time Domain Results

The 35 ps input step used in the TDR and TDT tests can be seen in Figure 5.2 on the following page. Screen shots of the TDR and TDT results from both the wire bond and coaxial cable test fixtures can be seen in Figure 5.3(a) and Figure 5.3(b) on page 30. Where C1 and C2 are the TDR and TDT respectively for the wire bond test and R3 and R4 are the TDR and TDT respectively for the coax cable test. The time division for the scope was set at 2 ns/div. The data and plots were measured using the large CPW structures.

The response of the time domain data shows a very long rise time associated with the signal propagation across the test figure. In general, this resembles a large capacitive load[27, 28]. The large capacitive value is due to the coplanar structure.

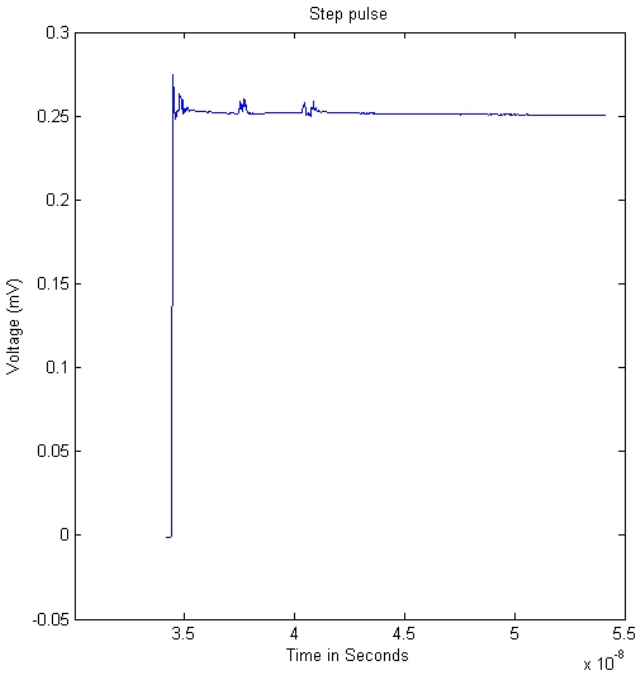
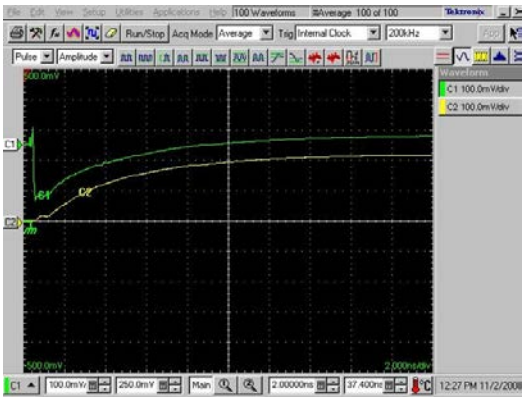


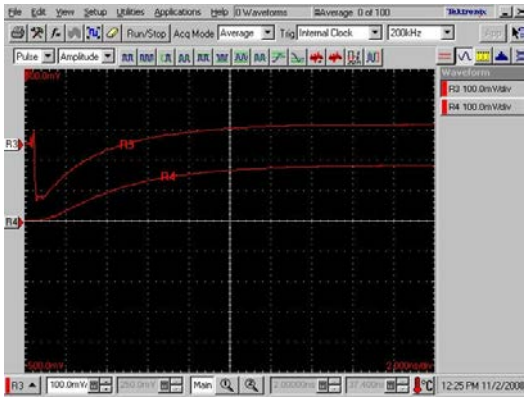
Figure 5.2: The TDR/TDT Gaussian Step.

This capacitance is between the metal coplanar waveguide traces and the doped silicon substrate. A simple capacitor equation can be seen in Equation 5.2. The capacitance value is related to the area, the effective relative permittivity, and the distance between the materials. The ϵ_r for silicon is 11.7 and 3.97 for SiO_2. The area, A, is very large, being the CPW traces occupy most of the length of the substrate. The distance, d, between the metal traces and the substrate are separated by a very thin dielectric layer of SiO_2 with thickness of $8000\mathring{A}$.

$$C = \frac{\epsilon_r * A}{d} \tag{5.2}$$



(a) TDR/TDT results for Wire Bond



(b) TDR/TDT results for Coaxial Cable

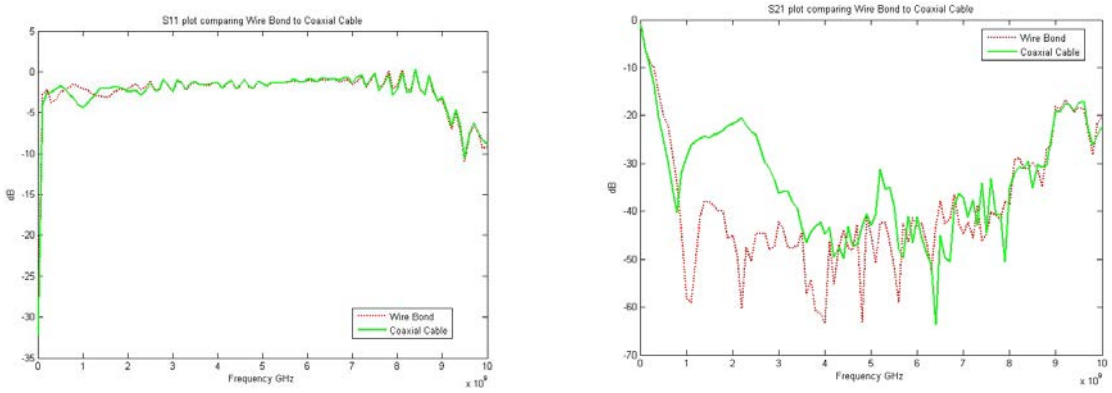
Figure 5.3: The TDR and TDT results for the Wire bond and Coaxial Cable test fixtures.

Frequency Domain Results

This project used heavily doped boron silicon wafers, which leads to a high substrate conductivity. The conductivity of the doped wafers was between 100 - 100000 Siemens/m. With such a low resistivity, losses within the substrate can amount to significant values when operating at microwave frequencies [29]. The S-parameters can be seen in Figure 5.4. Figure 5.4(a) shows the S_{11} reflected power comparing the wire bond and coaxial cable. Figure 5.4(b) shows the S_{21} transmitted power comparing the wire bond and coaxial cable. Both figures use the large CPW structures and are created using $IConnect^{®}$.

In Figure 5.4, the coaxial cable shows similar S_{11} S-parameter reflections compared to the wire bond interconnect. As for the forward transmission coefficient, the coaxial cable interconnect performs as well or better than the wire bond interconnect for S_{21} parameter over all frequencies except between the 6 - 7 GHz mark. The coaxial cable

shows significant improvement in S_{21} parameter over the 1 - 4 GHz frequency range, showing as much as 40 dB improvement at 2.2GHz.



(a) S_{11} S-parameter (b) S_{21} S-parameter

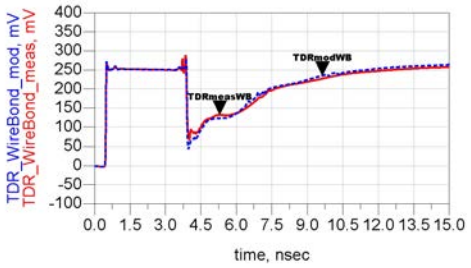
Figure 5.4: The S-parameters of Wire Bond compared to Coaxial Cable.

Equivalent Modeling

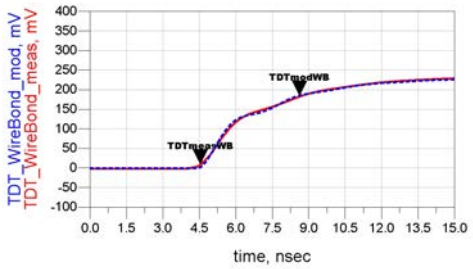
Equivalent circuit models of the entire test system were built using the Advanced Design Systems (ADS) from *Agilent Technologies*®. A Finite Element Analyzer (FEA) called Momentum was used to model the coplanar waveguide structures using a Method of Moments Algorithm. The S-parameters for these structures were then exported from Momentum, and imported into an ADS schematic. Once the coplanar transmission interconnect elements were added into the circuit, simple RLC components and T-line elements were placed into the circuit to model the rest of the system. This process was performed for both the wire bond and coaxial systems. These results were than overladed onto the measured data for correlation. The model data matched the electrical performance of the TDR and TDT measured data. These equivalent circuit models matched the electrical responses of the measured data and can be seen

in Figure 5.5. Figure 5.5 shows the responses for the large cable waveguide which is 10 mm in length[30].

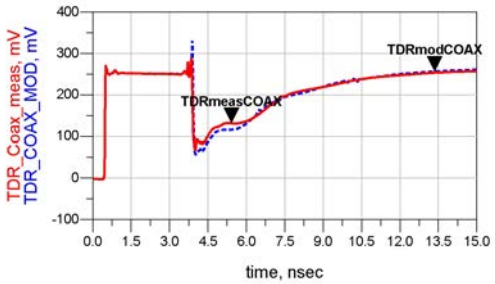
To verify the models were correct and scalable, the short coplanar waveguide structures were measured. The short CPW measured data was then plotted onto the modeled data. The models used were the same as models as the long CPW with the exception of a 6 mm coplanar trace instead of the 10 mm coplanar trace. The models show an excellent correlation to the measured data. This verifies the models of the CPW are correct and can be broken up into smaller CPW segments for simulating other configurations. The correlation between the model and measured data for the short coplanar structures can be seen in Figure 5.6.



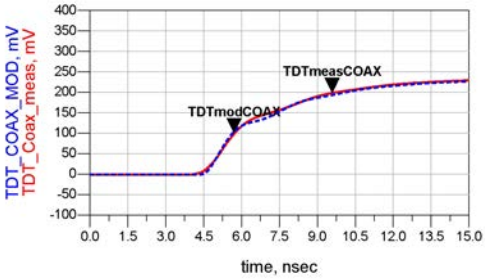
(a) Wire bond TDR



(b) Wire bond TDT

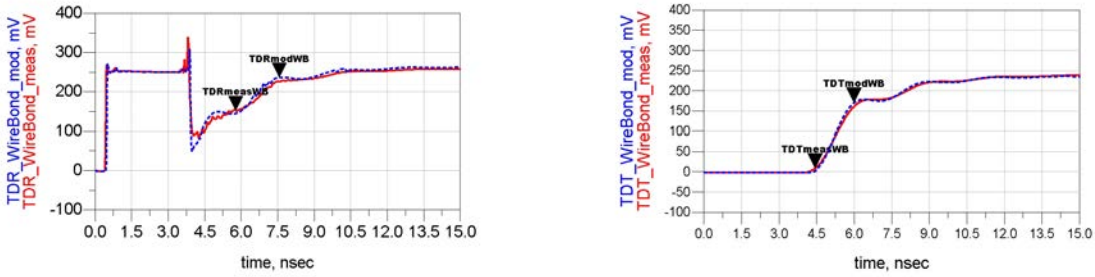


(c) Coax Cable TDR



(d) Coax Cable TDT

Figure 5.5: The TDR and TDT responses for wire bond and coax cable using the long coplanar waveguide structures. Each figure shows both the measured (_MEAS) and model (_MOD) data for the time domain test.



(a) Wire bond TDR

(b) Wire bond TDT

Figure 5.6: The TDR and TDT responses for wire bond using the short coplanar waveguide structures. Shows both the measured (_MEAS) and model (_MOD) data for the time domain test.

Electromagnetic Design System (EMDS) was used to model the coaxial cable transition onto the coplanar structure. EMDS is a three dimensional Finite Element Analysis tool. The coaxial cable used to connect the adjacent dies together was striped in several segments. By stripping the cable in segments, this caused discontinuities along the cable's length due to the varying cross-sections of the new structure. Using EMDS to model the coaxial cable resulted in a more accurate model due to the discontinuities being taken into account. This model gave the impedance and length for each section of the cable. These sections were imported into ADS creating an entire cable model to be used for all the cable simulations. The definition of each cross-section of the cable model are shown in Figure 5.7. The magnitude values of the Z_0 and the transmission lengths (1/Td) for the cable can be seen in Table 5.1 on the next page[1]. Figure 5.8 shows the cross sections of the coaxial cable to coplanar structure.

Table 5.1: Characteristic Impedance and Electrical Length for the coaxial cable broken up into regions[1].

Region	Impedance Mag (Ω)	Transmission Length (ps)
XC1	57.83	9.78
XC2	56.27	5.765
XC3	113.8	0.242
XC4	128.2	0.216
XC5	133.8	0.204
XC6	111.4	1.009
XC7	50.37	2.359
XC8	50.37	20

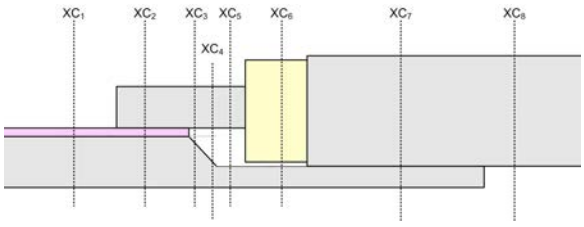


Figure 5.7: Side view of the coaxial cable segments used within the FEA tool. These are defined in table 5.1.

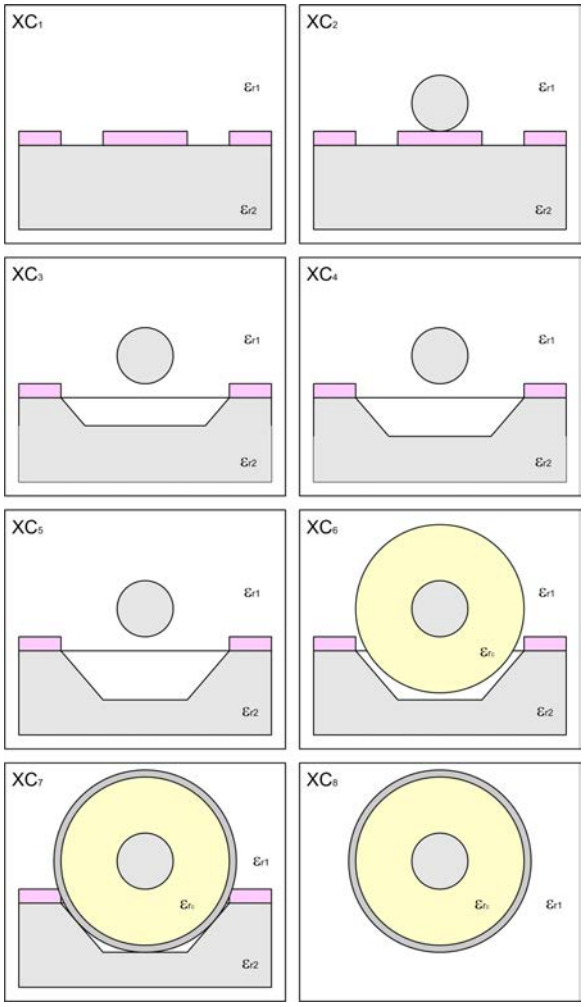


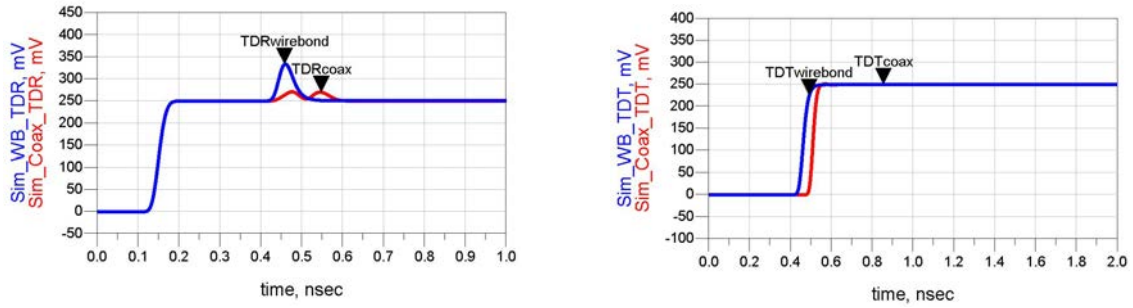
Figure 5.8: Shows the cross sections of the coaxial cable. These sections match up the segments in figure 5.7.

De-embedded Model Performance

Once the models had been correlated to the measurement data, new models were created using only the interconnect portions of the circuit. This created two models: one based on the coax approach and the other based on the wire bond method. This allowed for a true comparison of the electrical performance of the two die-to-die interconnects without the rest of the test step. These models represent two dies connected together using both approaches and allows the performance of only the interconnect to be isolated. These models where then stimulated with an ideal 500 mV Gaussian step with a rise time of 35ps to examine their time domain responses. These results are shown in comparison in Figure 5.9 on the following page.

Figure 5.9(a) shows a TDR simulation comparing the responses of the wire bond system to the coaxial cable interconnect system. The wire bond system resulted in reflections of 33% when stimulated with a 35ps voltage step. The coaxial system resulted in reflections of 8%, an improvement of 76%. The reduction in reflected energy in the coaxial interconnect is due to the elimination of impedance discontinuities caused by the inductive wire bonds.

Figure 5.9(b) shows a TDT simulation which compares the responses of the wire bond system to that of the coaxial interconnect system. The output $10-90\%$ rise time of the coaxial system is modeled at 38ps compared to 49ps for the wire bond, an improvement of 22%. This improvement is also due to the reduction of reflections from the inductive wire bond.



(a) TDR

(b) TDT

Figure 5.9: The TDR and TDT results based on the models from the FEA, comparing both the wire bond system to the coax cable system.

FUTURE IMPROVEMENTS

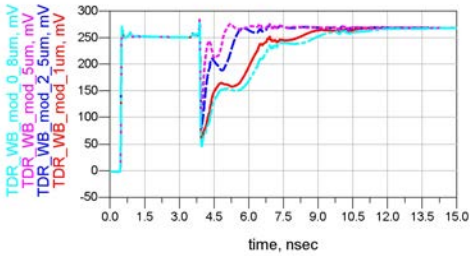
Dielectric Thickness of Coplanar Transmission Lines

As previously mentioned, one of the major causes of the poor signal propagation across the CPW structures was the lossy semiconductor substrate. Due to the very thin dielectric layer of SiO_2 separating the metal traces of the CPW from the substrate, the signal experienced large losses. One solution to this problem is to increase the separation distance of the traces from the substrate. This could be done by increasing the thickness of the dielectric. Using the models that were correlated from the measured data, the FEA tool Momentum was used to change the thickness of SiO_2. Four thickness of SiO_2 were simulated and plotted in Figure 6.1 on the next page.

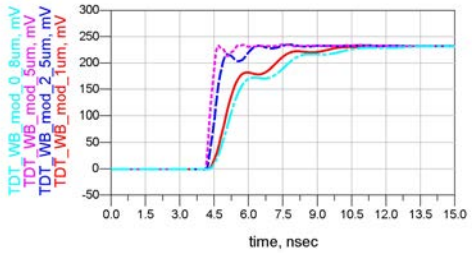
Looking at the data from Figure 6.1, the propagation delay is substantially reduced when the thickness of the oxide is increased. Increasing the oxide thickness by a factor of three made dramatic differences in loss. The 2.5 μm of silicon dioxide in the figure shows remarkable improvement in the signal rise time over the 0.8 μm thick silicon dioxide. The 10-90% rise time improved from 3.45 ns to 660 ps which accounts for an improvement of 80.7%.

Figure 6.2 show the substrate losses of a large coplanar waveguide measuring 1 mm in length. The two figures show the losses associated with the four thickness of SiO_2. The signal losses are extensively reduced as the oxide thickness is increased.

Silicon dioxide thickness depends on a availability of oxygen defusing into the silicon[15]. As the thickness of SiO_2 gets above 1 μm, the time and energy required to produce the oxide increases sharply making it inefficient to produce. SiO_2 would no longer be plausible as the dielectric used between the metal traces and substrate,

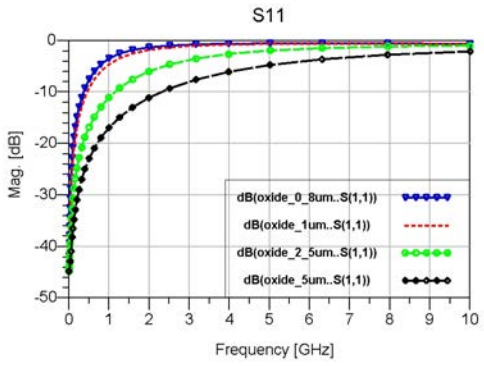


(a) The TDR plot.

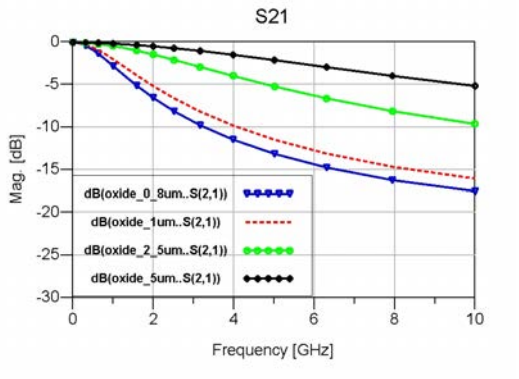


(b) The TDT plot.

Figure 6.1: The TDR and TDT results of different thickness of SiO_2 dielectrics separating the CPW from the substrate. The four oxide thickness are: 0.8μm,1.0μm,2.5μm,5.0μm.



(a) The S_{11} S-parameter Substrate losses



(b) The S_{21} S-parameter Substrate losses

Figure 6.2: The S-parameter Substrate losses for 1mm of coplanar waveguide with different thickness of SiO_2 ranging from 0.8μm,1.0μm,2.5μm,5.0μm.

due to its exponential growth rate.[15]. Another common dielectric used frequently in commercial applications is silicon nitride (Si_3N_4). Since Si_3N_4 uses LPCVD as a means of depositing it, a greater thickness can be achieved than SiO_2[31].

Another possibility to increase the separation distance the metal traces are from the substrate would be to use a thick, etchable dielectric such as benzocyclobutene (BCB). This would allow the traces to be placed at a controlled distance above the lossy substrate. Instead of etching the trenches into the silicon and possibly damaging other structures on-chip, the dielectric would be used as the trench. The metal traces would be fabricated on top of the dielectric. This would allow the cable to still have a trench to fit into while having the CPW structures some distance away from the substrate. Using this method, the dielectric would be used for both separating the traces and as the etched structure.

To reduce the large substrate losses at microwave frequencies, the substrate needs to be altered. There are several acceptable ideologies to achieve this. The first is to used a high-resistive silicon substrate. However, most microwave IC fabrication uses low-cost low resistivity silicon for standard CMOS processing[29]. Another way to achieve a high-resistive substrate would be to use Ion Implantation. Ion Implantation can change the dopant concentration level of the silicon directly beneath the traces. This can be used to change low-resistive silicon into a high-resistive silicon[29, 32, 33].

Processing Improvements

The order of the fabrication steps were done in the specified order to reduce the effects of TMAH etching on aluminium. This lead to the silicon trench etching being performed first, followed by the metal etching. One problem during the photolithography was the trenches caused streaking of the photoresist for the second mask. The streaking lead to errors in etching the aluminium traces of the CPW. To eliminate

the streaks, the order of the masks could be interchanged. To accomplish this, either dry etching of the silicon is need or a different silicon etch solution is required. Using a 5wt.% of TMAH, at least 1.4wt.% dissolved silicon, and 0.4-0.7wt.% of oxidant additive ($(NH_4)_2S_2O_8$), the silicon etchant rate can remain relitively high while protecting the aluminium from undesired etching[34]. Figure 6.3 shows what streaking of the PR can result in when the traces were etched.

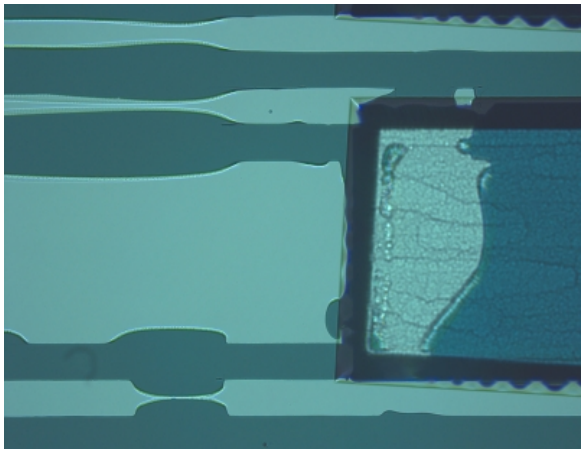


Figure 6.3: Aluminium traces of the coplanar waveguide structure etched incorrectly due to Photoresist streaking.

Assembly

The adhesion of the coaxial cable to the coplanar structure was done using epoxy. This epoxy, when measured, had a significant amount of DC resistance. When the entire coaxial cable system was measured (die-to-die), the resistance was double that of the wire bond system. Therefore, the epoxy alone had an equivalent resistance equal to the entire coplanar structures with wire bonds. This lead to the epoxy being more resistive than previously known. As a result from this resistance, the signal experienced larger losses. Therefore, the adhesion method used to connect the center conductor of the cable to the transmission line needs to be investigated further.

CONCLUSION

Coaxial Cable to Coplanar Waveguide Launch

Using a mixture of CMOS and MEMS fabrication techniques, a novel approach for SiP interconnect was developed and tested. This new interconnect approach was constructed to address the problem of large parasitics of traditional SiP interconnect. To reduce the inductance and capacitance of wire bond interconnect, a coaxial cable to coplanar waveguide launch was fabricated to be used on critical high speed lines. Using a simple two mask set, the process steps were followed to create working test structures that were characterized. By etching trenches into the silicon substrate, a holding cavity for the coaxial cable was created. This allowed for the center conductor of the coaxial cable to rest directly on top of the signal trace of the coplanar waveguide. This trench also allowed the outer conductor of the cable to make electrical contact with the return traces of the CPW. The cable was successfully secured between the dies using conductive silver epoxy.

Testing the die-to-die system was done using a test PCB. The test board created a stable and secure testing platform in which repeatable results were achieved. The wire bond interconnect was compared to the coaxial cable interconnect. These results showed the substrate capacitance was significantly higher than originally predicted. The large rise times of the system shown in Figure 5.5 can be directly attributed towards the large substrate capacitance.

By correlating the models with the measured data, the interconnect portions of the interconnect could be de-embedded from the circuit and modeled separately. The coaxial cable interconnect showed a reduction in reflections and rise time over the

wire bond interconnect. The models showed large improvements over the wire bond interconnect.

The large substrate losses were significant due to the thin separation between the substrate and coplanar traces. The dielectric used for this separation was SiO_2, at a thickness of 0.8μm. To reduce the substrate losses, the thickness of the dielectric needed to be increase, but the SiO_2 layer was approaching the upper limits for practical fabrication. Therefore a different dielectric was needed for this separation.

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APPENDIX A

EXTERNAL DRAWINGS AND SCHEMATICS

Cadence Layouts

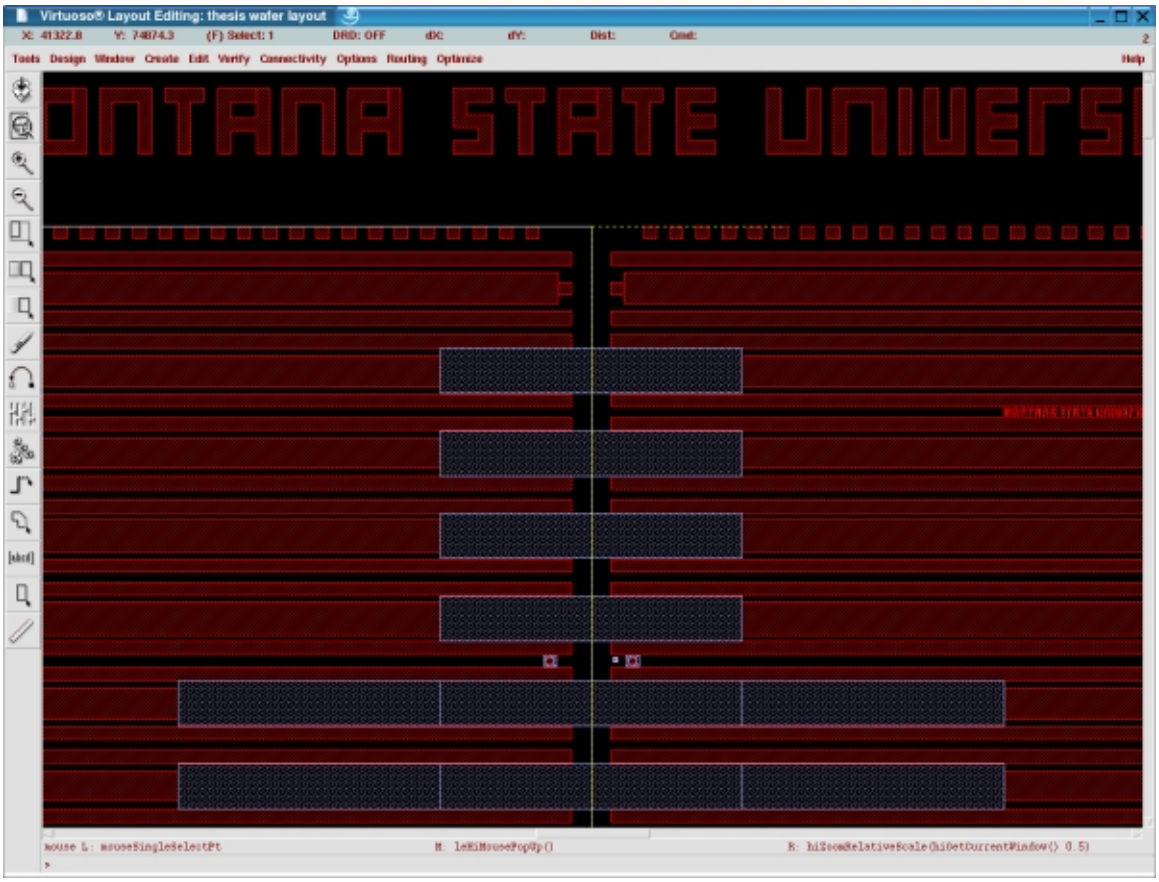

Figure A.1: Shows two dies side by side, the silicon etch regions (blue areas) extend from die to die. The streets are seen between the dies.

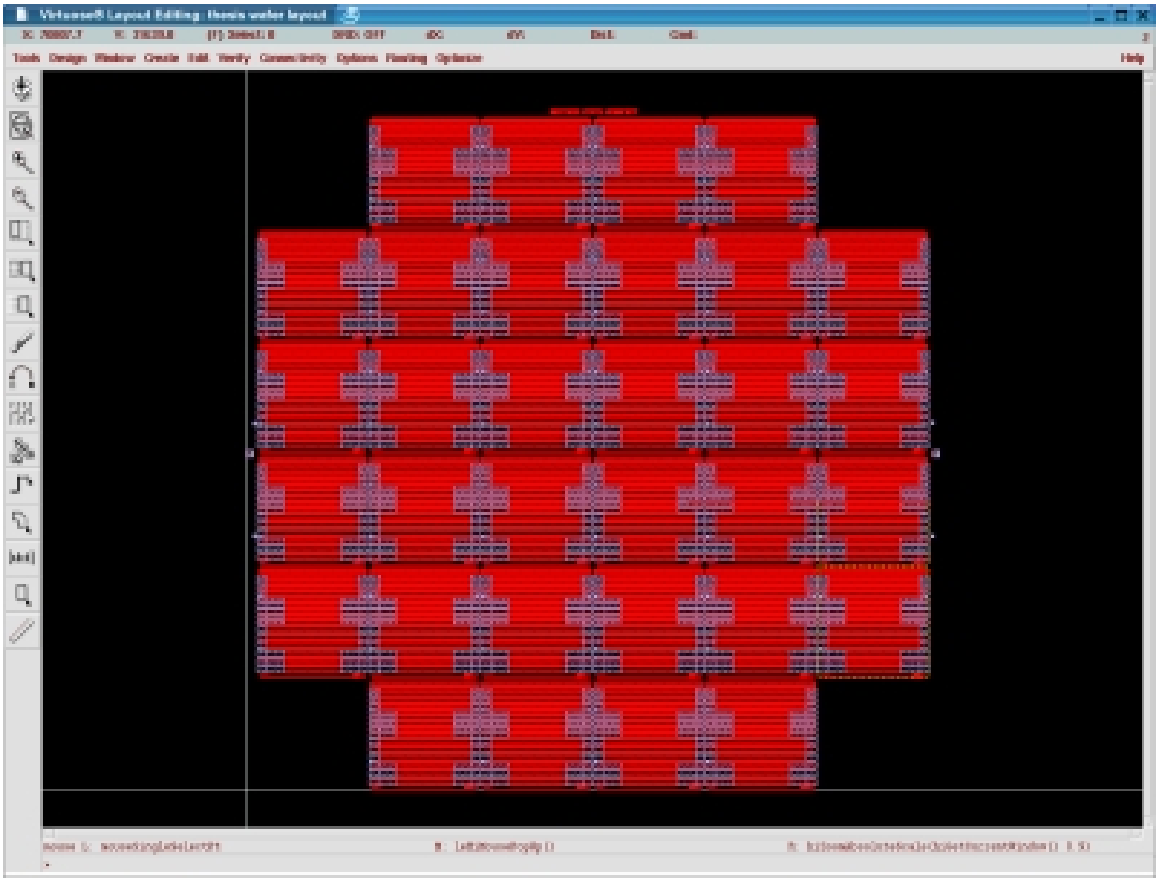

Figure A.2: Shows all 32 dies alligned on a 100mm wafer.

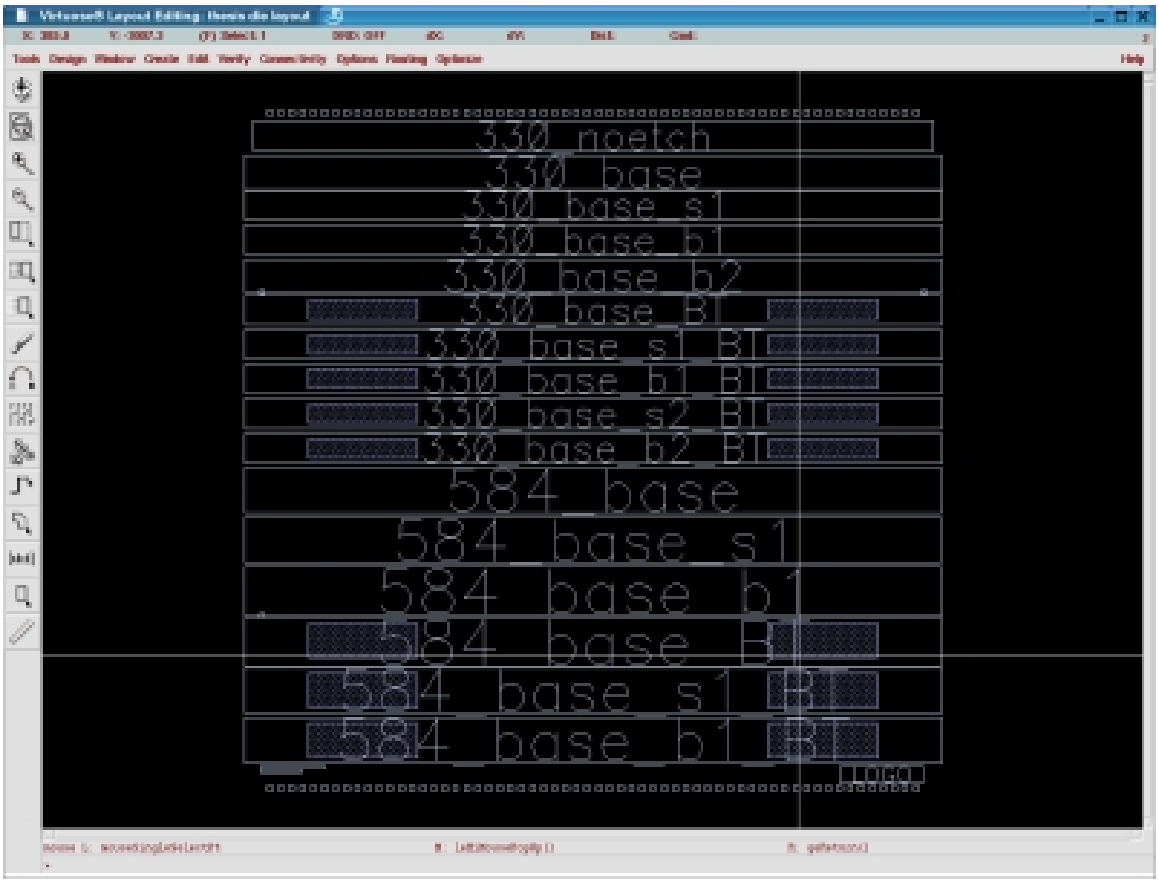

Figure A.3: Shows the different coplanar waveguide structures. The different sizes can be seen by the text describing in terms of small/large and if the signal trace has been increased or decreased.

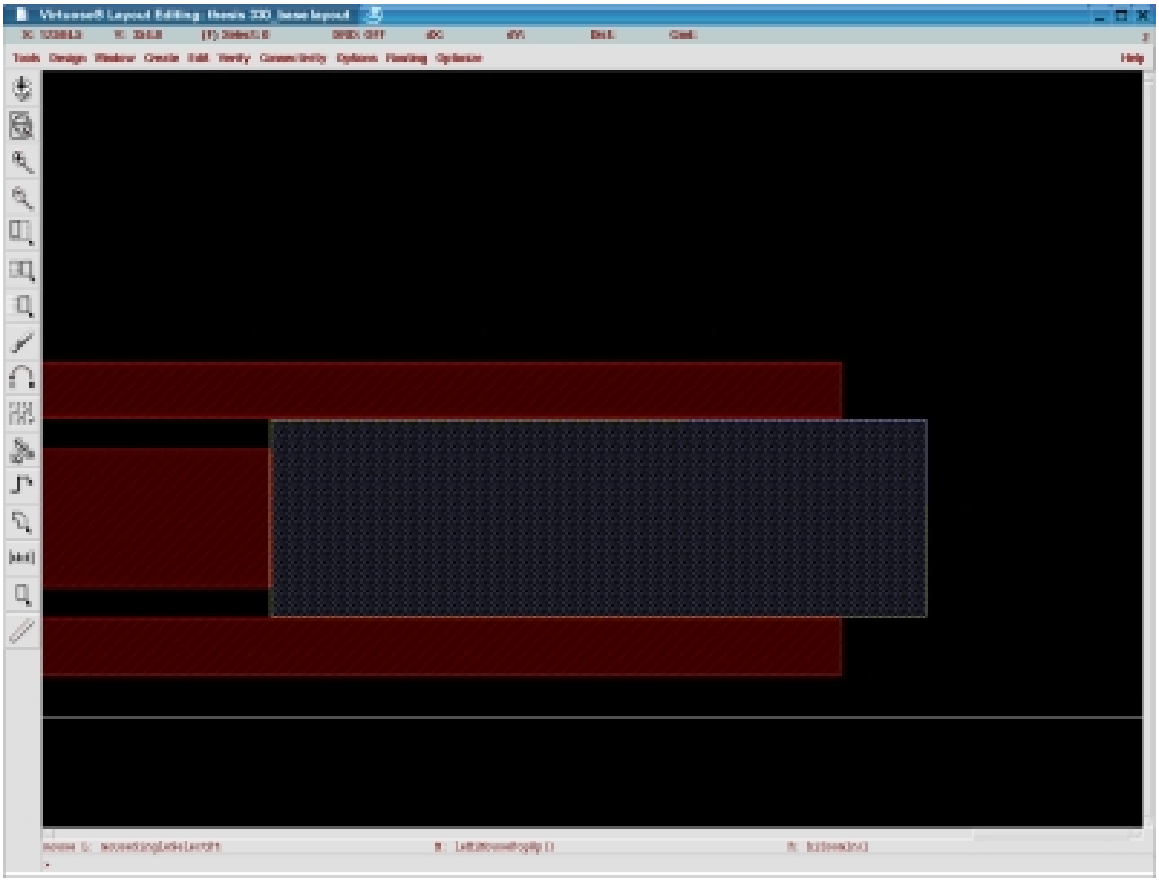

Figure A.4: Shows a trench and coplanar waveguide in detail.

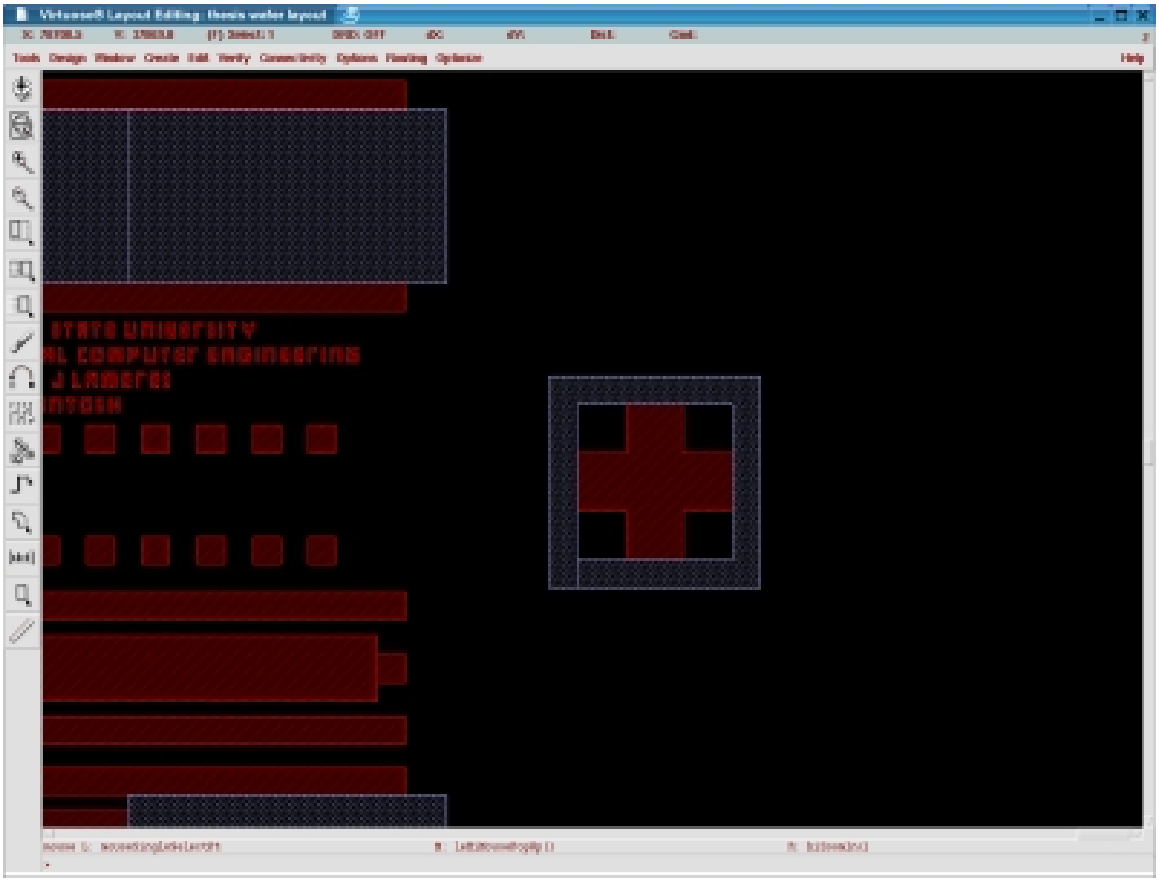

Figure A.5: Shows the alignment marks used to align the two masks